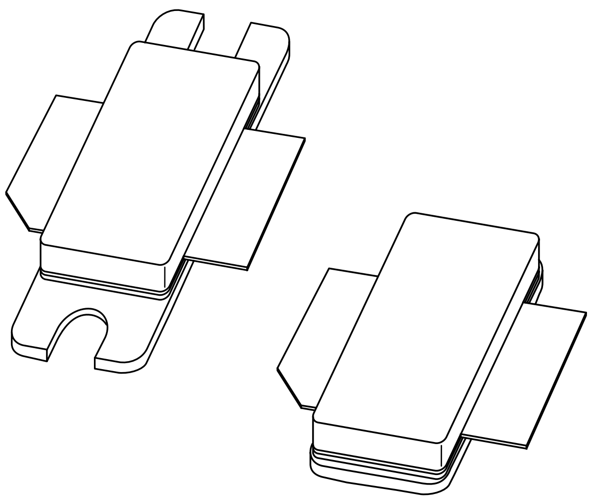
DATA SHEET



BLF0810-90; BLF0810S-90
Base station LDMOS transistors

Preliminary specification 2002 Mar 18

Philips
Semiconductors

PHILIPS

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (750 MHz to 1 GHz).

APPLICATIONS

- Common source class-AB operation in CDMA applications in the 750 to 960 MHz frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistors encapsulated in a 2-lead flange package (BLF0810-90) with a ceramic cap or in a 2-lead earless package (BLF0810S-90). The common source is connected to the flange.

Typical CDMA IS95 performance at standard settings at a supply voltage of 27 V and I_{DQ} = 500 mA

P_L = 18 W
G_P = 16 dB
η = 26 %
ACPR <–45 dBc at 750 kHz and BW = 30 kHz
ACPR <–63 dBc at 1.98 MHz and BW = 30 kHz

PINNING - SOT502A

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange

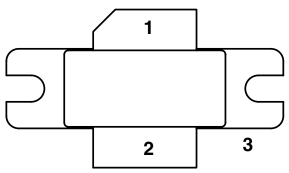


Fig.1 Simplified outline SOT502A (BLF0810-90)

PINNING - SOT502B

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange

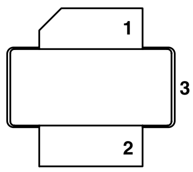


Fig.2 Simplified outline SOT502B (BLF0810S-90)

QUICK REFERENCE DATA

2-tone performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L PEP (W)	G_p (dB)	η_D (%)	d_3 (dBc)
Class-AB	881.4 - 881.6	27	60	typ. 16.5	typ. 35	typ. –30

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L avg (W)	G_p (dB)	η_D (%)	ACPR (dB)
CDMA(1)	881.5	27	18	typ. 16	typ. 26	typ. –46 (2) typ. –63 (3)

Note

1. IS95 CDMA (pilot, Paging, Sync, and Trafic Codes 8 trough 13)
2. ACPR 750 kHz at BW = 30 kHz
3. ACPR 1.98 MHz at BW = 30 kHz.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	75	V
V_{GS}	gate-source voltage		–	±15	V
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	T_h = 25 °C, P_L = 18 W avg, note 1	<0.75	K/W

Note

1. Thermal resistance is determined under RF operating conditions.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 3 mA	75	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 300 mA	4	–	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 36 V	–	–	1	μA
I_{DSX}	on-state drain current	$V_{GS} = V_{GS(th)}$ + 9 V; V_{DS} = 10 V	28	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 10 A	–	4.8	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = 9 V; I_D = 10 A	–	120	–	mΩ

APPLICATION INFORMATION

RF performance in a common source-AB circuit; T_h = 25 °C.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L PEP (W)	G_p (dB)	η_D (%)	d_3 (dBc)
Class-AB	881.4 - 881.6	27	500	60	>16	>35	<–30

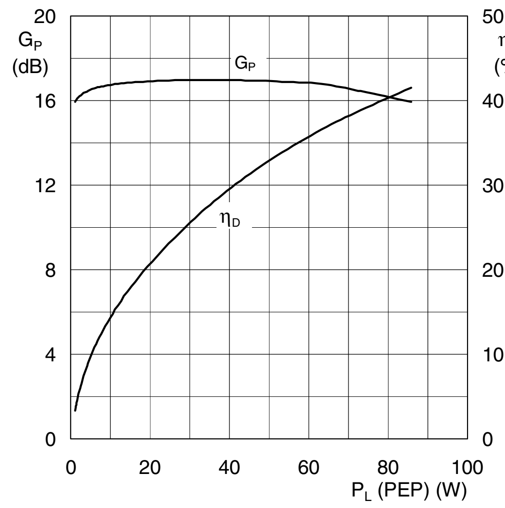
MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L avg (W)	G_p (dB)	η_D (%)	ACPR (dB)
CDMA(1)	881.5	27	500	>16	>15	>26	<–46 (2) <–63 (3)

Note

1. IS95 CDMA (pilot, Paging, Sync, and Trafic Codes 8 trough 13)
2. ACPR 750 kHz at BW = 30 kHz
3. ACPR 1.98 MHz at BW = 30 kHz.

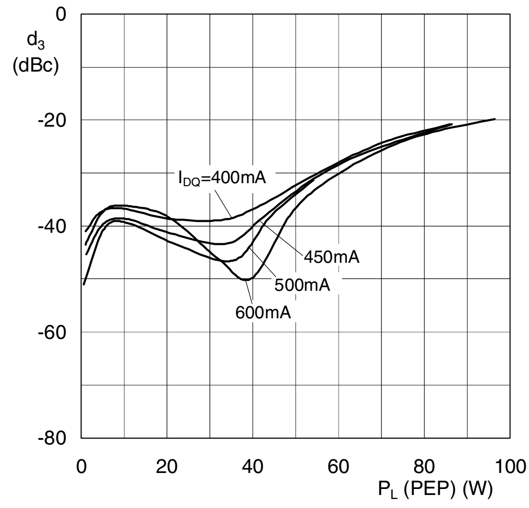
Ruggedness in class-AB operation

The BLF0810-90 and BLF0810S-90 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases at V_{DS} = 27 V; P_L = 60 W (PEP).



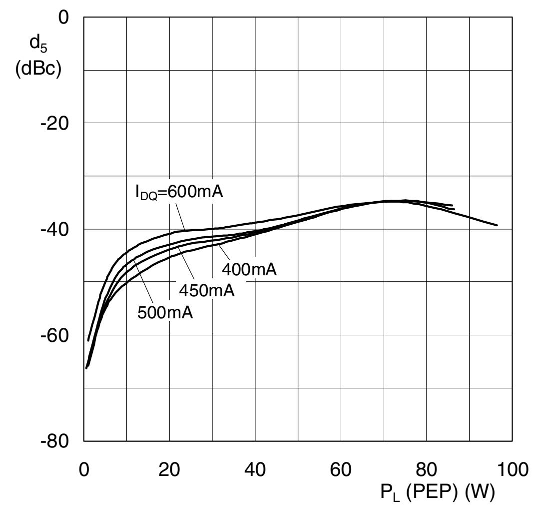
V_{DS} = 27 V; I_{DQ} = 500 mA; f_1 = 881.4 MHz; f_2 = 881.6 MHz.

Fig.3 Power gain and efficiency as functions of peak envelope load power, typical values.



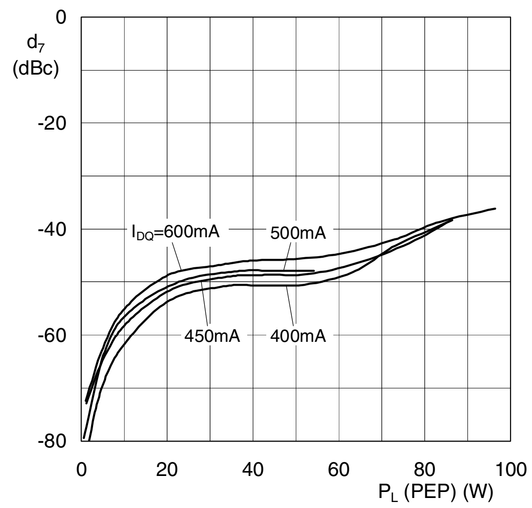
V_{DS} = 27 V; f_1 = 881.4 MHz; f_2 = 881.6 MHz.

Fig.4 Intermodulation distortion as a function of peak envelope load power, typical values.



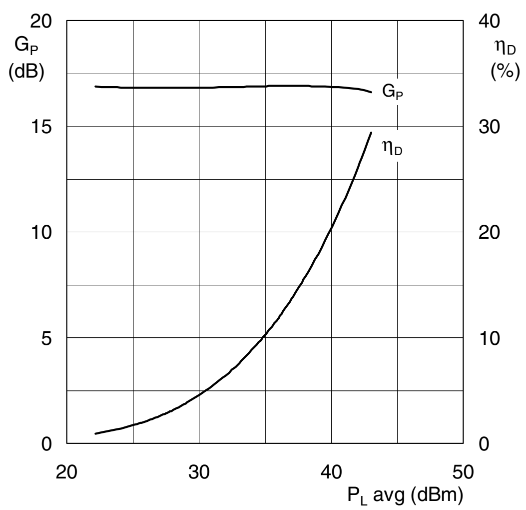
V_{DS} = 27 V; f_1 = 881.4 MHz; f_2 = 881.6 MHz.

Fig.5 Intermodulation distortion as a function of peak envelope load power, typical values.



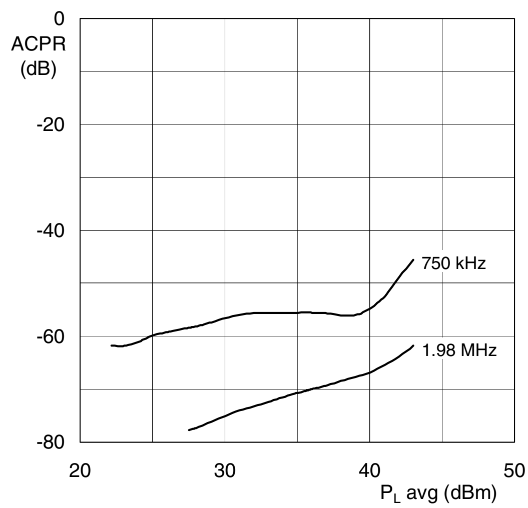
V_{DS} = 27 V; f_1 = 881.4 MHz; f_2 = 881.6 MHz.

Fig.6 Intermodulation distortion as a function of peak envelope load power, typical values.



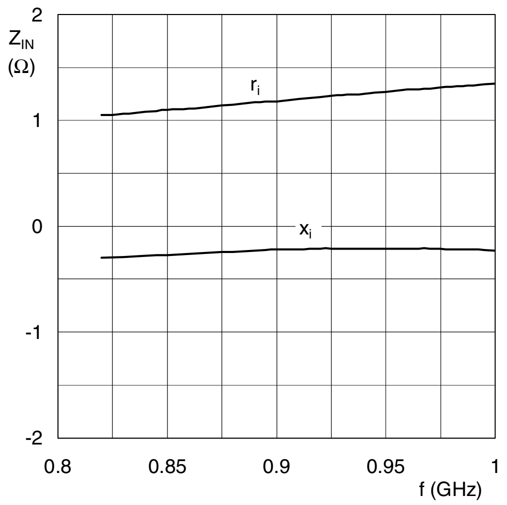
V_{DS} = 27 V; I_{DQ} = 500 mA; f = 881.5 MHz;
measured under CDMA conditions; test signal Standard IS-95

Fig.7 Power gain and efficiency as functions of the average load power, typical values.



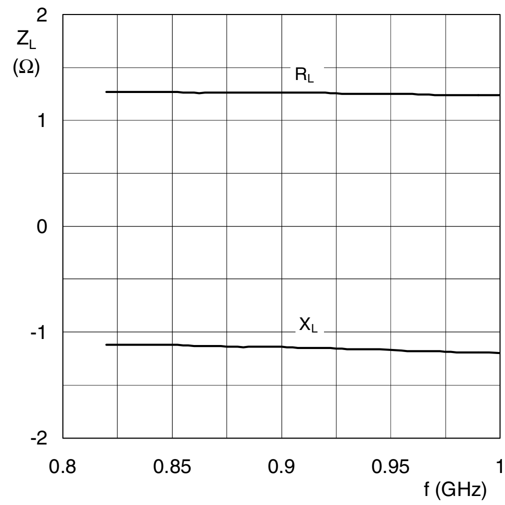
V_{DS} = 27 V; I_{DQ} = 500 mA; f = 881.5 MHz;
measured under CDMA conditions; test signal Standard IS-95

Fig.8 Intermodulation distortion as a function of the average load power, typical values.



Class-AB operation; V_{DS} = 27 V; I_{DQ} = 500 mA; P_L = 18 W.

Fig.9 Input impedance as a function of frequency (series components); typical values.



Class-AB operation; V_{DS} = 27 V; I_{DQ} = 500 mA; P_L = 18 W.

Fig.10 Load impedance as a function of frequency (series components); typical values.

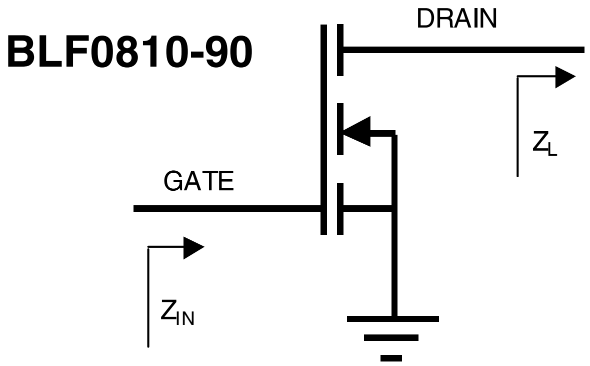


Fig.11 Definition of transistor impedance.

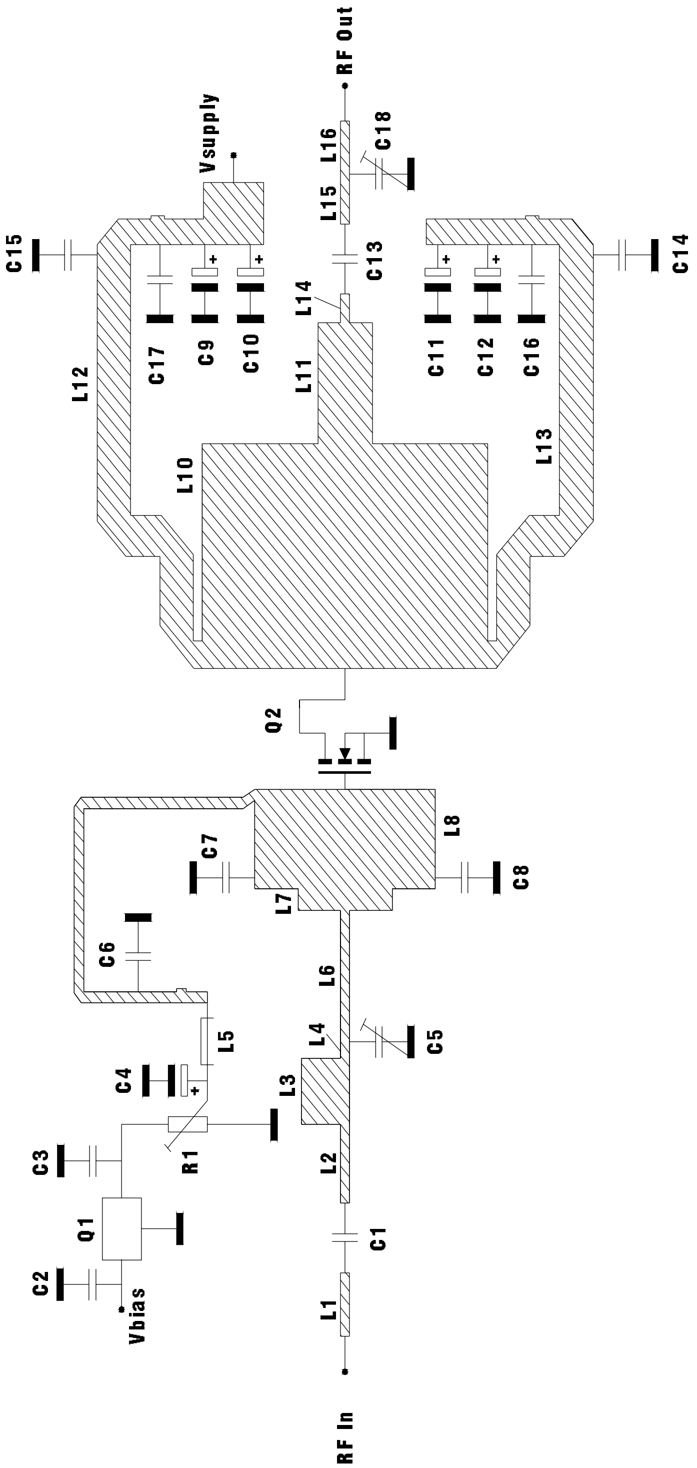
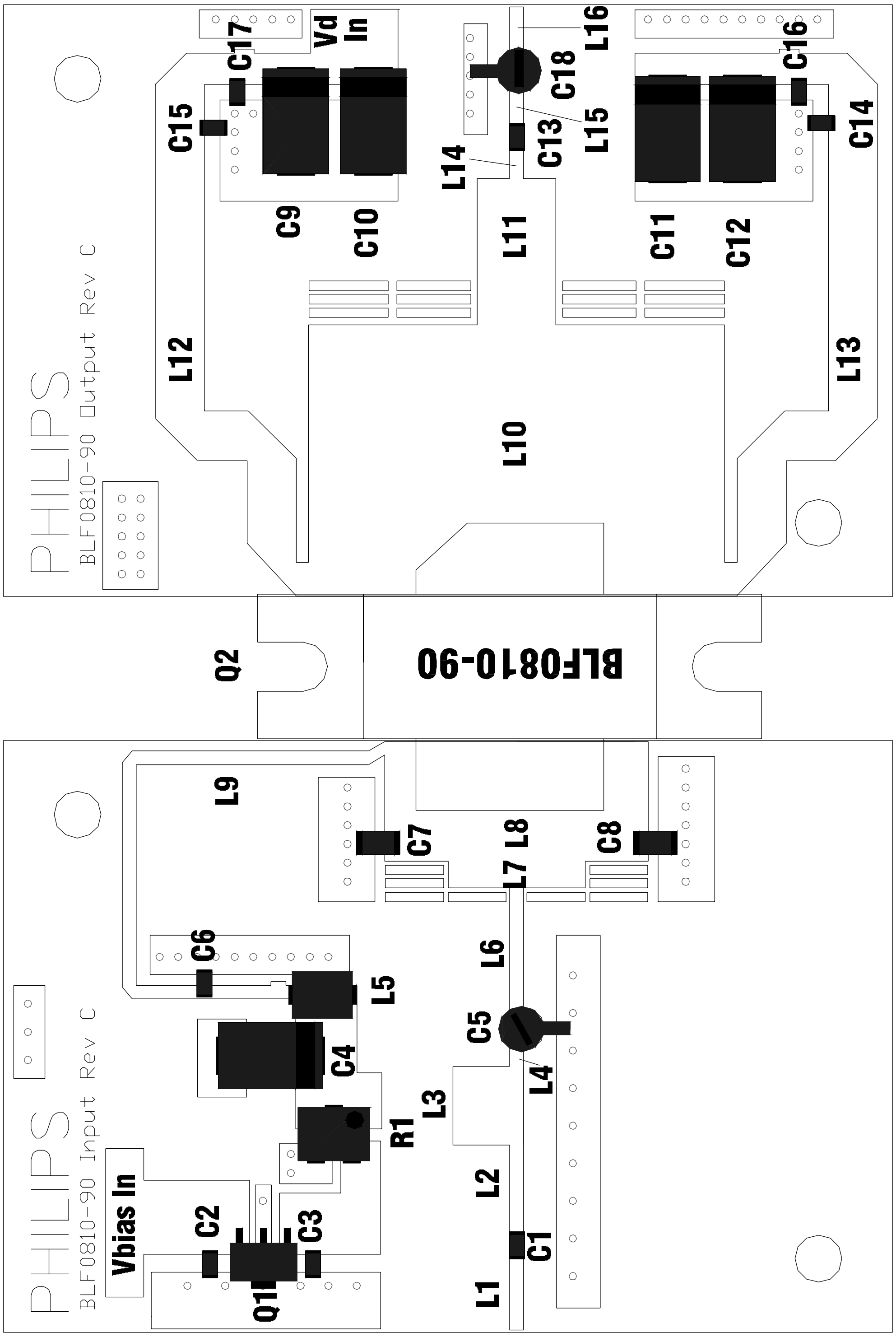


Fig.12 Circuit for 850 to 960 MHz test circuit.



Dimensions in mm.

The components are situated on one side of the copper-clad Rogers 6006 printed-circuit board (ε_r = 6.15); thickness = 25 mils.

The other side is unetched and serves as a ground plane.

Fig.13 Circuit for 850 to 960 MHz test circuit.

List of components

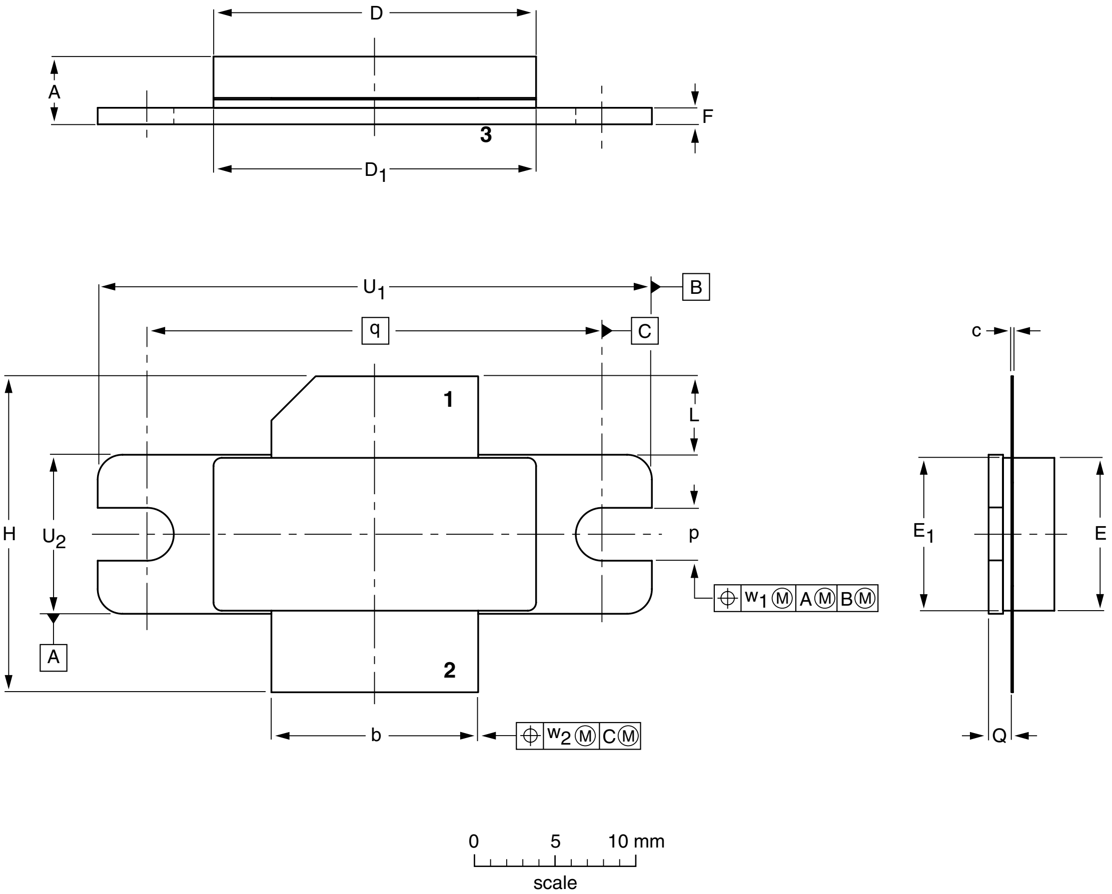
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1, C6, C13, C14, C15, C16, C17	multilayer ceramic chip capacitor; note 1	68 pF	
C2	multilayer ceramic chip capacitor; note 1	330 nF	
C3	multilayer ceramic chip capacitor; note 1	100 nF	
C4, C9, C10, C11, C12	tantalum capacitor	10 μF	
C5, C18	air trimmer capacitor	8 pF	
C7, C8	multilayer ceramic chip capacitor	8.2 pF	
R1	potentiometer	1 kΩ	
Q1	7808 voltage regulator		
Q2	BLF0910-140 LDMOS transistor		
L1	stripline; note 2		204 × 36 mils
L2	stripline; note 2		253 × 36 mils
L3	stripline; note 2		210 × 188 mils
L4	stripline; note 2		94 × 36 mils
L5	Ferroxcube		
L6	stripline; note 2		380 × 36 mils
L7	stripline; note 2		71 × 363 mils
L8	stripline; note 2		319 × 700 mils
L9	stripline; note 2		1724 × 36 mils
L10	stripline; note 2		721 × 1106 mils
L11	stripline; note 2		389 × 210 mils
L12, L13	stripline; note 2		1470 × 131 mils
L14	stripline; note 2		92 × 36 mils
L15, L16	stripline; note 2		165 × 36 mils

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. The striplines are on a double copper-clad Rogers 6006 printed-circuit board (ε_r = 6.15); thickness = 25 mils.

PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT502A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.99	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.157	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

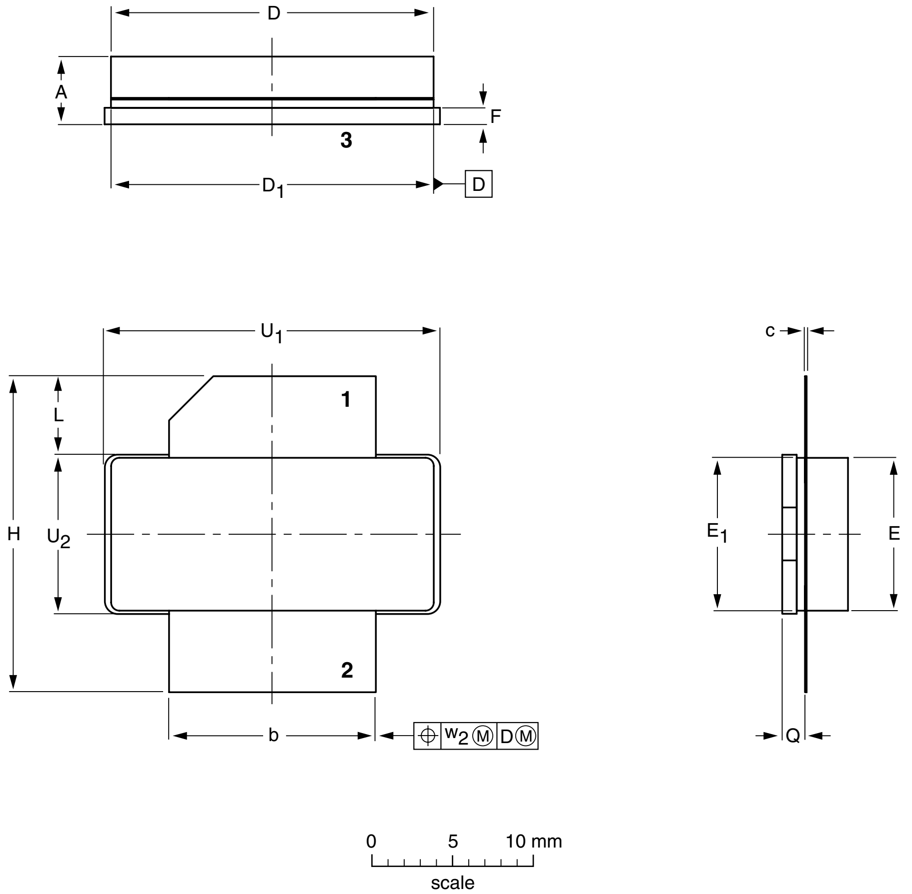
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT502A						~~99-10-13~~ 99-12-28

PACKAGE OUTLINE

Earless flanged LDMOST ceramic package; 2 leads **SOT502B**

Package under development

Philips Semiconductors reserves the right to make changes without notice.



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.99	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.157	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT502B						~~99-12-16~~ 99-12-28

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

Printed in The Netherlands budgetnum/printrun/ed/pp13 Date of release: 2002 Mar 18 Document order number: 9397 750 09548

Let's make things better.

Philips
Semiconductors

PHILIPS