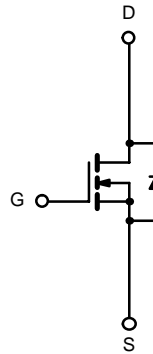
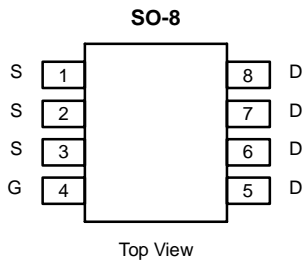




N-Channel 100-V (D-S) MOSFET

175°C Rated
Maximum Junction Temperature
High-Efficiency
PWM Optimized

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.025 @ $V_{GS} = 10$ V	7.9
	0.028 @ $V_{GS} = 6.0$ V	7.5



Ordering Information: Si4486EY
Si4486EY-T1 (with Tape and Reel)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	100		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 175^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	7.9	5.4	A
		$T_A = 85^\circ\text{C}$	6.1	4.2	
Pulsed Drain Current	I_{DM}	40			
Avalanche Current	I_{AR}	30			
Repetitive Avalanche Energy (Duty Cycle $\leq 1\%$)	E_{AR}	L = 0.1 mH	45		mJ
Continuous Source Current (Diode Conduction) ^a			I_S	3.1	1.5
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	3.8	1.8	W
		$T_A = 85^\circ\text{C}$	2.3	1.1	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	t ≤ 10 sec	33	40	$^\circ\text{C/W}$
		Steady State	70	85	
Maximum Junction-to-Foot (Drain)	R_{thJF}	17	21		

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

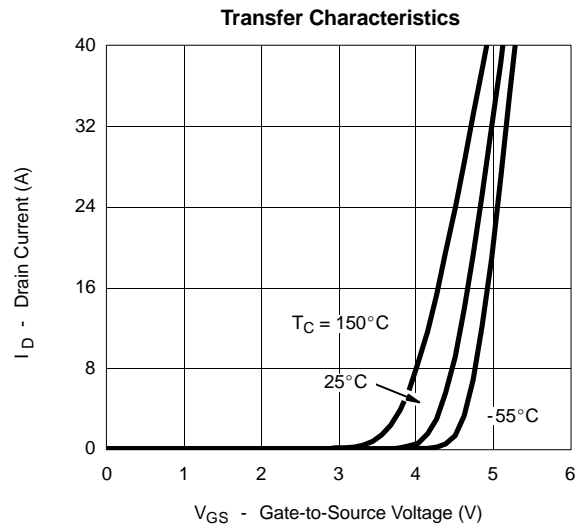
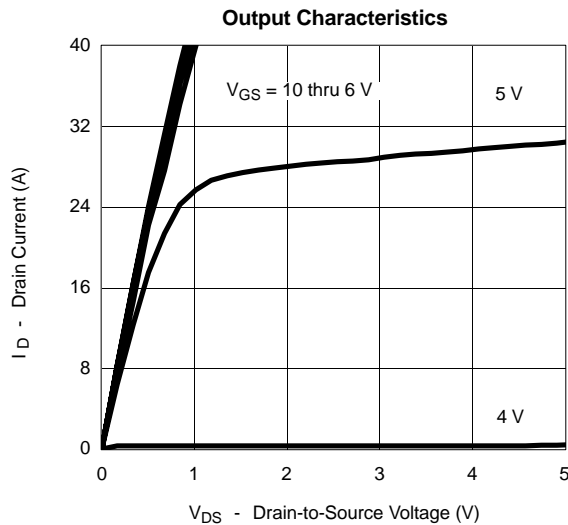


SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V			1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 85 °C			20	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	40			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 7.9 A		0.021	0.025	Ω
		V _{GS} = 6.0 V, I _D = 7.5 A		0.023	0.028	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 7.9 A		35		S
Diode Forward Voltage ^a	V _{SD}	I _S = 3.1 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 7.9 A		36	44	nC
Gate-Source Charge	Q _{gs}			10		
Gate-Drain Charge	Q _{gd}			8.6		
Gate Resistance	R _g		0.5	1.27	2.2	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 50 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		20	40	ns
Rise Time	t _r			10	20	
Turn-Off Delay Time	t _{d(off)}			46	90	
Fall Time	t _f			26	50	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 3.1 A, di/dt = 100 A/μs		50	80	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

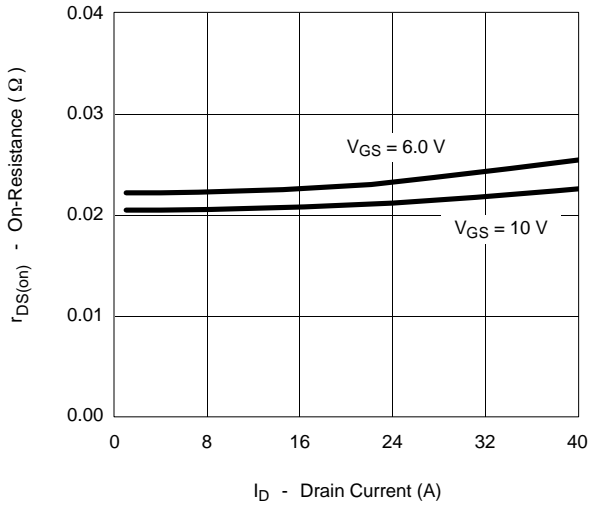
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



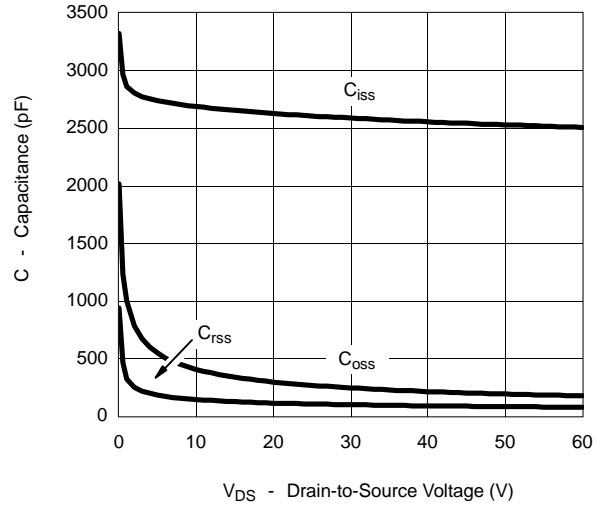


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

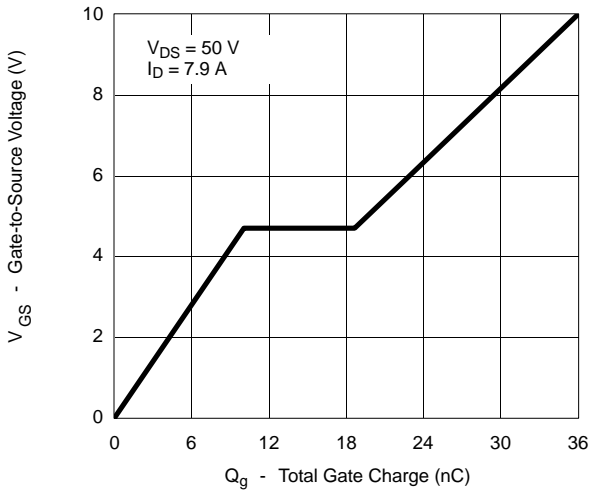
On-Resistance vs. Drain Current



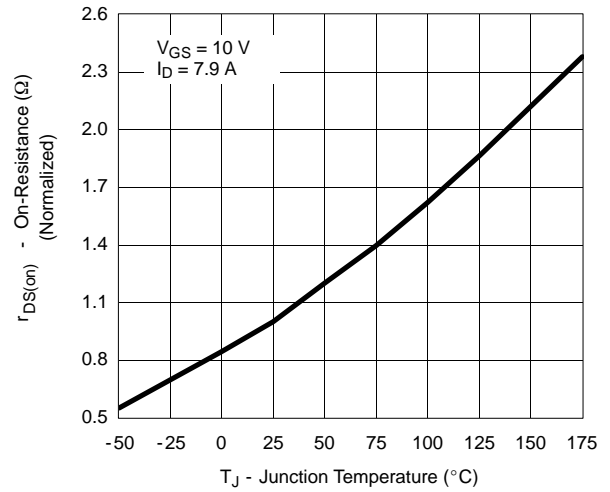
Capacitance



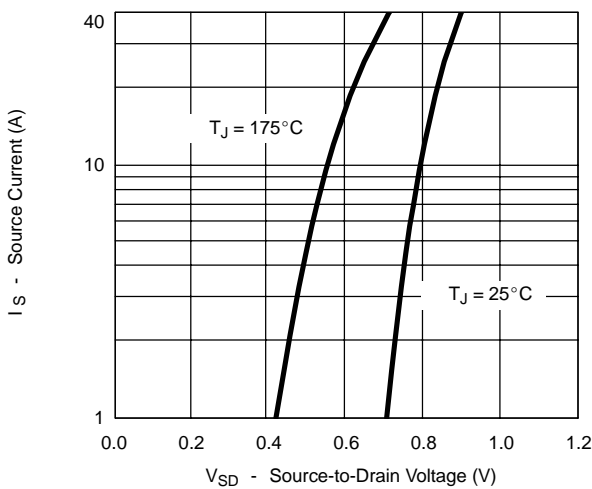
Gate Charge



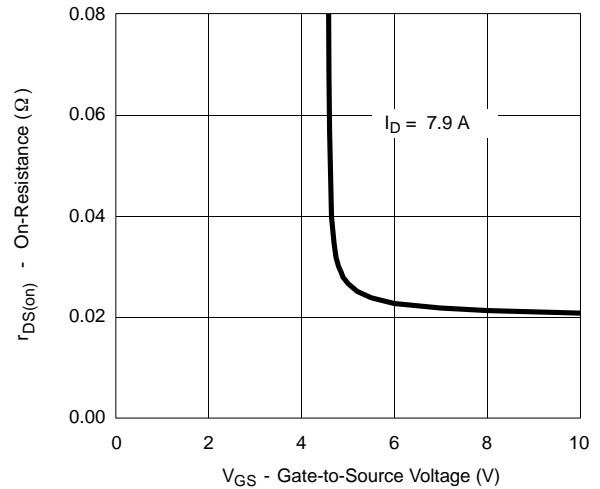
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

