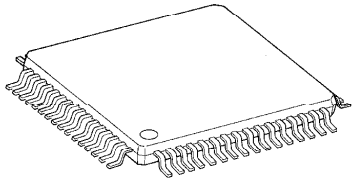
CCD AREA IMAGE SENSOR CCD(Charge Coupled Device)

TC6307AF

TCD5481D DRIVING PULSE GENERATOR IC

The TC6307AF is a CMOS LSI developed to drive the TCD5481D CCD area image sensor. It can be combined with a vertical clock driver and a synchronous signal generator IC to constitute the CCD area image sensor driving circuit.



LQFP64-P-1010-0.50B

Weight : 0.33g (Typ.)

FEATURES

- Generation of all timing pulses required to drive TCD5481D.
- Correspondence with electronic shutter from 1/60 to 1/8000 sec.
- Generation of sampling pulses for CDS signal processing.

MAXIMUM RATINGS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~7.0	V
Input Voltage	V_{INA}	−0.3~V_{DDA} + 0.3	V
	V_{INB}	−0.3~V_{DDB} + 0.3	
Input Current	I_{IN}	±10	mA
Storage Temperature	T_{stg}	−40~125	°C

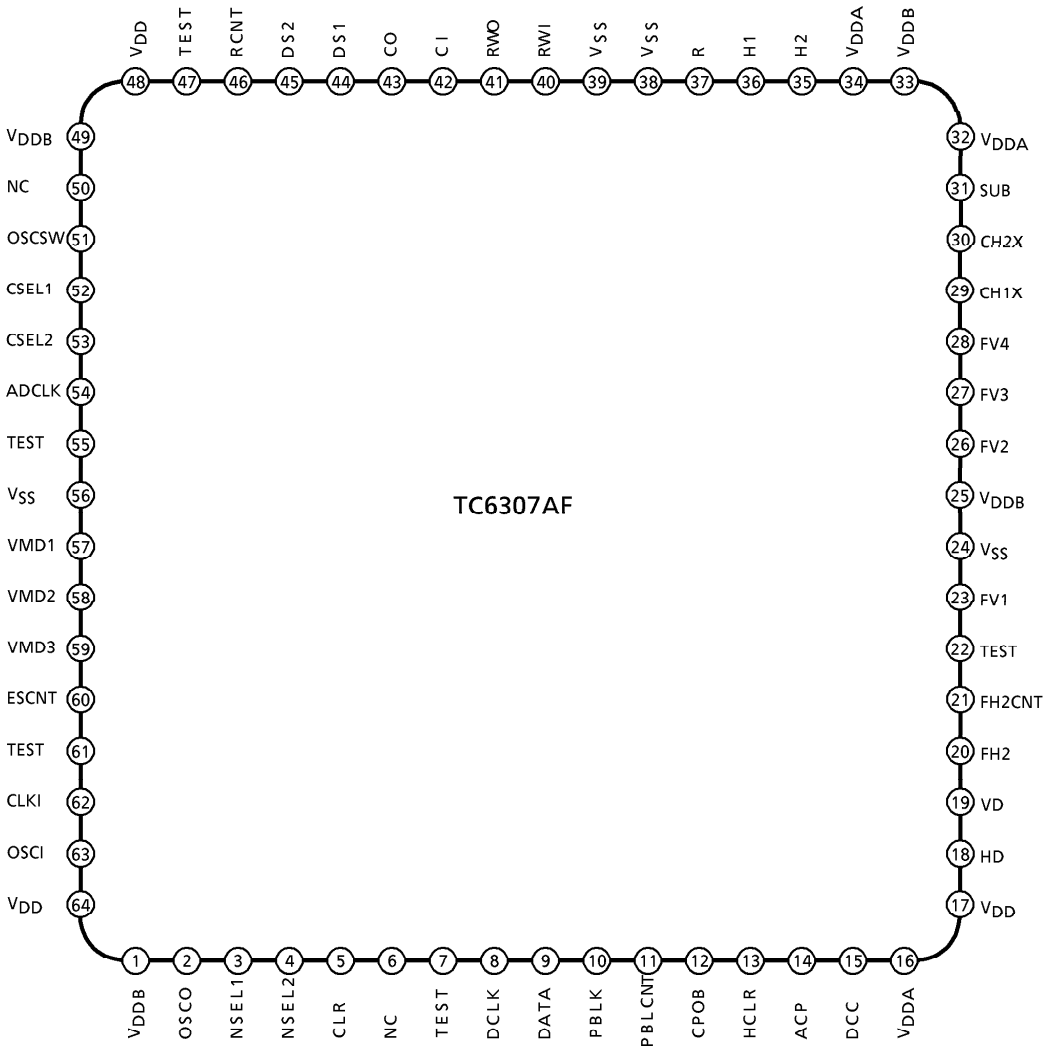
RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DDA}	4.75~5.25	V
	V_{DDB}	0.3~3.6	
Operating Temperature	T_{opr}	−10~70	°C

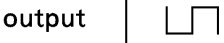
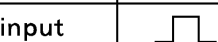
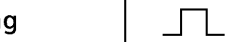
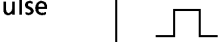
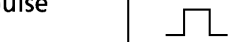
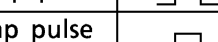
ELECTRICAL CHARACTERISTICS (V_{SS} = 0V, V_{DDA} = 4.75~5.25V, V_{DDB} = 3.0~3.6V, Ta = 0~70°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Input Voltage	"H" Level	V_{IH}	—		V_{DDB} × 0.8	—	—	V
	"L" Level	V_{IL}			—	—	V_{DDB} × 0.2	
Input Current	"H" Level	I_{IH}	—	$V_{INA} = V_{DDA}$, $V_{INB} = V_{DDB}$	– 10	—	10	μA
				$V_{INA} = V_{DDA}$, $V_{INB} = V_{DDB}$ (included PULL-DOWN)	10	—	200	
	"L" Level	I_{IL}		$V_{INA} = V_{DDB} = V_{SS}$	– 10	—	10	
				$V_{INA} = V_{DDB} = V_{SS}$ (included PULL-UP)	– 200	—	– 10	
Output Voltage	"H" Level	V_{OH}	—	I_{OH} = – 8mA, H1, H2	2.4	—	—	V
				I_{OH} = – 8mA, RS				
				I_{OH} = – 4mA, Other output				
	"L" Level	V_{OL}		I_{OL} = 8mA, H1, H2	—	—	0.4	
				I_{OL} = 8mA, RS				
				I_{OL} = 4mA, Other output				
Static Consumption Current		I_{DD}	—	CL = 0pF, V_{DD} = 5V, Ta = 25°C	—	—	100	μA

PIN ASSIGNMENT



PIN FUNCTION

PIN No.	SYMBOL	I/O	NAME	POLARITY	FUNCTION
1	V_{DDB}	—	Power supply	—	Connected to power supply 3.3±0.30V
2	OSCO	O	Oscillating output		Oscillating output terminal of quartz oscillator. (2fck)
3	NSEL1	I	Vertical read position setting input	—	Used to set the vertical read position.
4	NSEL2				
5	CLR	I	All clear input	—	Returns circuit to initial settings. Normal operation in "H" level Clear settings in "L" level
6	NC	—	Not connected	—	—
7	TEST	—	—	—	Test terminal (open for normal use)
8	DCLK	I	—		Clock input terminal for serial data.
9	DATA	I	Serial data input		Serial data input terminal.
10	PBLK	O	Pre-blanking		Pre-blanking pulse output. "H" level indicates the erase period.
11	PBLCNT	I	Pre-blanking switching input	—	Switches pre-blanking pulse. PBLK2 in "H" level PBLK1 in "L" level
12	CPOB	O	OB clamp pulse output		Clamps the OB part of the CCD output signal with clamp pulse. Does not include vertical return line period.
13	HCLR	O	ϕH clear pulse output		Displays horizontal CCD transmission stop period (horizontal cycle) with pulse output during horizontal return line period.
14	ACP	O	Analog clamp pulse		Analog clamp pulse output
15	DCC	O	Digital clamp pulse output		Digital clamp pulse output
16	V_{DDA}	—	Power supply	—	Connected to power supply 5.0±0.25V
17	V_{DD}	—	Power supply	—	Connected to power supply 5.0±0.25V
18	HD	I	Horizontal drive pulse input	—	Inputs HD pulse of cycle signal generator IC.
19	VD	I	Vertical drive pulse input	—	Inputs VD pulse of cycle signal generator IC.
20	FH2		FH2/FH2B output		"L" level repeated at "H" level for each H at color discrimination signal, and frame cycle resets.
21	FH2CNT	I	FH2/FH2B switching input	—	Switching of FH2 and FH2B output FH2B in "H" level FH2 in "L" level
22	TEST	—	—	—	Test terminal (open for normal use)

PIN No.	SYMBOL	I / O	NAME	POLARITY	FUNCTION
23	FV1	O	Vertical CCD drive pulse		Vertical CCD drive pulse ϕV1 connected to the inversion type vertical clock driver.
24	V_{SS}	—	GND	—	GND
25	V_{DDB}	—	Power supply	—	Connected to power supply 5.0 ± 0.25V
26	FV2	O	Vertical CCD drive pulse		Vertical CCD drive pulse ϕV2 connected to the inversion type vertical clock driver.
27	FV3	O	Vertical CCD drive pulse		Vertical CCD drive pulse ϕV3 connected to the inversion type vertical clock driver.
28	FV4	O	Vertical CCD drive pulse		Vertical CCD drive pulse ϕV4 connected to the inversion type vertical clock driver.
29	CH1X	O	ϕV1 charge pulse output		CCD drive charge pulse ϕV1 connected to the inversion type vertical clock driver.
30	CH2X	O	ϕV3 charge pulse output		CCD drive charge pulse ϕV3 connected to the inversion type vertical clock driver.
31	SUB	O	Electronic shutter pulse		SUB substrate pulse connected to the inversion type driver.
32	V_{DDA}	—	Power supply	—	Connected to power supply 5.0 ± 0.25V
33	V_{DDB}	—	Power supply	—	Connected to power supply 3.3 ± 0.30V
34	V_{DDA}	—	Power supply	—	Connected to power supply 5.0 ± 0.25V
35	H2	O	Horizontal CCD drive pulse		Horizontal CCD drive pulse connected to ϕH2 gate of the CCD image sensor.
36	H1	O	Horizontal CCD drive pulse		Horizontal CCD drive pulse connected to ϕH1 gate of the CCD image sensor.
37	R	O	Reset gate pulse		Reset gate pulse connected to ϕRS gate of the CCD image sensor.
38	V_{SS}	—	GND	—	GND
39	V_{SS}	—	GND	—	GND
40	RWI	I	Input for adjusting reset width	—	Output terminal for adjusting reset width. The RWO output is delayed with a capacitor and resistor connected to the input of RWI.
41	RWO	O	Input for adjusting reset width		Input terminal for adjusting reset width. The RWO output is delayed with a capacitor and resistor connected to the input of RWI.
42	CI	I	—	—	Supplemental buffer input terminal
43	CO	O	—	—	Supplemental buffer output terminal. Pulse input to CI is output through the inversion buffer.
44	DS1	O	—		CDS pulse 1 output
45	DS2	O	—		CDS pulse 2 output

PIN No.	SYMBOL	I / O	NAME	POLARITY	FUNCTION
46	RCNT	—	ϕR output transfer input	—	ϕRS pulse logic switching input. Positive logic in "H" level Negative logic in "L" level
47	TEST	—	—	—	Test terminal (open for normal use)
48	V_{DD}	—	Power supply	—	Connected to power supply 5.0 ± 0.25V
49	V_{DDB}	—	Power supply	—	Connected to power supply 3.3 ± 0.30V
50	NC	—	Not connected	—	—
51	OSCSW	I	—	⊔⊓	Internal oscillation and external clock input switching input terminal.
52	CSEL1	I	Horizontal transfer pulse phase switching input	—	H1, H2, DS1, DS2, and R output phase switching input.
53	CSEL2				
54	ADCLK	O	—	⊔⊓	Digital clock output
55	TEST	—	—	—	Test terminal (open for normal use)
56	V_{SS}	—	GND		GND
57	VMD1	I	—	—	Electronic shutter setting input
58	VMD2				
59	VMD3				
60	ESCNT	I	Electronic shutter speed data input switching	—	Electronic shutter speed data input switching terminal. Serial setting mode in "H" level Parallel setting mode in "L" level
61	TEST	—	—	—	Test terminal (open for normal use)
62	CLKI	I	External clock input		External clock input terminal
63	OSCI	I	Oscillation input	—	Oscillating input terminal of quartz oscillator.
64	V_{DD}	—	Power supply	—	Connected to power supply 5.0 ± 0.25V

[Explanation of output buffer cell-type]

(1) Output buffer A-type

Terminals used : H1, H2, R

Summary : I_O = 8.0mA output standard buffer (when V_{DD} = 5.0V)

(2) Output buffer B-type

Terminals used : PBLK, CPOB, ACP, DCC, FH2, FV1, FV2, FV3, FV4, CH1X, CH2X, SUB, RWO, CO, DS1, DS2

Summary : I_O = 4.0mA output standard buffer (when V_{DD} = 3.3V)

(3) Output buffer C-type

Terminals used : ADCLK

Summary : I_O = 8.0mA output standard buffer (when V_{DD} = 3.3V)

(4) Output buffer D-type

Terminals used : HCLK

Summary : I_O = 24.0mA output standard buffer (when V_{DD} = 3.3V)

(5) Output buffer E-type

Terminals used : OSCO

Summary : I_O = 4.0mA output OSC buffer (when V_{DD} = 3.3V)

[Setting of Vertical Read Position]

The vertical read position can be switched between NSEL1 and NSEL2 input. The serial setting mode is set when NSEL1 and NSEL2 input are in "H" level.

NSEL1	NSEL2	Vertical read position	Vertical transfer levels
L	L	Middle of screen	28
H	L	Fixed at top of screen	0
L	H	Fixed at bottom of screen	60
H	H	Serial setting mode	0~60

[Setting of the Shutter Speed]

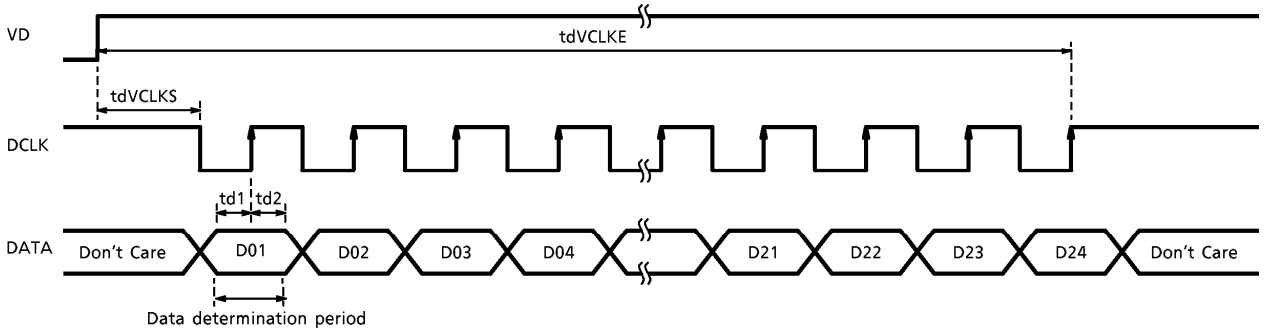
In setting the shutter speed, use ESCNT input to select either the parallel setting mode or the serial setting mode. When ESCNT input is in "L" level, the parallel setting mode is set, and the shutter speed is set with VMD1, VMD2, and VMD3. When ESCNT input is in "H" level, the parallel setting mode is set, and the shutter speed can be controlled regardless of VMD1, VMD2, or VMD3.

VMD1	VMD2	VMD3	ESCNT	Shutter speed
L	L	L	L	1 / 8000 sec.
H	L	L	L	NTSC: 1 / 100 sec. (flickerless mode)
L	H	L	L	1 / 250 sec.
H	H	L	L	1 / 500 sec.
L	L	H	L	1 / 1000 sec.
H	L	H	L	1 / 2000 sec.
L	H	H	L	1 / 4000 sec.
H	H	H	L	NTSC : 1 / 60 sec. (normal mode)
×	×	×	H	Serial setting mode (*1)

(*1) Set the shutter speed within the range below.
NTSC : IH~133H (in 1H units) (134~254H (in 2H units).
(Use the shutter speed within the CCD specifications.)

[Serial Setting Mode]

Use NSEL1, NSEL2 or ESCNT to select the vertical read position or shutter speed serial setting mode. Serial data is input with VD, DCLK, and DATA.



td1 > 1μs, td2 > 1μs (td1 and td2 apply to each of the 24 bits)
tdVCLXE < 6H TDVCLKS > 1μ

The data is fed into the shutter speed controller when DCLK pulse raises. The data is organized in 24 bits with the functions described below. Binary data is input to data to designate the vertical read position and shutter speed settings. When more than 24 bits of data are input, only the first 24 bits remain valid.

Bit1 : LSB
Bit2 : LSB — Charge read field setting; Vertical transfer level setting (Remaining charge sweep level) — Vertical read position setting (EIS operation)
Bit8 : LSE

Bit9 : LSB
Bit16 : LSE — No setting

Bit17 : LSB
Bit24 : LSE — Shutter speed setting

Set the binary data according to the following logic format.

Setting of the Vertical Read Position

The relationship between the vertical transfer level and binary data is defined as follows.

Vertical transfer level (n defined as binary number)
NTSC : $n = 64 - (\text{vertical transfer level})$ $(4 \leqq n \leqq 64)$

When bits 1 to 8 are in "H" level, EIS is turned off and the middle of the screen is read. The relationship between the serial data and the color discrimination signal of the initial level line of the CCD output signal is defined as shown below.

When EIS = OFF

Bit2	Bit1	FH2 (Color discrimination)	Field
L	L	H (2B-G)	Second, fourth
L	H	L (2R-G)	First, third
H	L	L (2R-G)	Second, fourth
H	H	H (2B-G)	First, third

Setting of the Shutter Speed

The relationship between the shutter speed and binary data is defined by the following logic format.

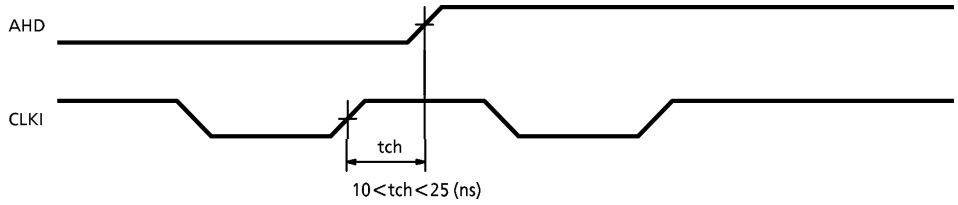
Shutter speed (n defined as binary number)

NTSC : $[262 - 2n]$ H $(4 \leqq n \leqq 64)$
$[(262 - 64) - n]$ H $(65 \leqq n \leqq 197)$

When bits 17 to 24 are in "H" level, CH1X and CH2X are fixed in "H" level regardless of ESCNT input.

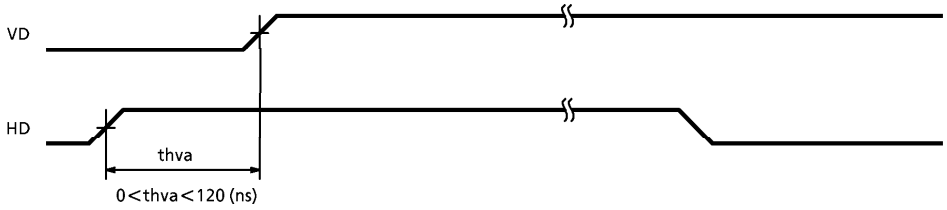
Input pulse timing chart

(1) CLKI-AHD input phase relationship

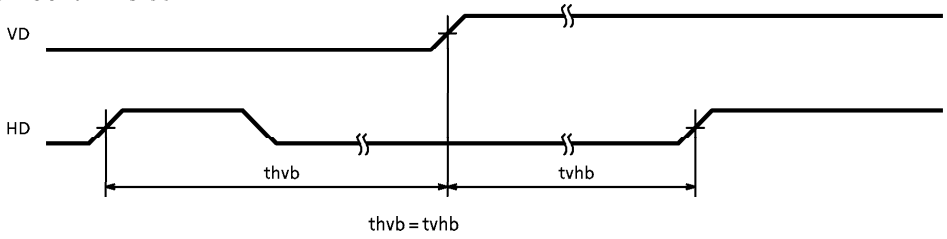


(2) VD-HD input phase relationship

① First and third fields

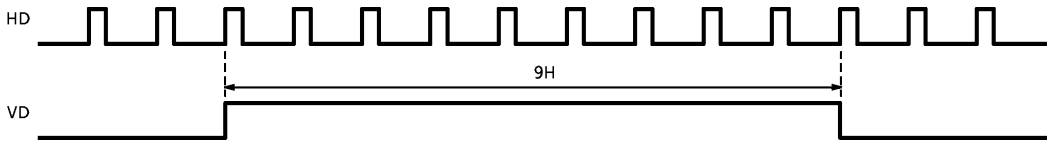


② Second and fourth fields

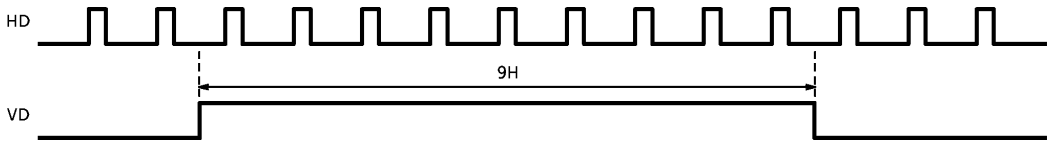


(3) VD-HD input phase relationship

① First and third fields

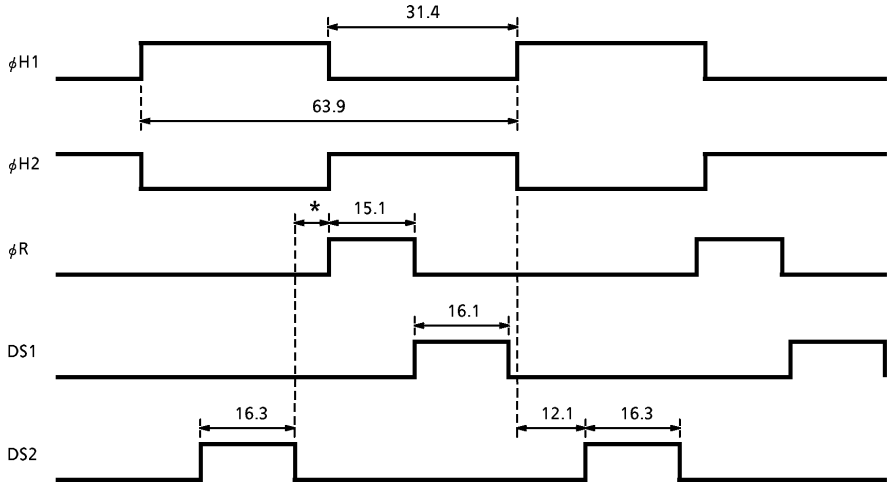


② Second and fourth fields

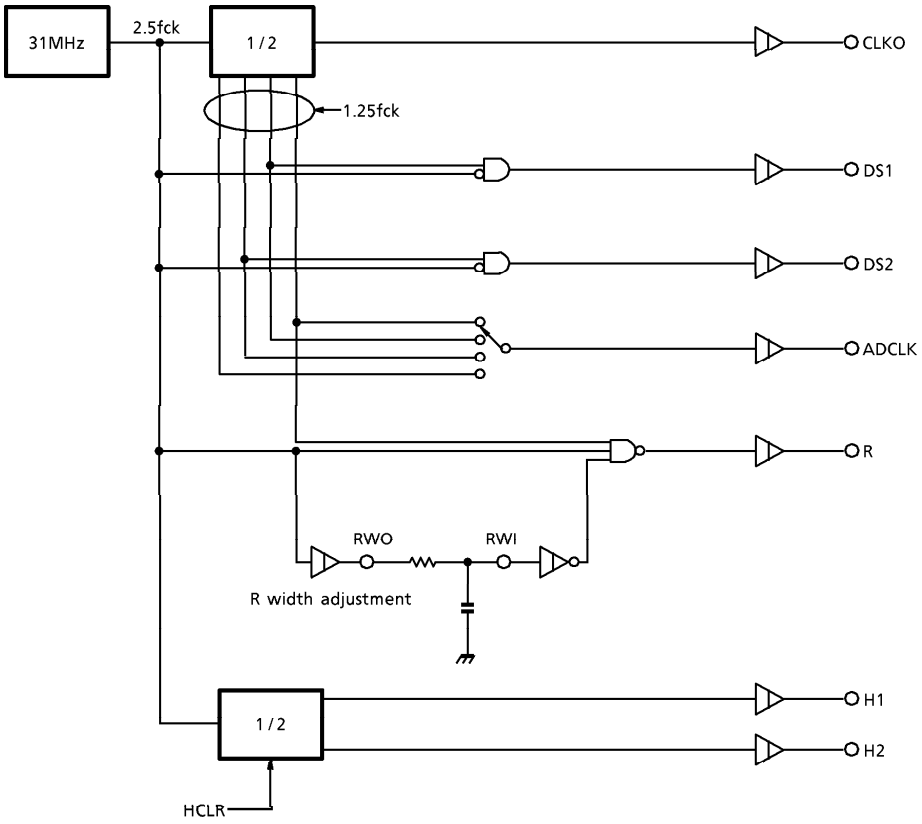


Reset Timing Chart

Unit: ns

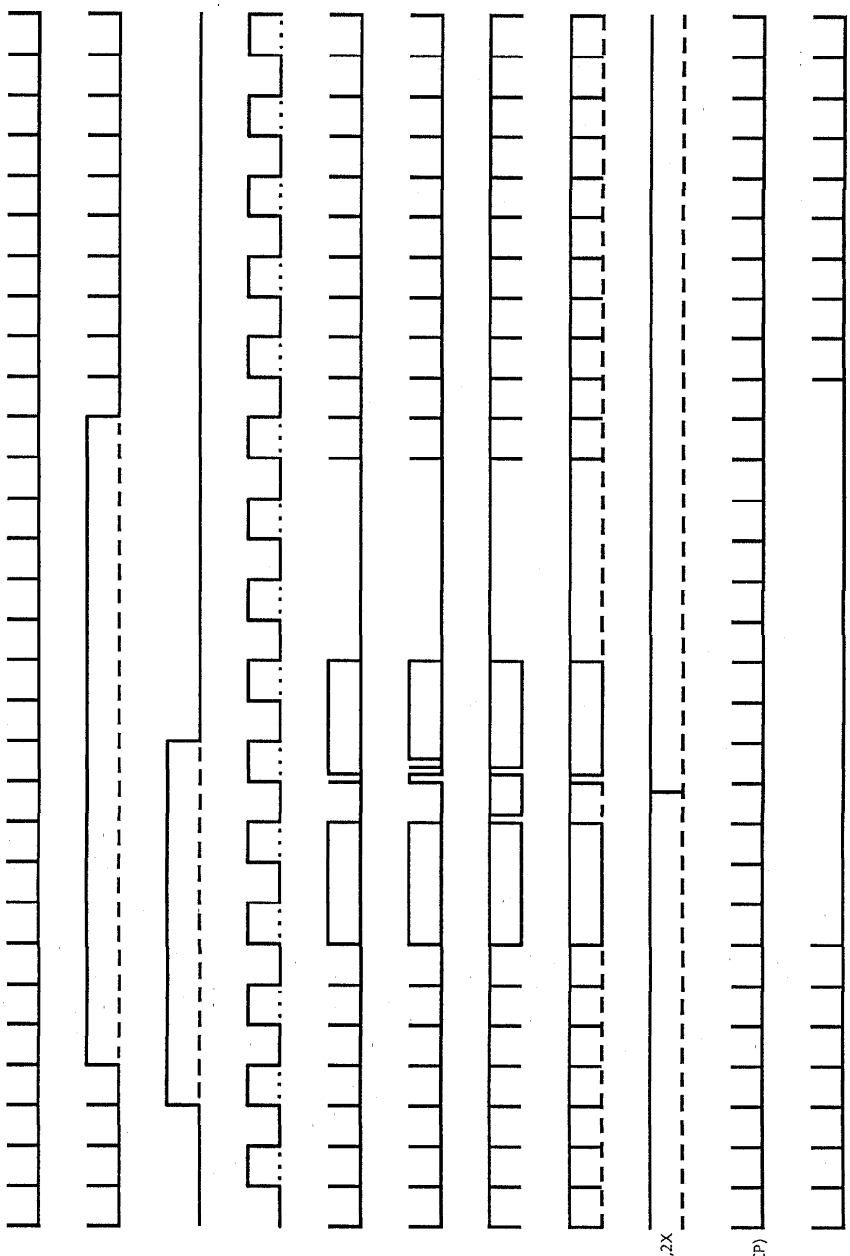


* MIN : 3.12, TYP : 6.64, MAX : 11.72
Simulation values when 10 pF load connected to external circuit.


31MHz
2.5fck
1 / 2
CLKO
1.25fck
DS1
DS2
ADCLK
R
RWO
RWI
R width adjustment
1 / 2
H1
H2
HCLR

Vertical Rate Timing Char

First and third fields



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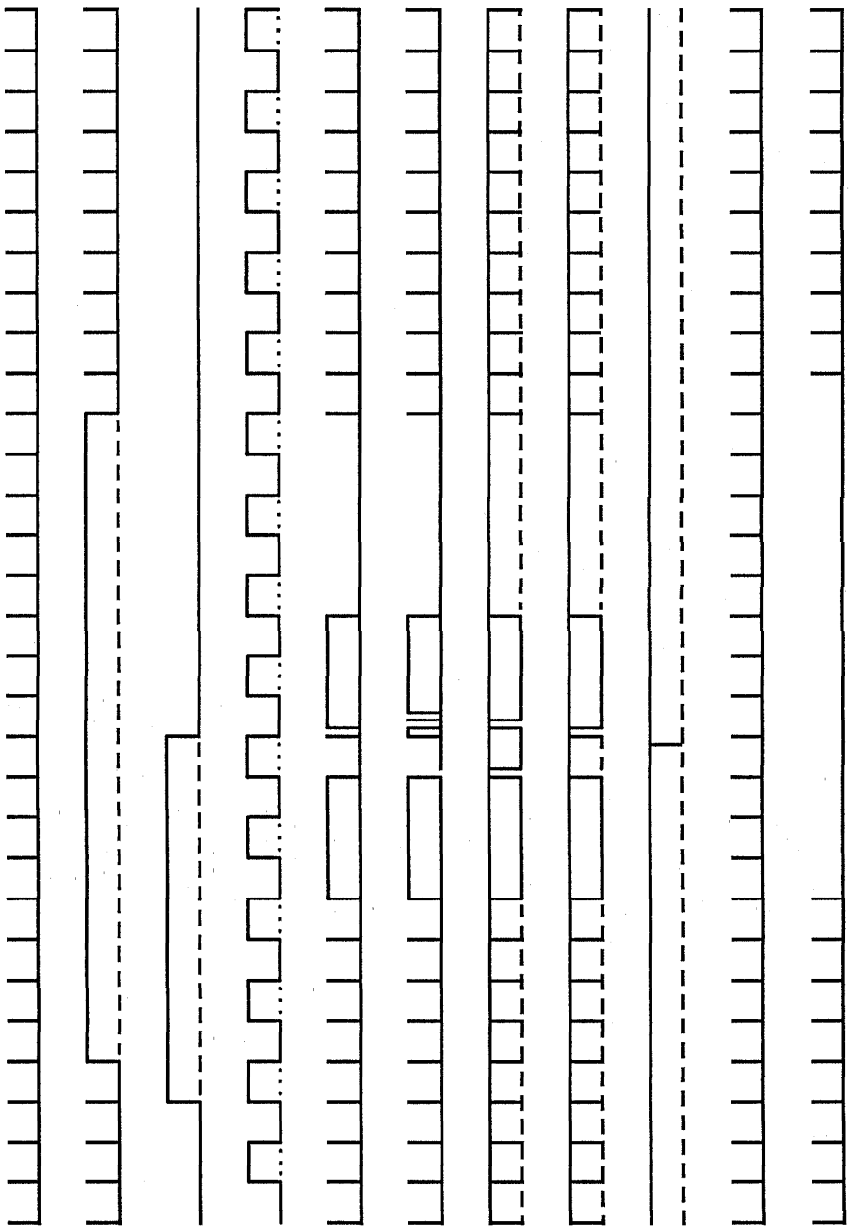
Vertical Rate Timing Chart

Second and fourth fields



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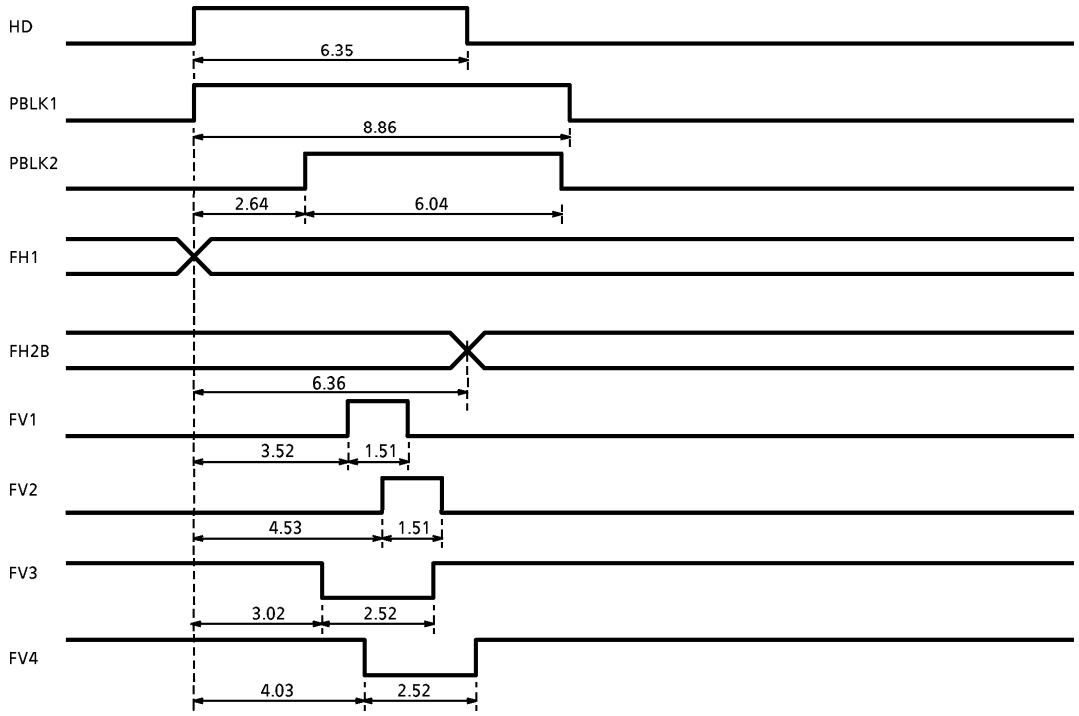
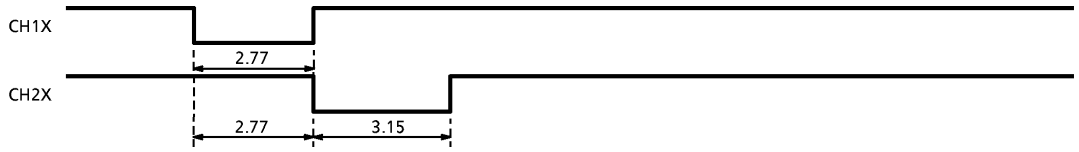
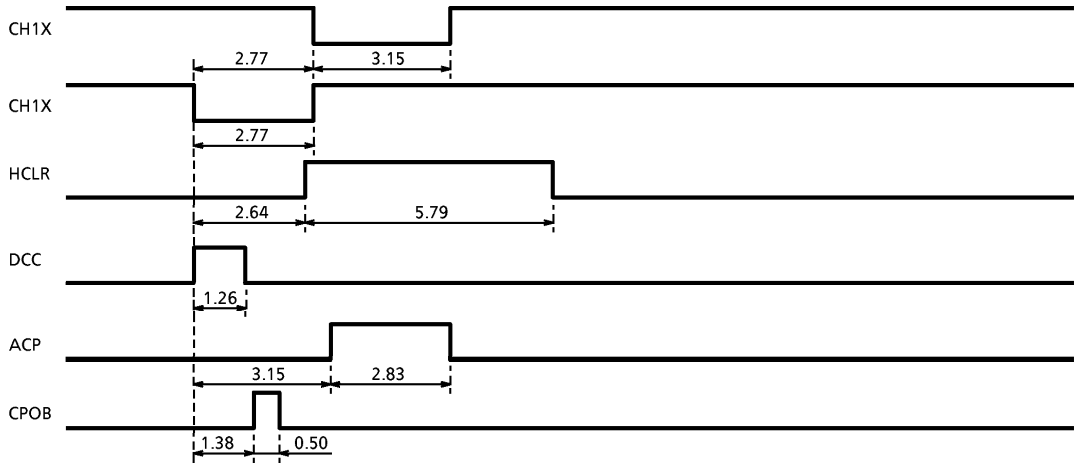
Horizontal Rate Timing Chart Units: (μs)



At first and third fields



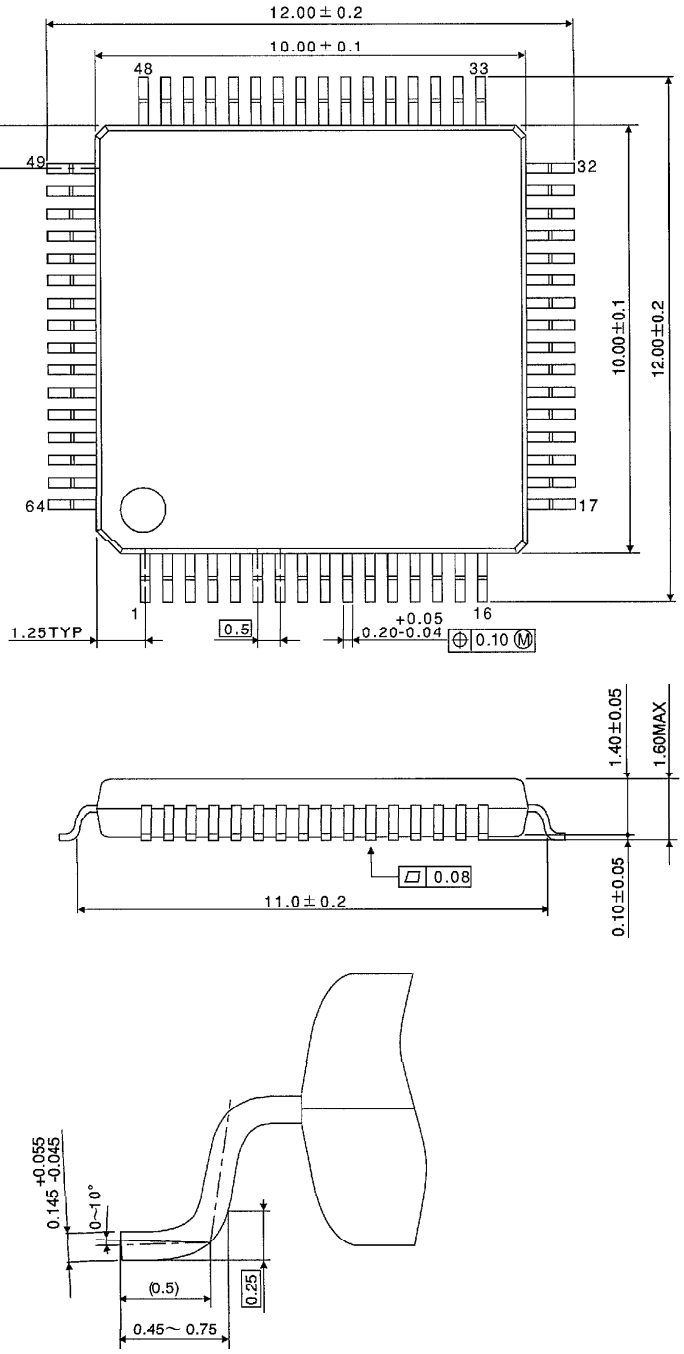
At second and fourth fields



OUTLINE DRAWING

LQFP64-P-1010-0.50B

Unit : mm



Weight : 0.33g (Typ.)