ATM SWITCH USING S/UNI-ATLAS, QRT, AND QSE

REFERENCE DESIGN

PRELIMINARY

ISSUE 2: JUNE 1999

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	Apr 1999	Document created.
2	July 1999	Added implementation description

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1 DEFINITIONS

CPCI	Compact PCI. The PCI Industrial Computer Manufacturers Group (PICMG) defines a set of standards for the use of PCI in industrial applications. The standards can be found at http://www.picmg.org.
Eurocard	IEEE 1101.1 specifies the mechanical requirements for rack mounted cards. The standard is referred to commonly as the eurocard standard.
HP	Horizontal Pitch. Refers to horizontal increments in card width. One HP is 0.2 inches. A 4HP card occupies 0.8 inches of rack width.
SPort Card	The SPort Card reference design is a switch port card based on the S/UNI-TETRA, S/UNI-ATLAS, and QRT devices from PMC-Sierra. This design is detailed in document PMC-980583, available from PMC-Sierra's website.
U	Unit. Refers to height increments in card sizes in the euorocard standard. One U is 1.75 inches. A 6U card, then, is 10.5 inches in height.

2 FEATURES

- Demonstrates interoperability between QSE and SPort Card reference designs
- Modified CPCI form factor improves portability
- Centralized switch fabric timing

3 REFERENCES

- PMC-Sierra, Inc. *"Switch Port Card Reference Design"* PMC-980583
- PMC-Sierra, Inc. *"QSE Reference Design"*, PMC-981288
- PCI Industrial Computer Manufacturer's Group, *"CompactPCI Specification",*September 1997
- IEEE Computer Society, "IEEE Standard for Mechanical Core Specifications for Microcomputers using IEC 60603-2 Connectors", IEEE 1101.1-1998

4 DESCRIPTION

This reference design describes a 5G ATM switch using the SPort Card and QSE reference designs. The SPort Card reference design is a 4xOC-3 switch port card using the PM5351 S/UNI-TETRA, PM7324 S/UNI-ATLAS, and PM73487 QRT devices. The QSE reference design is a 10Gbps switch core building block using two PM73488 QSE devices. These two boards are designed to be housed in a 9U subrack, using a 3U 8-slot Compact PCI backplane for microprocessor access and a 6U custom backplane for card interconnect.

For simplicity, this design uses an eight slot compact PCI backplane. Since the processor card takes up two slots, the chassis will support 6 cards. The chassis will then be able to support multiple switch fabric configurations. The components of the system described in this document are:

- Subrack mechanical specification
- Custom high speed backplane
- QSE Switch Cards, PMC-981288
- SPort Card reference designs, PMC-980585
- Timing card
- cPCI backplane
- cPCI Processor card
- Custom backplane

The design guidelines used in this design may be scaled to very large fabrics, as the serialiser and deserialiser components greatly reduce the required interconnection through the backplane. Section 7 attempts to describe how a large system might be designed by extending the design practices.

5 FUNCTIONAL DESCRIPTION

The components that make up the ATM Switch are detailed in the subsections that follow.

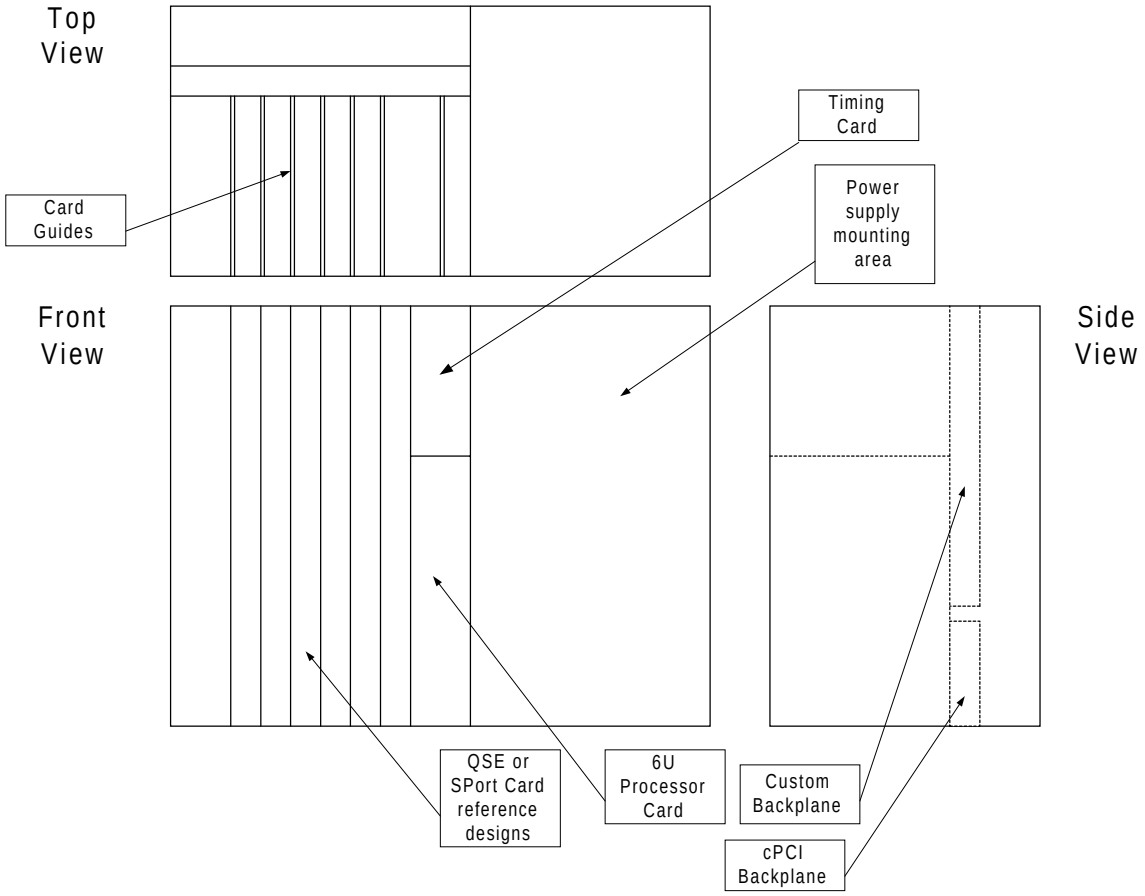
5.1 Subrack Mechanical specification

A 19 inch, 9U rack conforming to the eurocard standard is used to house SPort cards, QSE switch core cards, timing card, processor card, and backplane interconnect. The following is a non-exhaustive list of features:

- 19 inch width with brackets for rackmounting
- Support for 6 IEEE 1101.1 'Eurocard' format 9U, 160mm deep, 4HP cards each with access to the cPCI bus.
- Mounting area for 3U cPCI Backplane
- Mounting area for 6U Custom backplane
- Support for 6U, 160mm deep, 8HP cPCI processor card
- Support for a single 3U, 160mm deep, 4HP card. No micrprocessor access is given to this card.
- Mounting area for Power supply, which connects to the cPCI backplane as well as the custom backplane.

A line drawing of the subrack is shown below in Figure 1.

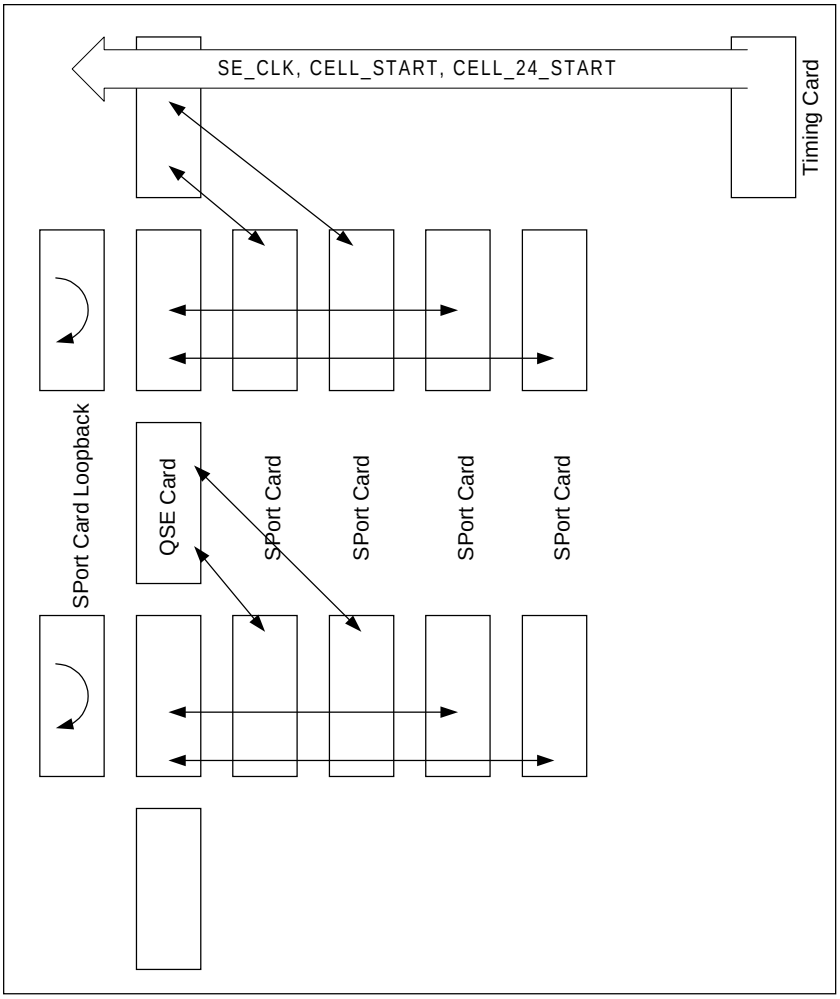
Figure 1 - Subrack Line Drawing



5.2 Custom high speed backplane

The backplane is a 6U height passive backplane using AMP HS3 controlled impedance connectors. The backplane routes high-speed signals beteen the QSE switch cards and ATLAS/QRT port cards. The backplane also carries timing information from the timing card to the switch cards and port cards. Power for the timing card is also sourced from the backplane. Depending on the power required by each of the cards, the analog power supply for each of the port cards and switch cards may also be sourced from the backplane. A block diagram of the backplane is illustrated below in Figure 2. The leftmost slot, slot 6, is intended to loopback a port card in order to test the analog portion of the board. Slot 5 is a QSE card slot. Slots 4 through 1 are port card slots. Slot 0 is for the timing card, above the processor card. Each port card connects to one of the 16 available ports on the QSE card. Unused ports on the QSE card are looped back in order to test the analog portion of the board.

Figure 2 - Switch Fabric Backplane



5.3 QSE Switch Cards, PMC-981288

The QSE switch card reference design (PMC-981288) is used as a building block for the scalable switch fabric. The QSE switch card reference design has 16 bidirectional ports, each of which can interface to a single SPort Card reference design. The QSE switch card is 9U in height. For more information, refer to document PMC-981288.

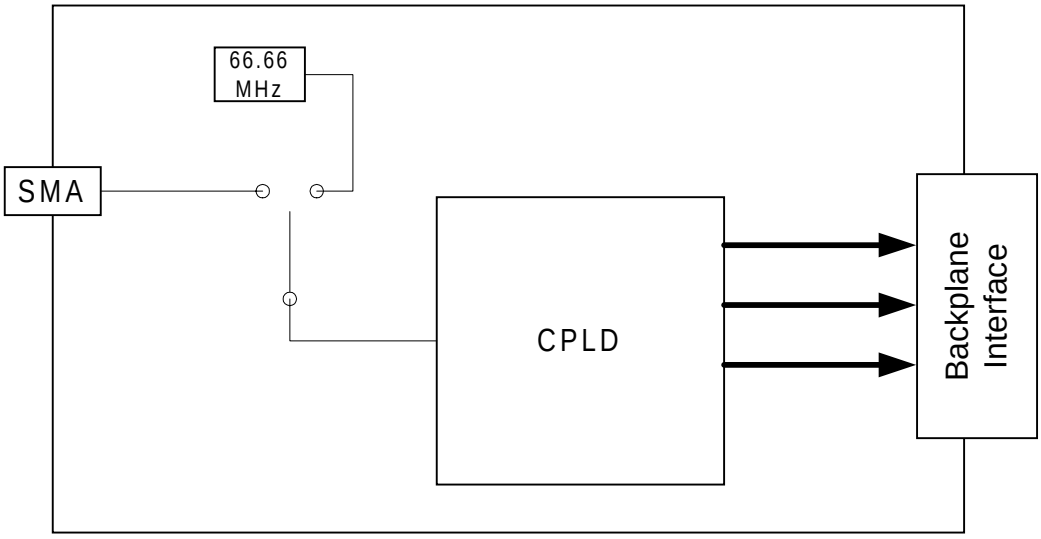
5.4 SPort Card reference designs, PMC-980585

The SPort Card reference design (PMC-980585) is used as a 4xOC-3 rate port card. 4 port cards are used, providing a total of 16 OC-3 ports. The SPort Card is 9U in height.

5.5 Timing card

The timing card provides switch fabric timing information to each of the port cards and switch cards. This is a 3U card using an AMP HS3 connector. The reference clock may be sourced from an on-board oscilator or alternately from an external source. Since the card does not require microprocessor access, it does not use a compact PCI slot. Rather, it will be connected only to the custom high speed backplane. A block diagram is shown below in Figure 3.

Figure 3 - Timing Card



5.6 cPCI backplane

The cPCI backplane is an off-the-shelf 3U design to provide microprocessor access to each of the SPort Cards and QSE cards. For this design, the backplane must be eight slots, with a right-hand system slot.

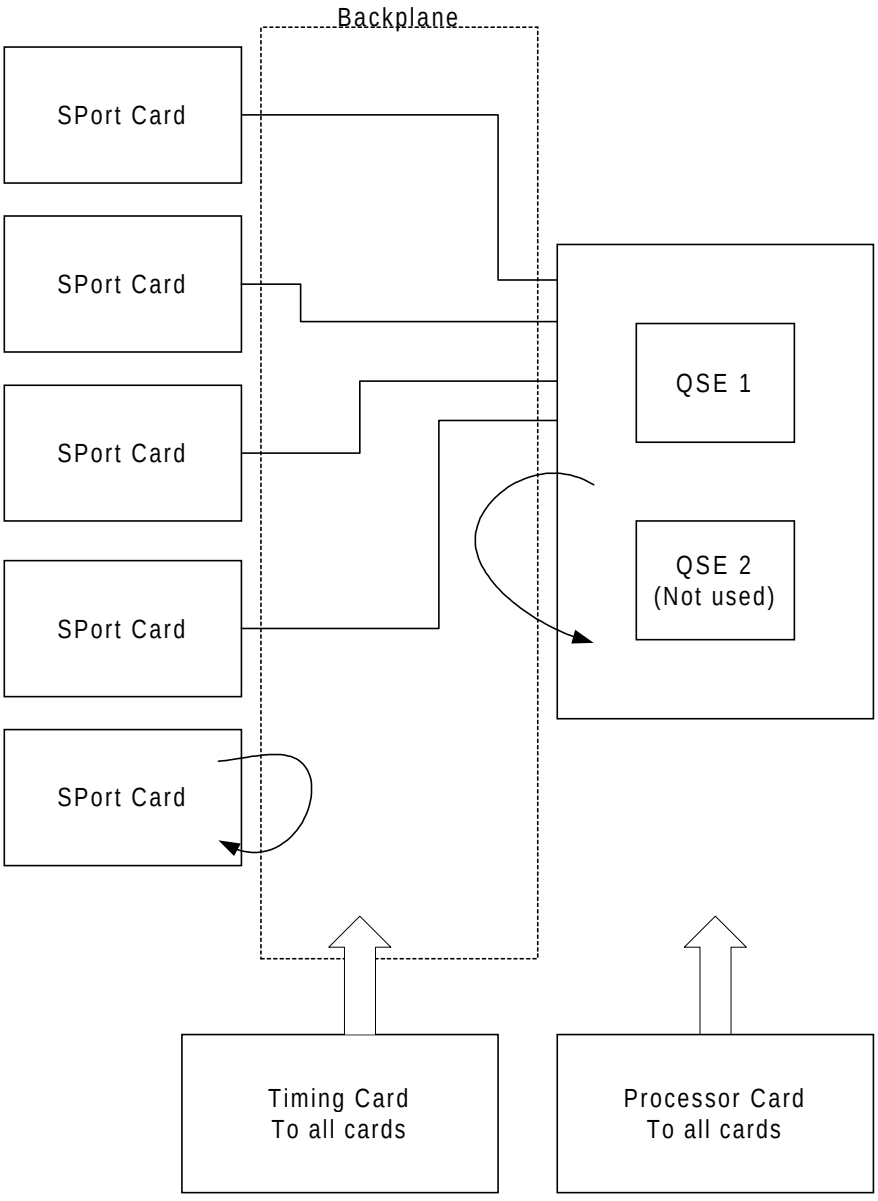
5.7 cPCI Processor Card

A 6U cPCI Intel-based processor card is an off-the-shelf component used to provide software control to each of the SPort Cards and Switch Cards. Because it is 6U, and the subrack is 9U, there is 3U of space above to mount the timing card. The processor card supports multiple operating systems, including VxWorks and Windows 95/NT.

6 IMPLEMENTATION DESCRIPTION

A 5G single stage switch is constructed using 1 QSE reference design and up to 5 SPort Card reference designs, thus using all the available slots. One of the QSEs on the card will not be used in this case. A block diagram of the switch is shown below in Figure 4.

Figure 4 - 5G switch with 16 OC-3 Ports



6.1 Subrack

The subrack was constructed using the bill of materials in Table 1.

Table 1 - Subrack Bill of Materials

No.	Description	Schroff Part No.	Qty.
1	9Ux280mm deep lab side plate	30825-592	2
2	9U 19" Mounting angles	30847-816	2
3	84HP Front Rails with extended lip	30846-465	2
4	84HP Rear Rails for top and bottom	30819-241	2
5	84HP Centre rear rail.	30825-356	2
6	20HP Centre rail for guide rail mounting	30825-082	2
7	Vertical splitter for 9U	30897-203	1
8	Screw kit for securing rails to splitters	21100-575	1 pkg
9	Screw kit for securing splitters	21100-148	1 pkg
10	Screw kit for securing rails to sideplates	21100-457	1 pkg
11	Screw kit for securing 19" mounting angles	21100-739	1 pkg
12	Guides for 160mm boards	60817-103	16
13	Threaded Inserts 84HP	30819-594	8
14	Insulating strips for backplane mounting	60817-061	4

6.2 Custom High speed backplane

The schematics for the high speed backplane are included in Appendix A for reference.

6.2.1 Sheet 1, Root Drawing

This sheet shows the top-level inconnection between each of the SPort Card reference designs with the QSE reference design and the timing card. This backplane forms a single stage fabric using only one of the QSEs on the QSE

reference design. Unused ports on the QSE reference design are looped back on themselves. Slot 6 provides external loopback for the SPort Card.

6.2.2 Sheets 2 – 6, SPort Card

Each of these sheets is identical, and reflects the interface to the SPort Card reference design. Refer to PMC-980583 for more information on this interface.

6.2.3 Sheet 7, Power supply

J17 provides power to the backplane. The SPort Cards and QSE Cards both have the ability to source analog power through the backplane. Additionally, the timing card (slot 0) must be powered through this connector. Terminal 1 is for analog power (if required) and should be connected to 3.3V. Terminal 2 is for power to the timing card and should be connected to 3.3V. Terminal 4 should be connected to ground.

6.2.4 Sheets 8 & 9, QSE Card

These sheets make up the interface to the QSE reference design. Refer to PMC-981288 for more information on this interface.

6.2.5 Sheet 10, Timing Card Interface

This sheet shows the interface to the timing card. Refer to section 6.3 for more information on this interface.

6.2.6 Backplane Bill of Materials

Table 2 - Backplane Bill of Materials

No.	Description	Manufacturer/Part No.	Ref Des	Qty
1	6 row HS3 connector Male vertical	AMP 97-8522-25	J1-J16	16
2	10µF tantalum Capacitor, 6.3V	DIGI-KEY PCS1106CT-ND	C1, C2	2
3	Surface mount fuse, 3A	DIGIKEY F1228CT-ND	F1	1
4	Green surface mount LED	NEWARK -- 95F9373	U1, U2	2
5	300 Ω resistor, 5%, 805		R1, R2	2

6.3 Timing Card

The schematics for the timing card are included in Appendix B for reference.

6.3.1 Sheet 1, Timing Root Drawing

This sheet provides an overview of the design. The general layout of the main blocks and interfacing signals are shown on this sheet. The design is divided into three sections: CPLD, RoboClocks, and Backplane Interface. They are described in the sections that follow.

6.3.2 Sheet 2, CPLD

A low voltage, 100-pin, CPLD is used to generate nine CELL_START (RX_CELL_START) signals, six CELL_24_START signals, and 24 RoboClock control signals.

All CELL_START and CELL_24_START signals are connected to two input/output pins of the CPLD. This increases the output drive current for each signal and utilization of the CPLD. The VCCIO power pins are connected to 3.3V giving the output drivers 3.3V operation.

The CPLD serves two functions. The first function is to supply CELL_START and CELL_24_START signals. One 66.66 MHz clock signal is taken from RoboClock U3 and is connected to the global clock pin of the CPLD. This clock is then connected to an 8-bit counter with an enable. The enable is connected to Vcc, thus making the counter increment on every clock pulse. Three AND gates are

used to determine when the counter reaches 117. Once 117 has been reached, a logic one is sent to a D flip-flop which uses the same timing as the counter. This allows a logic one to remain for one clock pulse. The 8-bit counter is reset to zero when its output reaches 117. The result of this is a CELL_START signal that becomes high on the rising edge of every 118th cycle of SE_CLK. A 4-bit counter with enable is used to count each CELL_START signal. When the 8-bit counter reaches 117, it enables the 4-bit counter to increment once. A 4-bit AND gate is used to determine when the 4-bit counter reaches 4. At this point, a logic one is outputted and the counter is reset on the next clock pulse. The result is a CELL_24_START signal that goes high every four CELL_START pulses and remains high for one clock cycle.

The second purpose of the CPLD is for control of the RoboClocks. Nine switches are connected to the CPLD as input for configuring the RoboClocks. The first four switches can be used to select one output pair. The value of both pins in this pair is denoted by the configuration of the next four switches. The last switch is used as an enable switch to change the values of the selected output pins. This is done by first loading the switches into three registers. These registers are clocked on the global clock signal. The first four switches are connected to the load lines of each register and the next four switches are connected to the data lines of each register. The last switch is connected to the set line of each register. All three registers contain four 5-input AND gates that determine what output pair (if any) is to be changed. If a proper pair is selected and set is high, then the data lines are loaded into four D flip-flops. The output of the D flip-flops are connected to tri-state output buffers, which allows the output to be either low, high, or high impedance.

JTAG pins are connected to a right angle header located on the faceplate.

6.3.3 Sheet 3, RoboClocks

Three Cypress CY7B991V low voltage programmable skew clock buffers are used to buffer and drive nine SE_CLK signals.

The reference clock to the first RoboClock can be supplied from either a local 66.66 MHz crystal oscillator or an external clock source. An external source may be connected to the right angle SMA located on the faceplate. The output of the SMA is balanced with a BALUN transformer. A dual differential LVPECL to TTL translator is then used to convert the signal to TTL logic. A jumper must be used to connect pins two and three of header J3 if using an external clock, otherwise pins one and two must be connected.

Nine switches located on the faceplate can be used to vary the skew of each SE_CLK signal. The switches are coded to allow one input pair of a RoboClock

to be changed at a time. Decoding the switches is done by the CPLD. The first four switches are used to select which RoboClock and pair to modify. See Table 3for the configuration of the first two switches (switch 0 and switch 1).

Table 3 - RoboClock Select

Switch 01	Description
00	Last RoboClock (U4)
01	Middle RoboClock (U2)
10	First RoboClock (U3)
11	Not Used

Once the RoboClock has been selected, the pair that requires modification must be selected. Each RoboClock contains four input pairs. See Table 4 for the configuration of the next two switches (switch 2 and switch 3).

Table 4 - Pair Select

Switch 23	Selected Pair
00	1F0, 1F1
01	2F0, 2F1
10	3F0, 3F1
11	4F0, 4F1

After the RoboClock and pair have been selected, the value of the pair can be set. Each function input is tri-state. In each pair, there is a XF0 pin and a XF1 pin where X stands for either 1, 2, 3, or 4 depending on the pair that was selected. Switch 4 and switch 5 control the value of the XF1 pin in the pair. If switch 4 = switch 5 = 0, then XF1 is LOW. If switch 4 = 0 (or 1) and switch 5 = 1 then the XF1 pin is MID (high impedance). And finally, if switch 4 = 1 and switch 5 = 0 then the XF1 pin is HIGH. A similar configuration follows for switch 6 and switch 7, which control pin XF0. Switch eight must be asserted for at least one clock pulse to load the value into the selected pair.

The input configuration of each pair determines the amount of skew the corresponding output pair will have with respect to the reference clock.

Table 5 - Programmable Skew Configurations

1F1, 2F1, 3F1, 4F1	1F0, 2F0, 3F0, 4F0	1Q0, 1Q1, 2Q0, 2Q1 (ns)	3Q0, 3Q1 (ns)	4Q0, 4Q1 (ns)
LOW	LOW	$-4t_U$	Divide by 2	Divide by 2
LOW	MID	$-3t_U$	$-6t_U$	$-6t_U$
LOW	HIGH	$-2t_U$	$-4t_U$	$-4t_U$
MID	LOW	$-1t_U$	$-2t_U$	$-2t_U$
MID	MID	$0t_U$	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+2t_U$	$+2t_U$
HIGH	LOW	$+2t_U$	$+4t_U$	$+4t_U$
HIGH	MID	$+3t_U$	$+6t_U$	$+6t_U$
HIGH	HIGH	$+4t_U$	Divide by 4	Inverted

Notes on Programmable Skew Configurations:

1. t_U can be calculated by the following formula $t_U = 1/(16f_{NOM})$

2. f_{NOM} is the operating frequency between 40MHz and 66.67MHz. Using a 66.66MHz clock, is approximately 0.94 ns.

When using the local 66.66 MHz crystal oscillator as the reference clock to RoboClock U3, both input pins 3F0 and 3F1 must equal MID. This allows all other output pins to run at the required frequency of 66.66 MHz. 2Q0 and 2Q1 provides the reference clock for the middle RoboClock and the last RoboClock respectively. Adjusting input pins 2F0 and 2F1 on the first RoboClock will skew all output signals from the middle and the last RoboClocks equally. Adjusting input pins 1F0 and 1F1 on the first RoboClock will affect all CELL_START and CELL_24_START signals equally.

6.3.4 Sheet 4, Backplane Interface

The backplane interface is a HS3 6 x 10 right angle connector. Nine SE_CLK, nine CELL_START and six CELL_24_START signals are delivered through the connector. Six 3.3V power pins are supplied from the backplane to the board.

Table 6 - Backplane Interface Connector

Pin Name	Type	Pin No.	Function
SE_CLK_1	Output	A1	*Switch Element Clock* is the 66.66 MHz switch fabric clock for the QSE and QRT.
SE_CLK_2		A2	
SE_CLK_3		A3	
SE_CLK_4		A4	
SE_CLK_5		A5	
SE_CLK_6		A6	
SE_CLK_7		A7	
SE_CLK_8		A8	
SE_CLK_9		A9	
CELL_START_1	Output	A10	*Cell Start* indicates the SOC for the QSE and QRT. It is driven high every cell time (118 SE_CLKs) and remains high for 1 clock cycle.
CELL_START_2		C1	
CELL_START_3		C2	
CELL_START_4		C3	
CELL_START_5		C4	
CELL_START_6		C5	
CELL_START_7		C6	
CELL_START_8		C7	
CELL_START_9		C8	

Pin Name	Type	Pin No.	Function
C24S_1 C24S_2 C24S_3 C24S_4 C24S_5 C24S_6	Output	C9 C10 E1 E2 E3 E4	*Cell 24 Start* indicates the 4th cell time. It is driven high every 4 CELL_START assertions and follows CELL_START when driven high.
NC	NC	B1 - B10, D1 - D10, F1 - F10	Not Connected
+ 3.3V	Input	E5 - E10	+ 3.3 Volt supply
GND	Input	AB1 - AB10, CD1 - CD10, EF1 - EF10	Ground

6.3.5 Timing Card Bill of Materials

Table 7 - Timing Card Bill of Materials

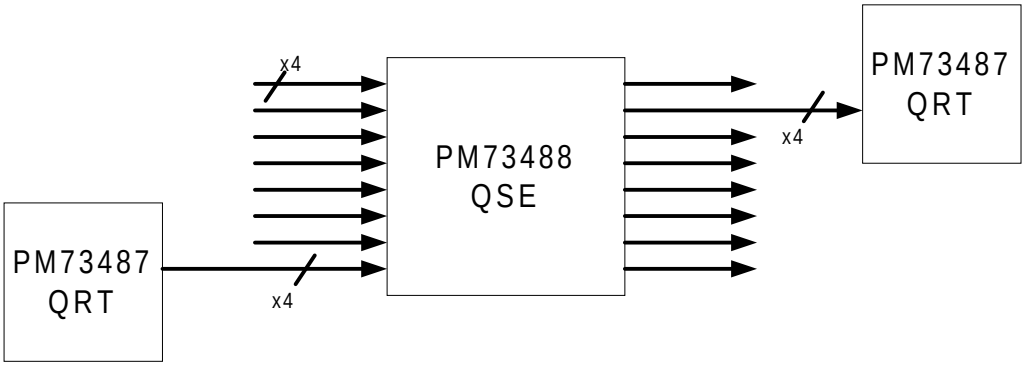
No.	Description	Manufacturer/Part No.	Ref Des	Qty
1	AMP HS3 6x10 Female Right Angle Connector	AMP 97-8522-24	J5	1
2	BALUN Transformer	TOKO 617DB-1024	T1	1
3	Capacitor 0.1uF, 50V, X7R_805	KEMET C0805C104K5RACTR	C1-C6, C8-29	28
4	Capacitor 4.7uF, 6.3V, TANT TE, SMD	Panasonic – ECG ECS-T0JY475R	C7, C30	2
5	Low Voltage Programmable Skew Clock Buffer	Cypress CY7B991V-5JC	U2-U4	3
6	Fuse 2A 125V Fast Nano 2 SMF	Littelfuse Inc. R451002	F1	1
7	Header-4	Sullins Electronics Corp. PZC36SAAN	J2	1
8	Switch 10 pos. DIP	Grayhill 78B10S	J1	1
9	Header-3	Sullins Electronics Corp. PZC36SAAN	J3	1
10	LED 5mm Green PCB Right Angle	Lumex Opto/Components Inc. SSF-LXH100MLGD	D1	1
11	Dual Differential PECL to TTL Translator	Motorola Semiconductor MC100ELT23	U1	1
12	Oscillator 66.6667MHz, HCMOS, 8-PIN, 3.3V	MMD Components MB3100H-66.6667MHz	Y1	1
13	Resistor 1.0 Ohm, 1/8W, 5%, 1206, SMD	Panasonic – ECG ERJ-8RQJ1R0V	R8, R9	2
14	Resistor 1.00k Ohm, 1/10W, 1%, 0805, SMD	Panasonic – ECG ERJ-6ENF1001V	R12	1

No.	Description	Manufacturer/Part No.	Ref Des	Qty
15	Resistor 10.0k Ohm, 1/10W, 1%, 0805, SMD	Panasonic – ECG ERJ-6ENF1002V	R4, R6	2
16	Resistor 100 Ohm, 1/10W, 5%, 0805, SMD	Panasonic – ECG ERJ-6GEYJ101V	R7	1
17	Resistor 20 Ohm, 1/10W, 5%, 0805, SMD	Panasonic – ECG ERJ-6GEYJ200V	R2, R13-R34, R36-R39	27
18	Resistor 20k Ohm, 1/10W, 5%, 0805, SMD	Panasonic – ECG ERJ-6GEYJ203V	R5, R11	2
19	Resistor 25.5 Ohm, 1/10W, 1%, 0805, SMD	Panasonic – ECG ERJ-6ENF25R5V	R3, R10	2
20	Resistor 300 Ohm, 1/10W, 5%, 0805, SMD	Panasonic – ECG ERJ-6GEYJ301V	R1	1
21	Resistor 49.9 Ohm, 1/10W, 1%, 0805, SMD	Panasonic – ECG ERJ-6ENF49R9V	R35	1
22	Resistor Network 10k Ohm, 16pin, 15Res, SMD	CTS Corporation Resistor Products 766161103G	RN1	1
23	SMA PCB Right Angle	Johnson Components, Inc. 142-0701-301	J4	1
24	XC95144XL High Performance CPLD, TQFP100	Xilinx XC95144XL-5TQ100C	U5	1

7 NOTES ON BUILDING LARGE FABRICS

This document showed how to use the QSE reference design and the SPort Card reference design to build a single stage switch with 16 OC-3 ports. The design could easily be scaled to 32 OC-3 ports by simply providing more slots in the backplane. The logical interconnection is shown below in Figure 5. For simplicity, the QRT input and output ports are drawn seperately, though they are in fact part of the same physical device.

Figure 5 - 5G Single Stage Switch



Where larger fabrics are desired, the design practices used to create a 5G switch can be extended to create scalable fabrics up to 40G, 80G, and 160G. Suggested strategies for reaching these rates are detailed in the sections that follow.

7.1 Increase the Number of Cards Per Shelf

A larger number of cards per shelf is recommended. A 19 inch rack is wide enough to house 16 cards quite comfortably, with enough room to spare for processor card, timing card, and power supply.

7.2 Raising the bandwidth of the port cards

The bandwidth of the port cards could be raised to OC-48 rates. The SPort Card is on a 100mm x 9U card. The design practices used on that card could be extended to build a card using 4 OC-12 PHYs, 4 ATLASs, and 4 QRTs. This would significantly reduce the number of slots dedicated to port cards.

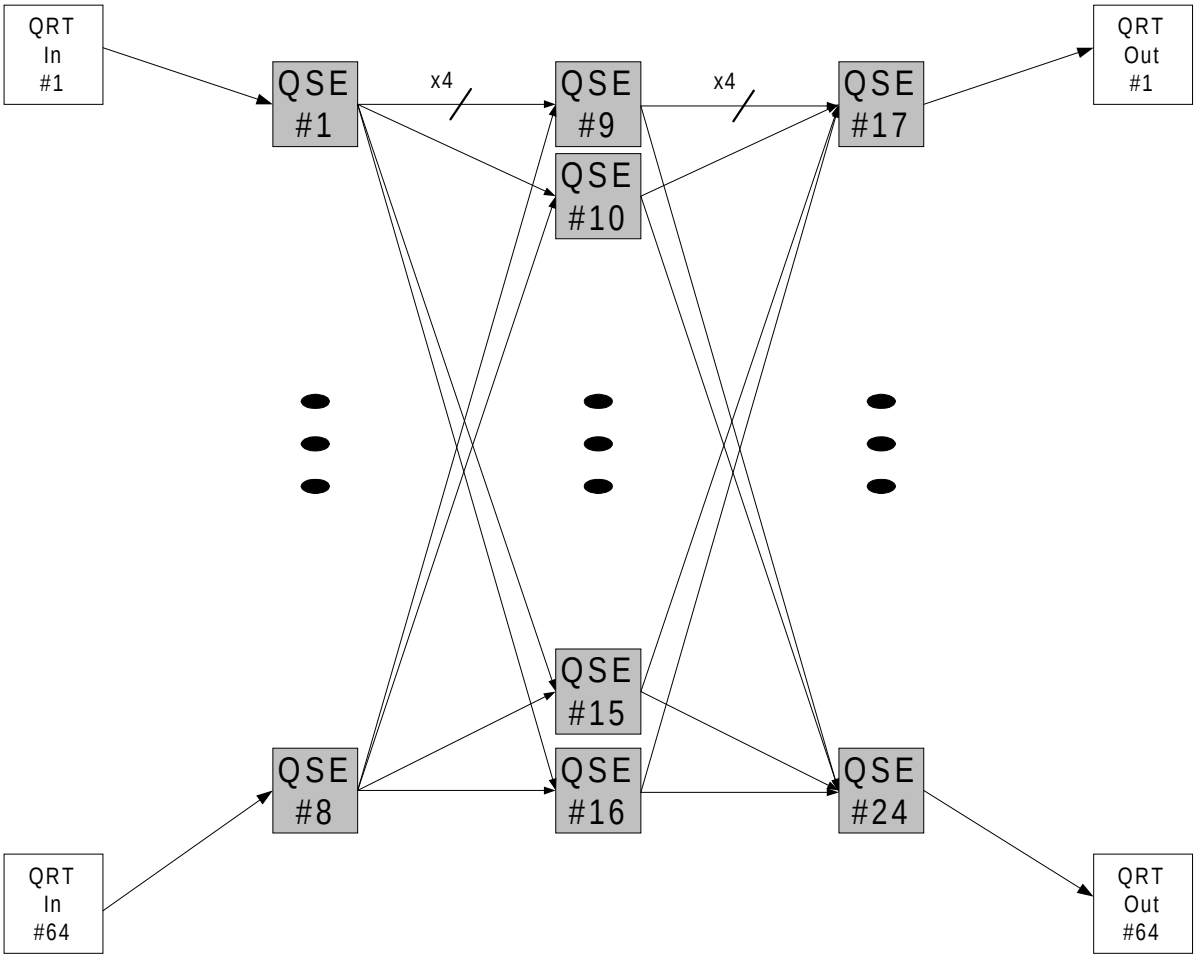
7.3 Beyond a Single Shelf

A good strategy for building multiple shelf designs would be to place all the QSE cards within the same rack. In this way, the most dense interconnection between the QSEs would be contained within the shelf, reducing the interconnect between shelves. The Port cards, having less interconnect to the QSEs, could then be housed in other shelves. The shelves could then be interconnected using a transition card using miniature coax or twinax cables.

7.4 40G Three Stage Switch

A 40G three stage switch can be constructed using 24 QSEs and 64 QRTs. The logical interconnection is illustrated in Figure 6 below.

Figure 6 - 40G Three Stage Switch



Clearly a design such as the one in Figure 6 would require multiple shelves. The number of shelves required depends on the density of the cards. Using the recommendations of section 7.1, we will assume that each shelf can accommodate 16 cards. Using the recommendation of section 7.2, we will assume that each port card has four PM73487 QRT devices. Thus, 64 QRTs could fit onto 16 cards. The 24 PM73488 QSE devices could fit onto 12 cards, assuming two QSEs per card. Since the most dense interconnect is between QSEs, it is recommended that all the switch cards be placed in one shelf, while all the port cards are placed in the second shelf.

Table 8 below describes how each of the switch cards corresponds to QSEs in Figure 6. Table 9 describes how each of the port cards corresponds to QRTs in Figure 6.

Table 8 - Switch Cards

Switch Card Number	QSE#s (From Figure 6)
1	#9, #10
2	#11, #12
3	#13, #14
4	#15, #16
5	#1, #17
6	#2, #18
7	#3, #19
8	#4, #20
9	#5, #21
10	#6, #22
11	#7, #23
12	#8, #24

Table 9 - Port Cards

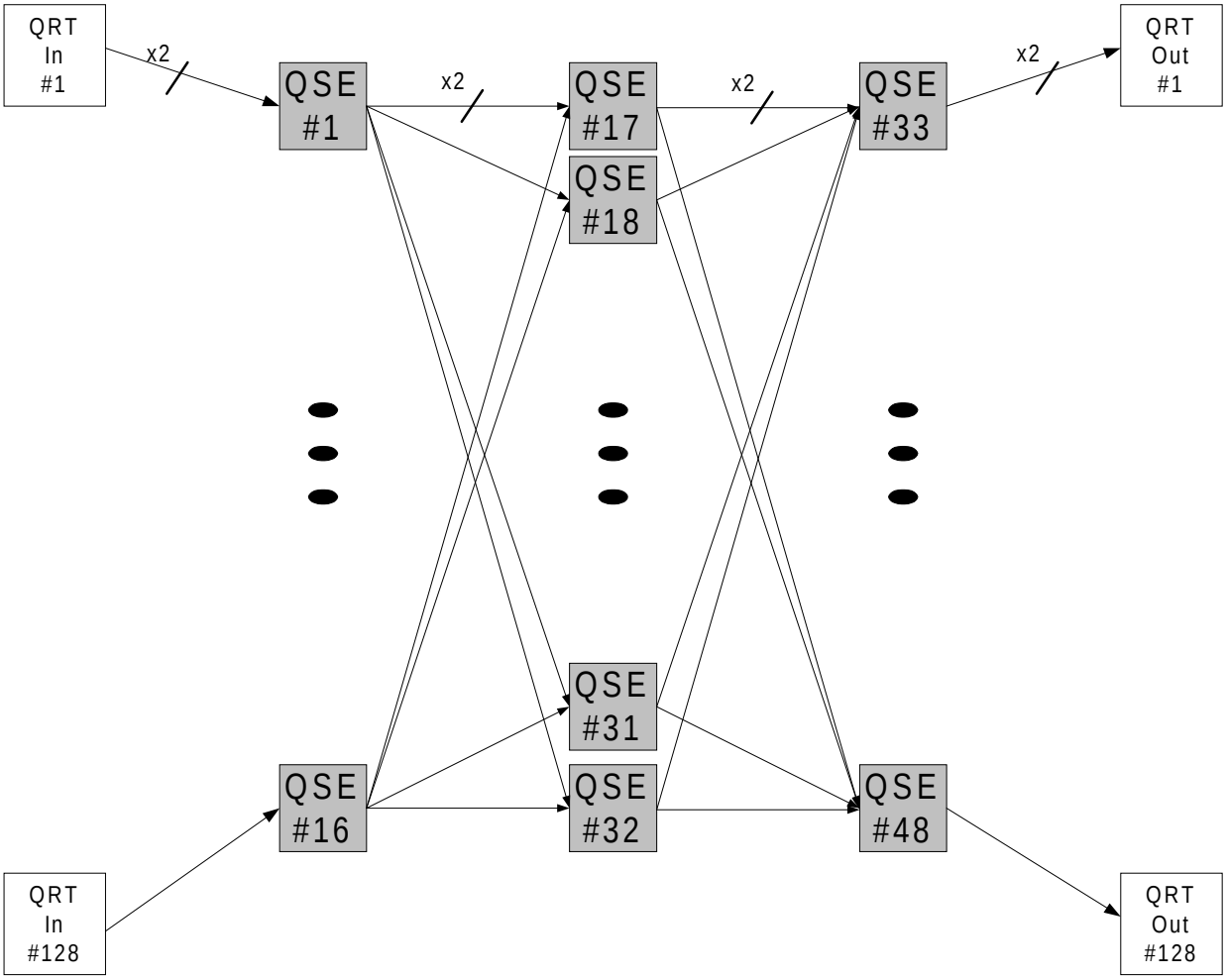
Port Card Number	QRT#s (from Figure 6)	Connects to switch card number
1	#1 - #4	#5
2	#5 - #8	#5
3	#9 - #12	#6
4	#13 - #16	#6
5	#17 - #20	#7
6	#21 - #24	#7
7	#25 - #28	#8
8	#29 - #32	#8
9	#33 - #36	#9
10	#37 - #40	#9
11	#41 - #44	#10
12	#45 - #48	#10
13	#49 - #52	#11
14	#53 - #56	#11
15	#57 - #60	#12
16	#61 - #64	#12

The design is scaleable from 2.5G to 40G, in increments of 2.5G. The initial installation of the switch would use switch cards 1 through 5 and port card 1 to create a 2.5G switch. Additional port cards can be added, with the corresponding switch cards to allow cost linearity in expanding the switch up to its maximum capacity of 40G.

7.5 80G Three Stage Switch

An 80G design can be constructed using 48 QSEs and 128 QRTs in the as described in Figure 7 below. Note that in the figure, QRT/QSE ports are grouped in twos, rather than in fours as was done in previous sections. This requires a change in the backplane serialization strategy, but is required to create an 80G fabric.

Figure 7 - 80G Three Stage Switch



Maintaining the assumptions of section 7.4, the above switch would require 24 switch cards and 32 port cards. Therefore, the entire switch would fit into 4 shelves. The QSEs would be grouped onto cards in the same manner as in section 7.4, as illustrated in below.

Table 10 - Switch Cards

Switch Card Number	QSE#s (from Figure 7)
1	#17, #18
2	#19, #20
3	#21, #22
4	#23, #24
5	#25, #26
6	#27, #28
7	#29, #30
8	#31, #32
9	#1, #33
10	#2, #34
11	#3, #35
12	#4, #36
13	#5, #37
14	#6, #38
15	#7, #39
16	#8, #40
17	#9, #41
18	#10, #42
19	#11, #43
20	#12, #44

Switch Card Number	QSE#s (from Figure 7)
21	#13, #45
22	#14, #46
23	#15, #47
24	#16, #48

Table 11 - Port Cards

Port Card Number	QRT#s (from Figure 7)	Connects to switch card number
1	#1 - #4	9
2	#5 - #8	9
3	#9 - #12	10
4	#13 - #16	10
5	#17 - #20	11
6	#21 - #24	11
7	#25 - #28	12
8	#29 - #32	12
9	#33 - #36	13
10	#37 - #40	13
11	#41 - #44	14
12	#45 - #48	14
13	#49 - #52	15
14	#53 - #56	15

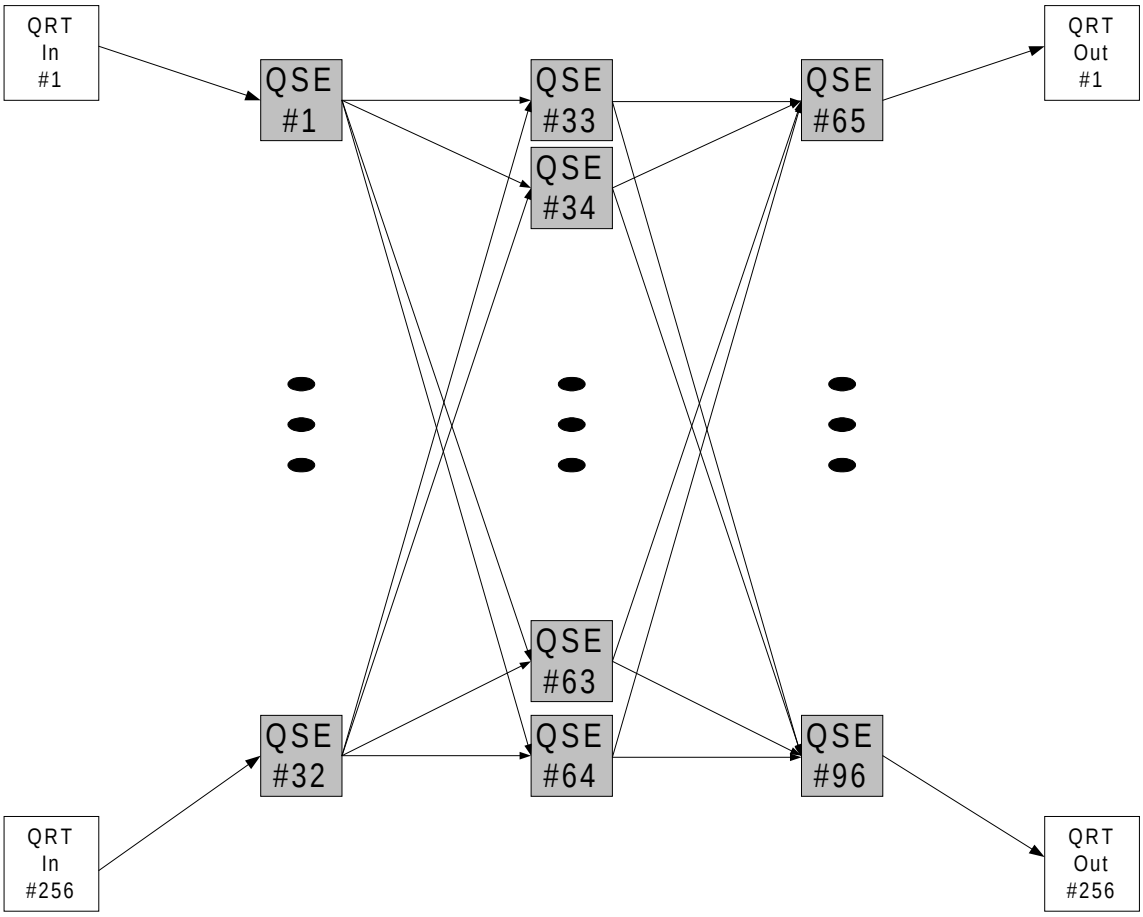
Port Card Number	QRT#s (from Figure 7)	Connects to switch card number
15	#57 - #60	16
16	#61 - #64	16
17	#65 - #68	17
18	#69 - #72	17
19	#73 - #76	18
20	#77 - #80	18
21	#81 - #84	19
22	#85 - #88	19
23	#89 - #92	20
24	#93 - #96	20
25	#97 - #100	21
26	#101 - #104	21
27	#105 - #108	22
28	#109 - #112	22
29	#113 - #116	23
30	#117 - #120	23
31	#121 - #124	24
32	#125 - #128	24

The design is also scaleable from 2.5G to 80G, in increments of 2.5G. The initial installation of the switch would use switch cards 1 through 9 and port card 1 to create a 2.5G switch. Additional port cards can be added, with the corresponding switch cards to allow cost linearity in expanding the switch up to its maximum capacity of 80G.

7.6 160G Three Stage Switch

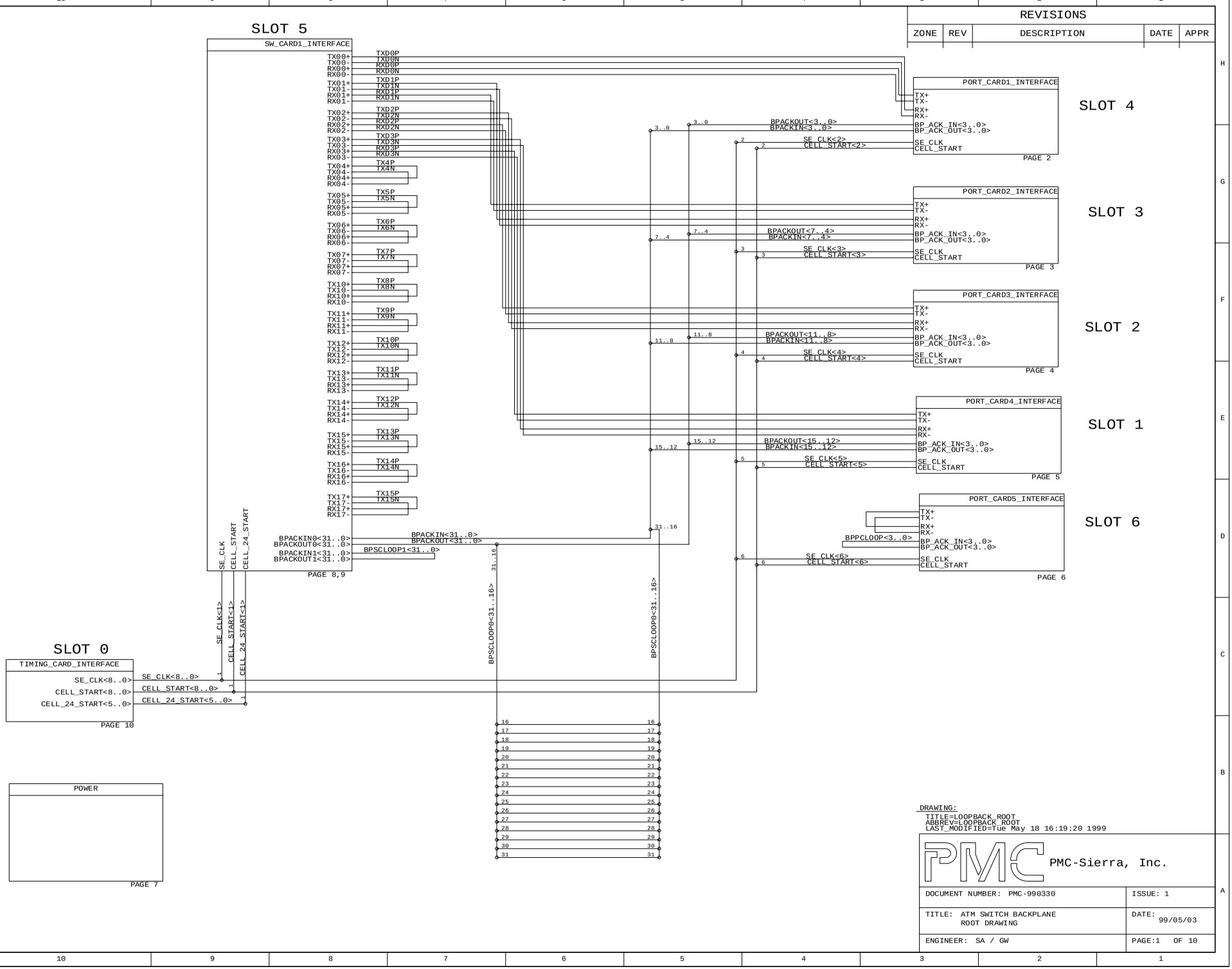
A 160G design can be constructed using 96 QSEs and 256 QRTs in the as described in Figure 7 below. Note that in the figure, QRT/QSE ports are not grouped as was done in previous sections. This requires a change in the backplane serialization strategy, but is required to create a 160G fabric.

Figure 8 - 160G Three Stage Switch



Using the assumptions of the previous section, this switch would require 64 port cards and 48 switch cards, and would occupy 7 shelves.

APPENDIX A: BACKPLANE SCHEMATICS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SW_CARD1_INTERFACE
PAGE 8,9
SLOT 4
PORT_CARD1_INTERFACE
PAGE 2
SLOT 3
PORT_CARD2_INTERFACE
PAGE 3
SLOT 2
PORT_CARD3_INTERFACE
PAGE 4
SLOT 1
PORT_CARD4_INTERFACE
PAGE 5
SLOT 6
PORT_CARD5_INTERFACE
PAGE 6
SLOT 0
TIMING_CARD_INTERFACE
PAGE 10
POWER
PAGE 7
SE_CLK
CELL_START
CELL_24_START
BPACKIN0<31..0>
BPACKOUT0<31..0>
BPACKIN1<31..0>
BPACKOUT1<31..0>
BPSCLOOP1<31..0>
BPACKIN<31..0>
BPACKOUT<31..0>
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BPSCLOOP0<31..16>
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CELL_START<8..0>
CELL_24_START<5..0>
BPACKOUT<3..0>
BPACKIN<3..0>
BPACKOUT<7..4>
BPACKIN<7..4>
BPACKOUT<11..8>
BPACKIN<11..8>
BPACKOUT<15..12>
BPACKIN<15..12>
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SE_CLK
CELL_START
REVISIONS
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REV
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DATE
APPR
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DOCUMENT NUMBER: PMC-990330
ISSUE: 1
TITLE: ATM SWITCH BACKPLANE ROOT DRAWING
DATE: 99/05/03
ENGINEER: SA / GW
PAGE:1 OF 10

SLOT 4 SPORT CARD

REVISIONS				
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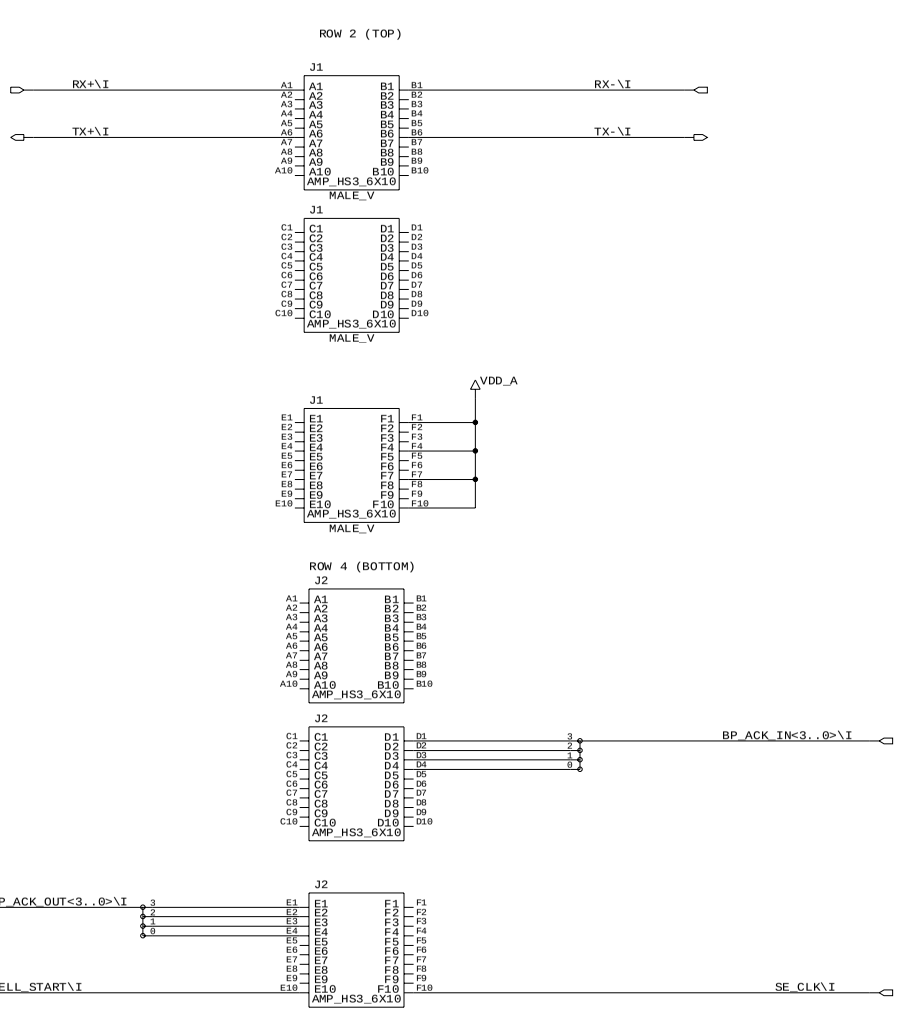
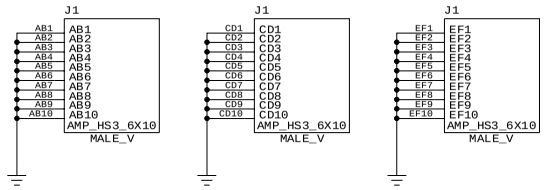
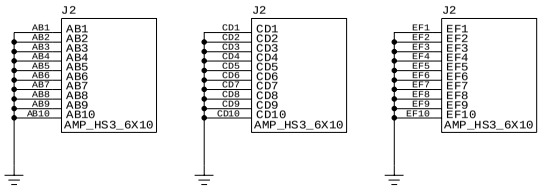




GND PINS FOR HS3 CONNECTORS



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PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990330	ISSUE: 1
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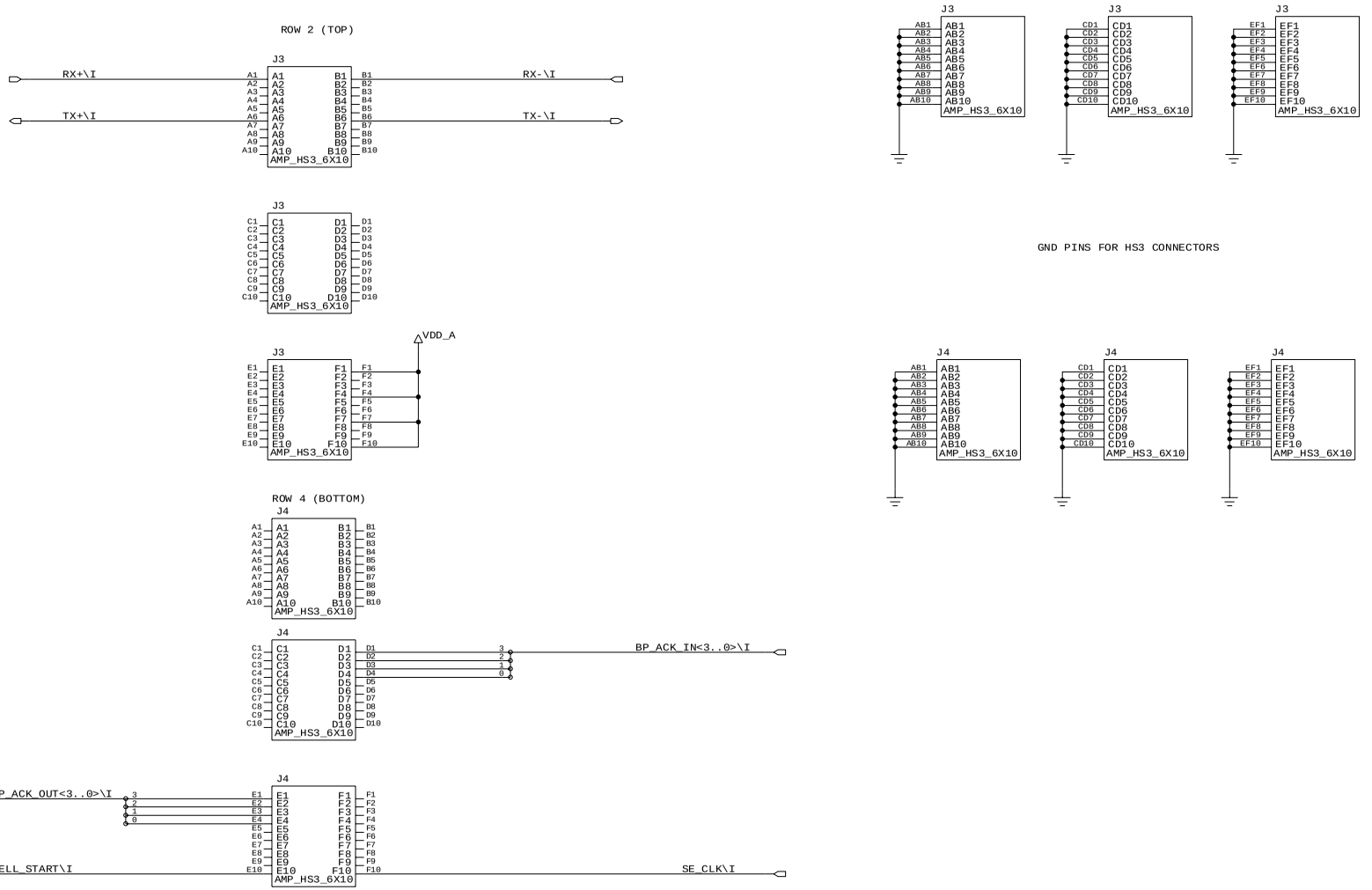
ENGINEER: SA / GW	PAGE:2 OF 10

SLOT 3 SPORT CARD

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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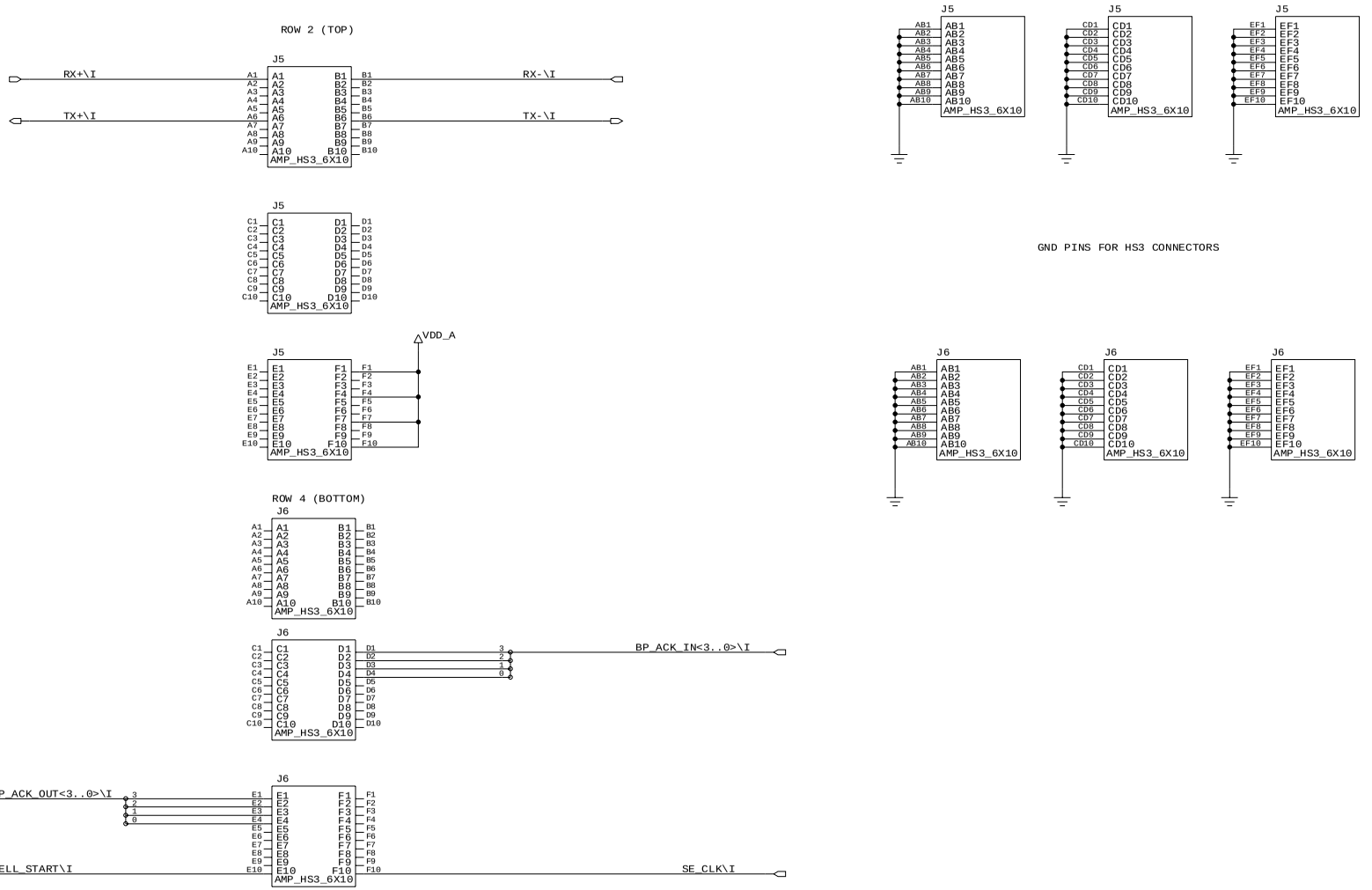
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-980330	ISSUE: 1
TITLE: ATM SWITCH BACKPLANE 1 SPORT CARD SLOT	DATE: 99/05/03
ENGINEER: SA GW	PAGE:3 OF 10

SLOT 2 SPORT CARD

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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PMC-Sierra, Inc.

DOCUMENT NUMBER: 990330	ISSUE: 1
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ENGINEER: SA / GW	PAGE:4 OF 10

SLOT 1 SPORT CARD

REVISIONS				
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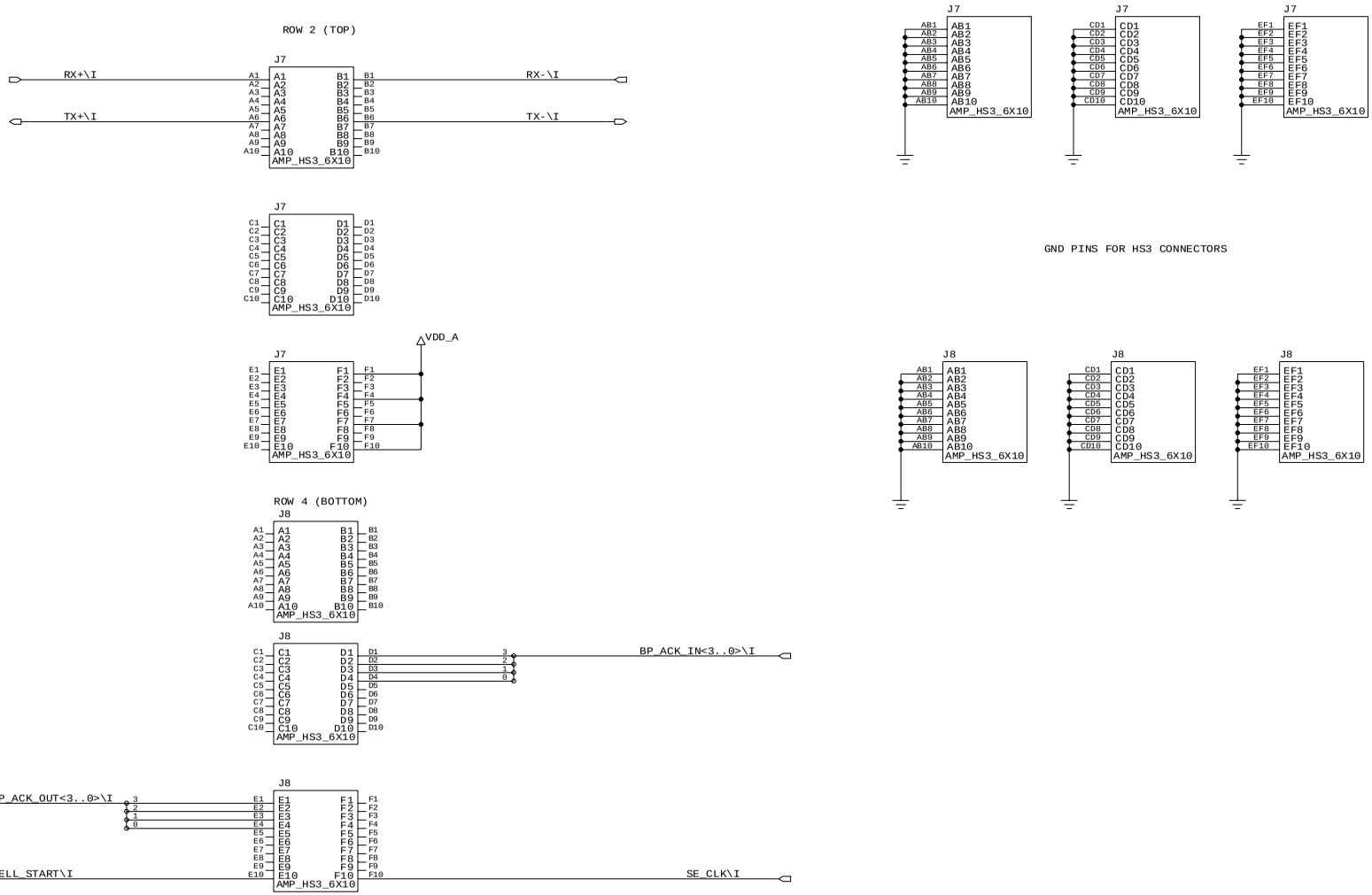

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PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990330	ISSUE: 1
TITLE: ATM SWITCH BACKPLANE 1 SPORT CARD SLOT	DATE: 99/05/03
ENGINEER: SA / GW	PAGE:5 OF 10

SLOT 6 SPORT CARD

REVISIONS				
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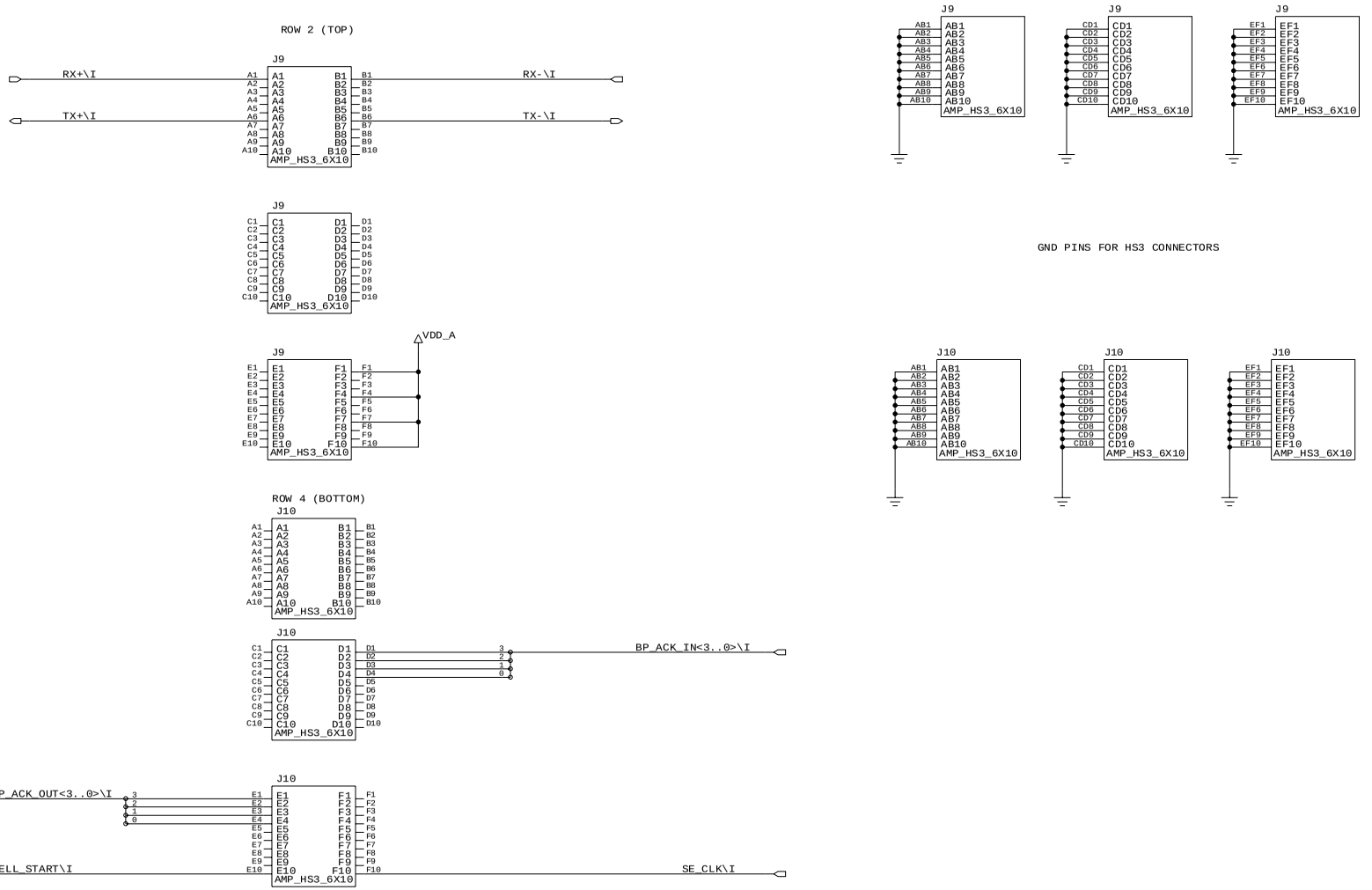

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PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990330	ISSUE: 1
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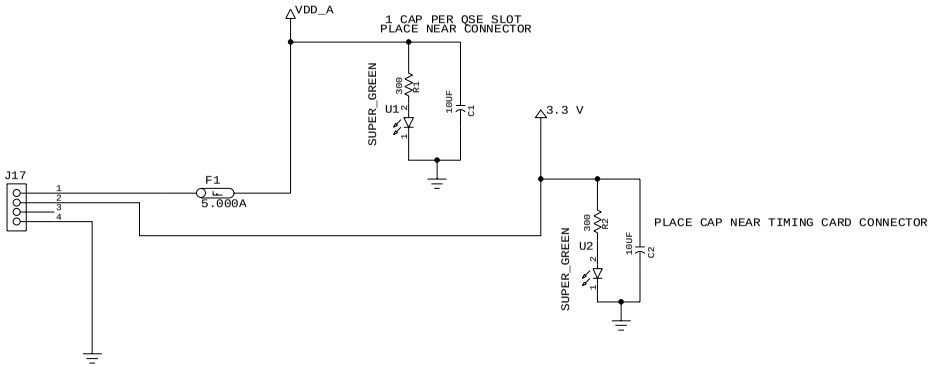
ENGINEER: SA / GW	PAGE:6 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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ENGINEER: SA / GW	PAGE:7 OF 10

SLOT 5 QSE

REVISIONS				
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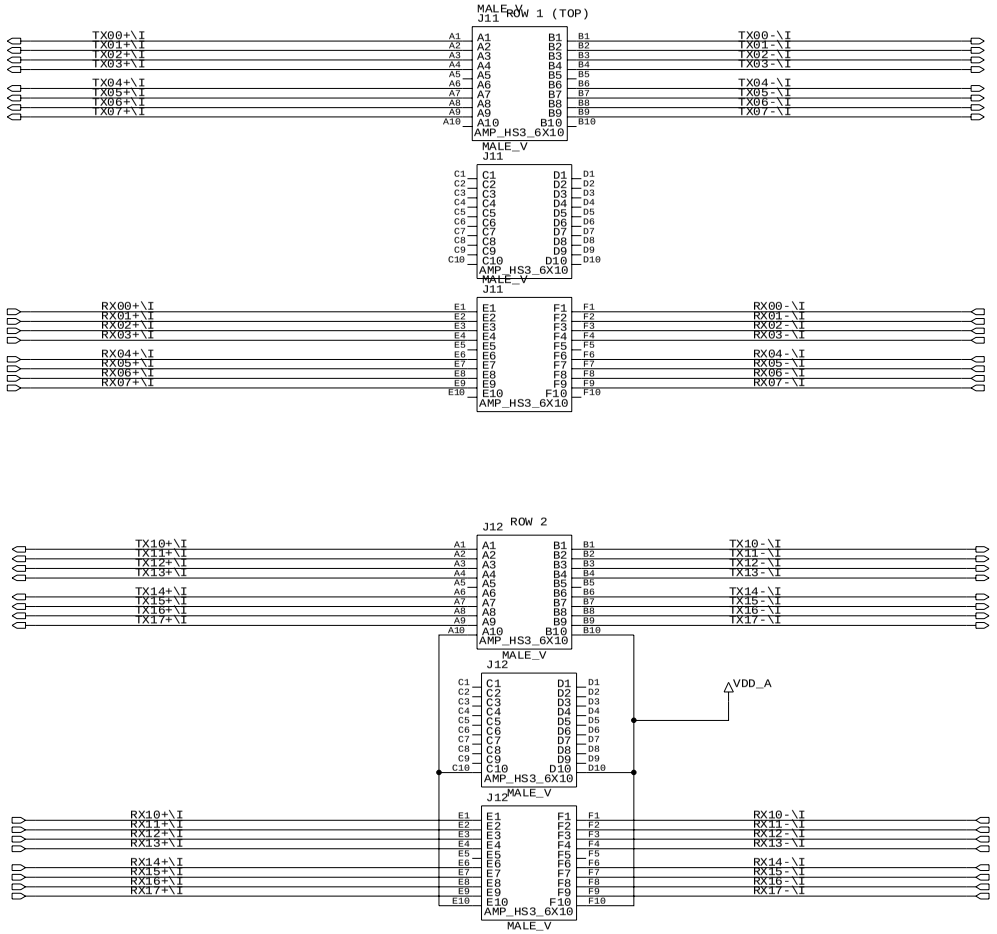

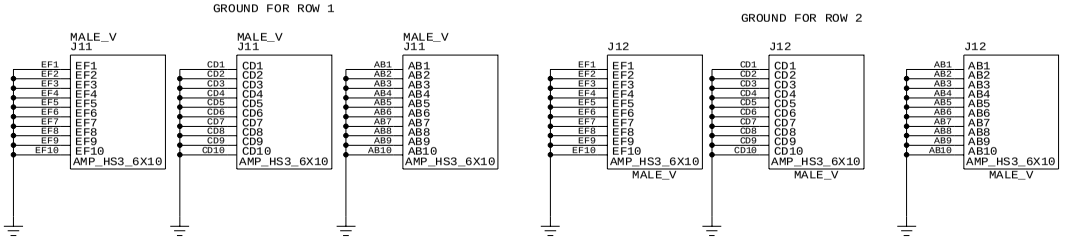

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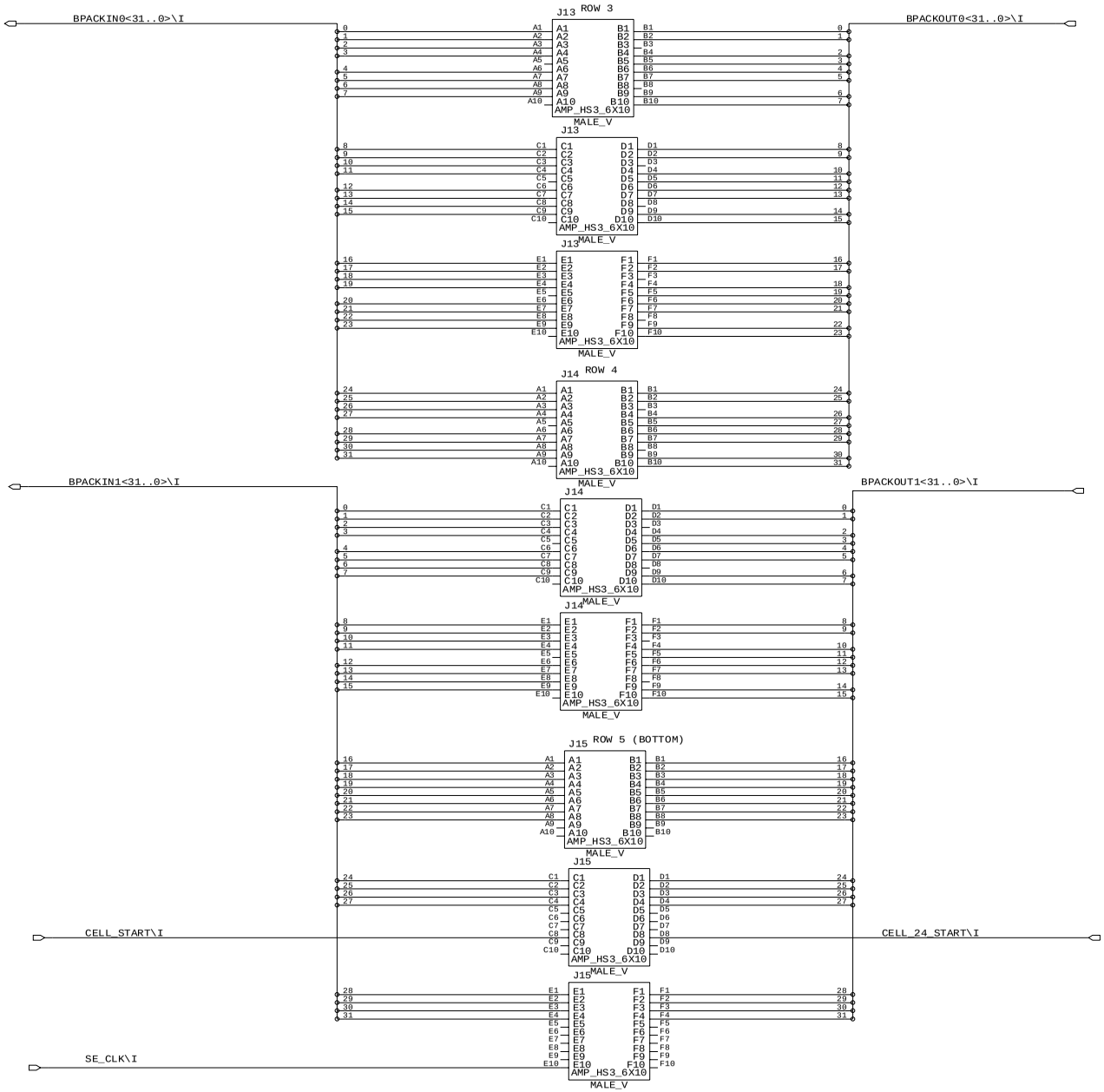
PMC-Sierra, Inc.

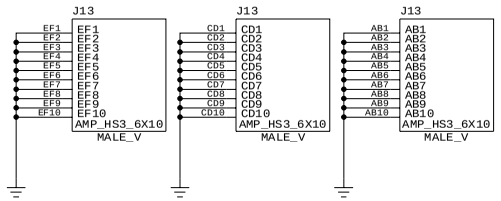
DOCUMENT NUMBER: PMC-990330	ISSUE: 1
TITLE: ATM SWITCH BACKPLANE 1 SWITCH CARD HIGH SPEED	DATE: 99/05/03
ENGINEER: SA / GW	PAGE:8 OF 10

SLOT 5 QSE

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



GROUND FOR ROW 3



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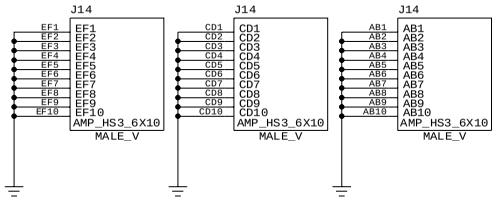

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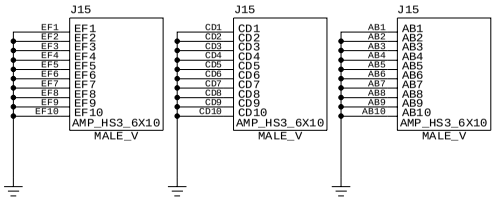
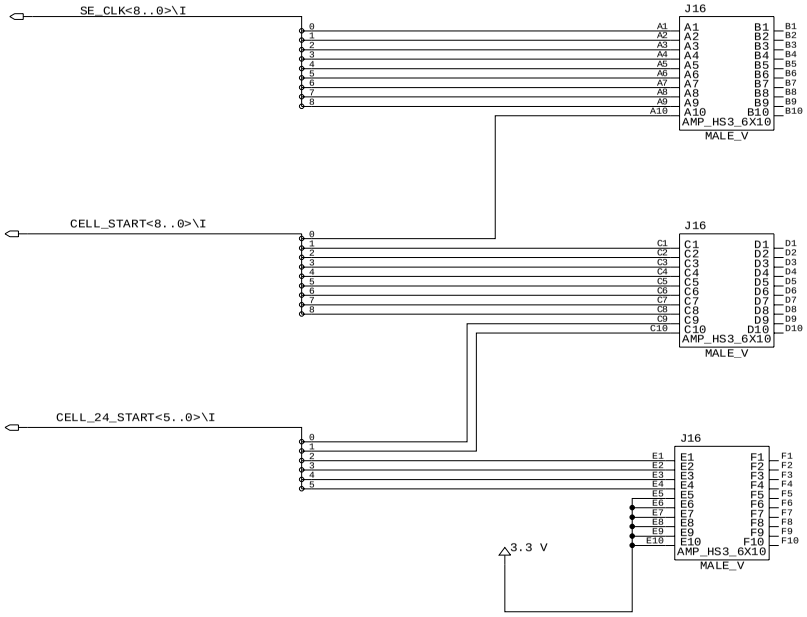


PMC-Sierra, Inc.

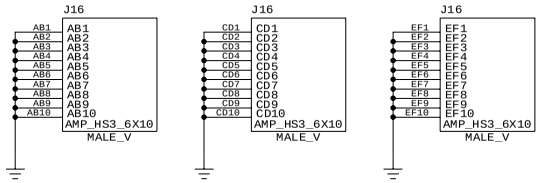
DOCUMENT NUMBER: PMC-990330	ISSUE: 1
TITLE: ATM SWITCH BACKPLANE 1 SWITCH CARD BACKPRESSURE SIGNALS	DATE: 99/05/03
ENGINEER: SA / GW	PAGE:9 OF 10

SLOT 0 TIMING CARD

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



GROUND FOR HS3 CONNECTOR



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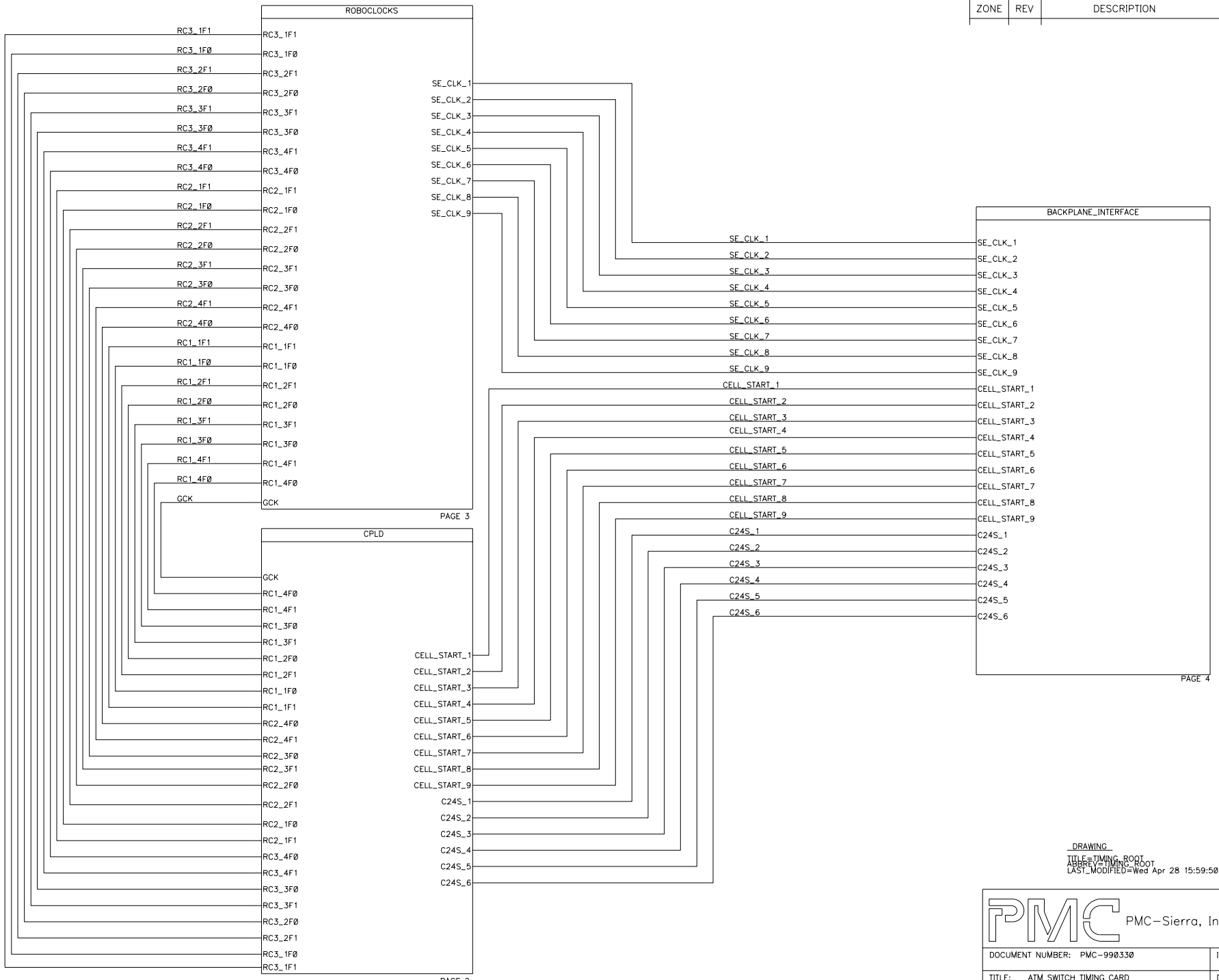
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-980330	ISSUE: 1
TITLE: ATM SWITCH BACKPLANE TIMING CARD INTERFACE	DATE: 99/05/03
ENGINEER: SA / GW	PAGE:10 OF 10

APPENDIX B: TIMING CARD SCHEMATICS

The schematics for the timing card are in two groups; the first is the schematics for the timing card pcb. The second is for the CPLD.



REVISIONS

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PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990330	ISSUE: 1
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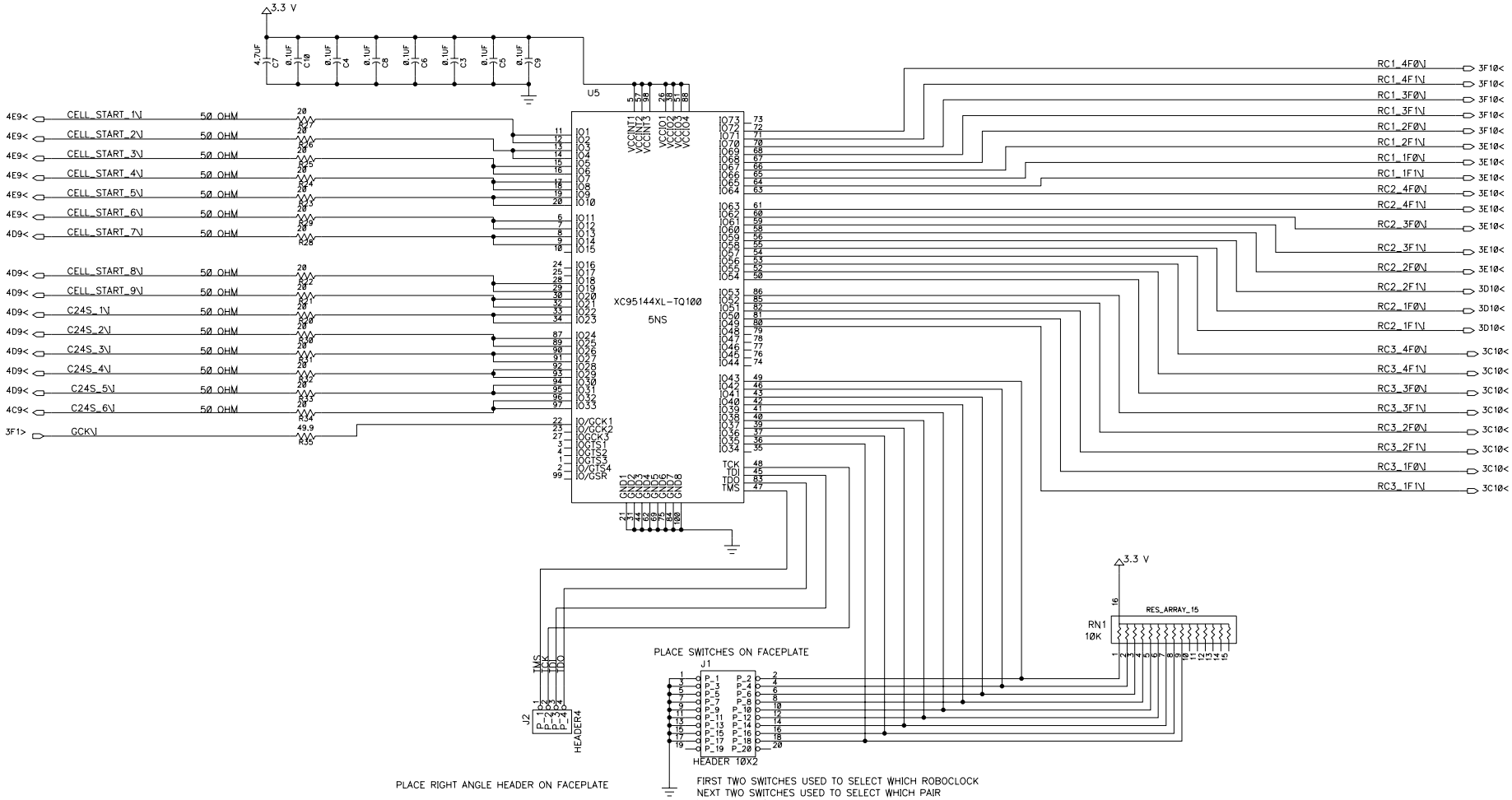
ENGINEER: SA	PAGE: 1 OF 4

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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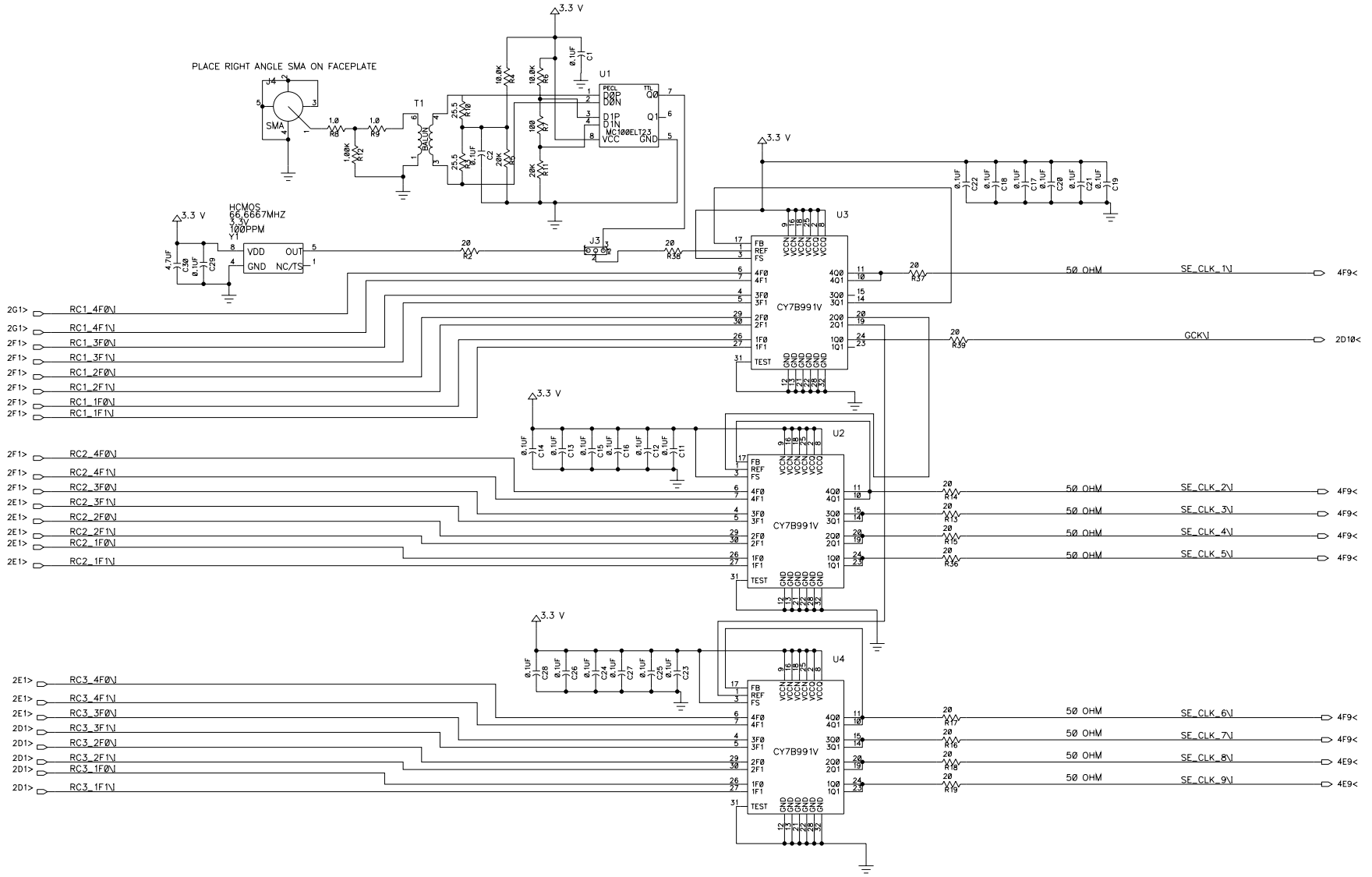
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990330	ISSUE: 1
TITLE: ATM SWITCH TIMING CARD PRELIMINARY	DATE: 99/03/09
ENGINEER: SA	PAGE: 2 OF 4

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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PMC-Sierra, Inc.

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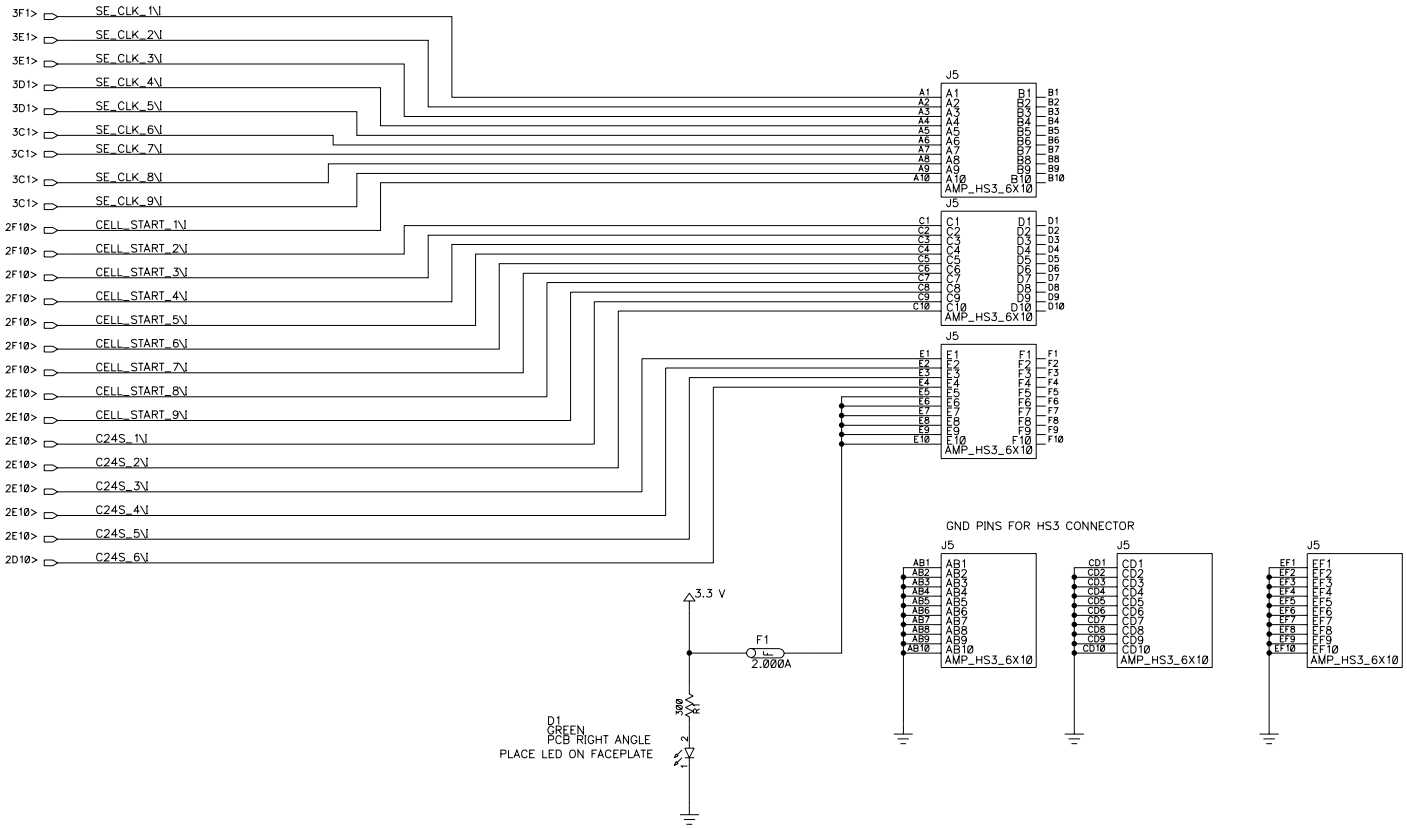
TITLE: ATM SWITCH TIMING CARD PRELIMINARY	DATE: 99/03/09
ENGINEER: SA	PAGE: 3 OF 4

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990330	ISSUE: 1
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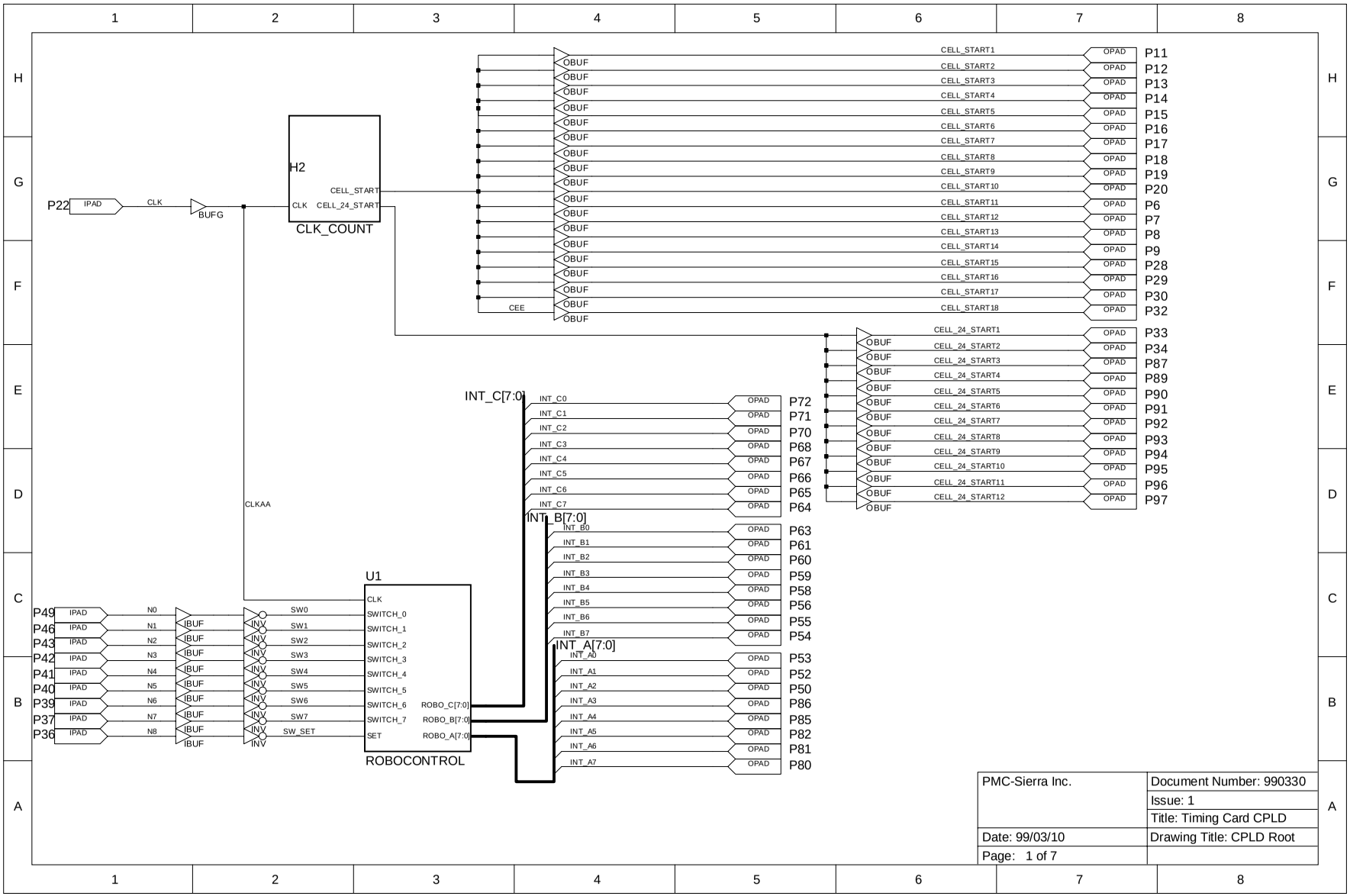
ENGINEER: SA	PAGE: 4 OF 4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CLK
BUFG
H2
CLK
CELL_START
CELL_24_START
CLK_COUNT
CEE
OBUF
CELL_START1
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CELL_START3
CELL_START4
CELL_START5
CELL_START6
CELL_START7
CELL_START8
CELL_START9
CELL_START10
CELL_START11
CELL_START12
CELL_START13
CELL_START14
CELL_START15
CELL_START16
CELL_START17
CELL_START18
OPAD
P11
P12
P13
P14
P15
P16
P17
P18
P19
P20
P6
P7
P8
P9
P28
P29
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P32
CELL_24_START1
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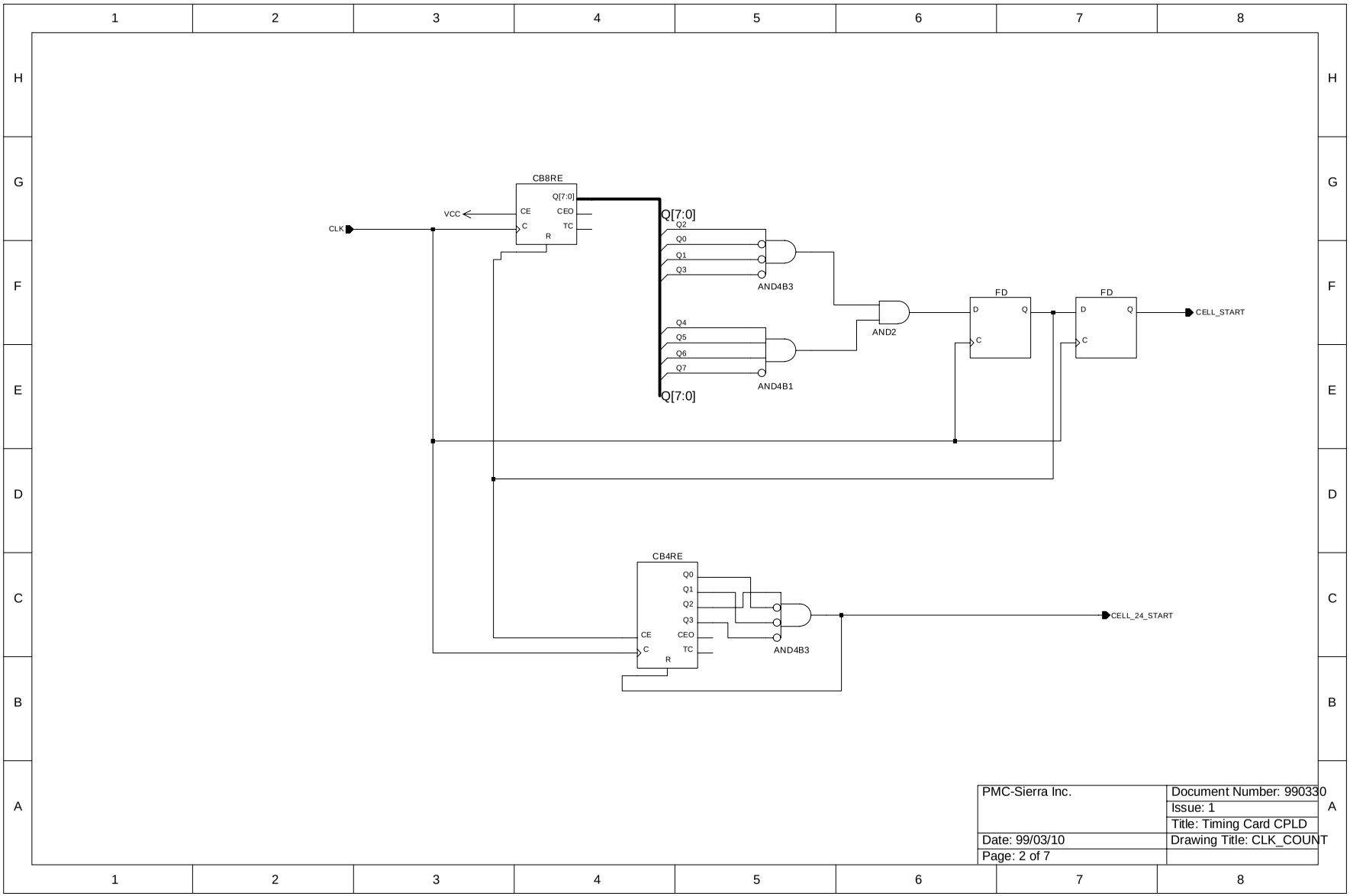
CELL_24_START3
CELL_24_START4
CELL_24_START5
CELL_24_START6
CELL_24_START7
CELL_24_START8
CELL_24_START9
CELL_24_START10
CELL_24_START11
CELL_24_START12
P33
P34
P87
P89
P90
P91
P92
P93
P94
P95
P96
P97
INT_C[7:0]
INT_C0
INT_C1
INT_C2
INT_C3
INT_C4
INT_C5
INT_C6
INT_C7
P72
P71
P70
P68
P67
P66
P65
P64
INT_B[7:0]
INT_B0
INT_B1
INT_B2
INT_B3
INT_B4
INT_B5
INT_B6
INT_B7
P63
P61
P60
P59
P58
P56
P55
P54
INT_A[7:0]
INT_A0
INT_A1
INT_A2
INT_A3
INT_A4
INT_A5
INT_A6
INT_A7
P53
P52
P50
P86
P85
P82
P81
P80
CLKAA
U1
CLK
SWITCH_0
SWITCH_1
SWITCH_2
SWITCH_3
SWITCH_4
SWITCH_5
SWITCH_6
SWITCH_7
SET
ROBO_C[7:0]
ROBO_B[7:0]
ROBO_A[7:0]
ROBOCONTROL
P49
P46
P43
P42
P41
P40
P39
P37
P36
N0
N1
N2
N3
N4
N5
N6
N7
N8
IBUF
INV
SW0
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW_SET
PMC-Sierra Inc.
Document Number: 990330
Issue: 1
Title: Timing Card CPLD
Date: 99/03/10
Drawing Title: CPLD Root
Page: 1 of 7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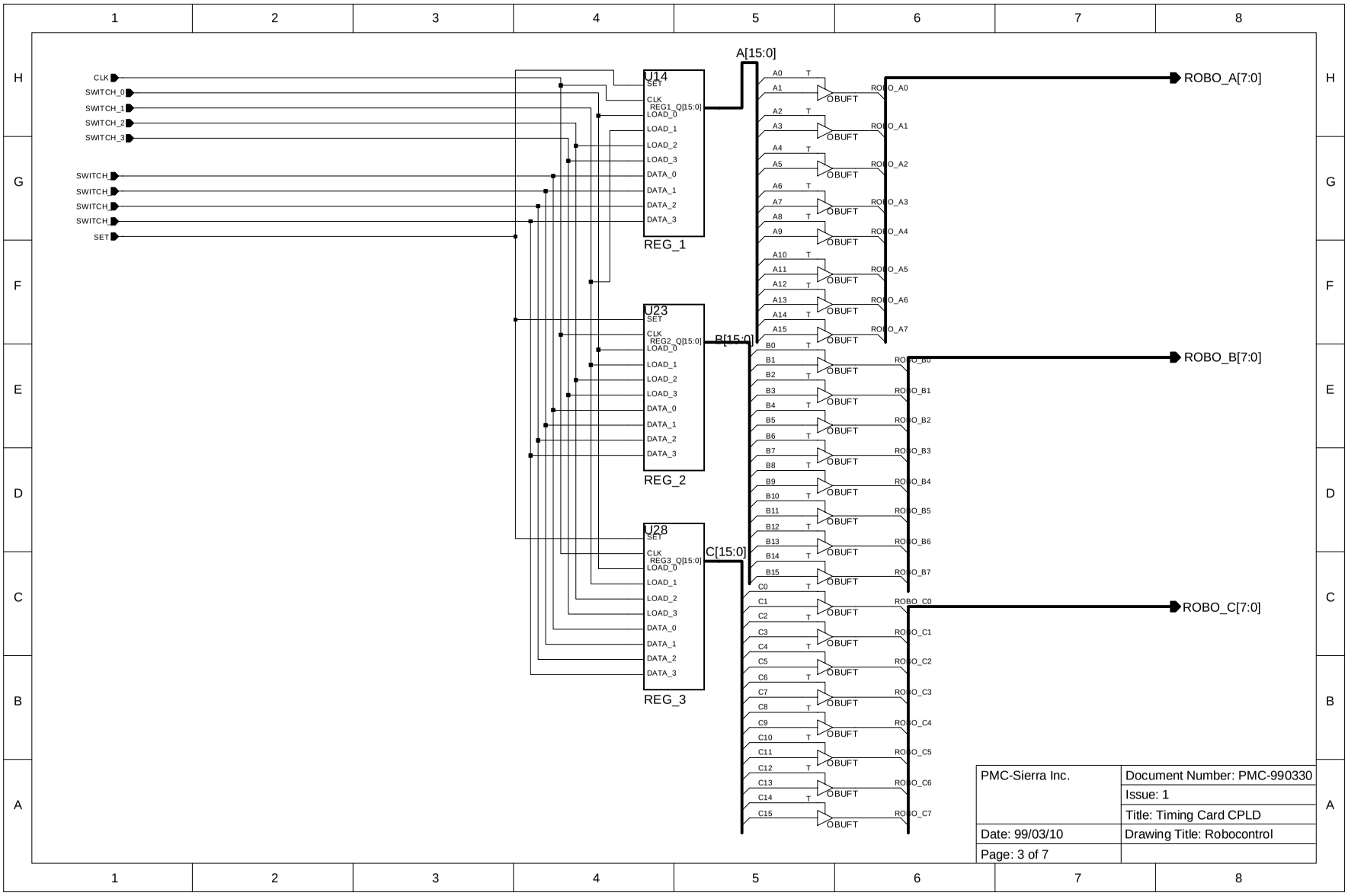
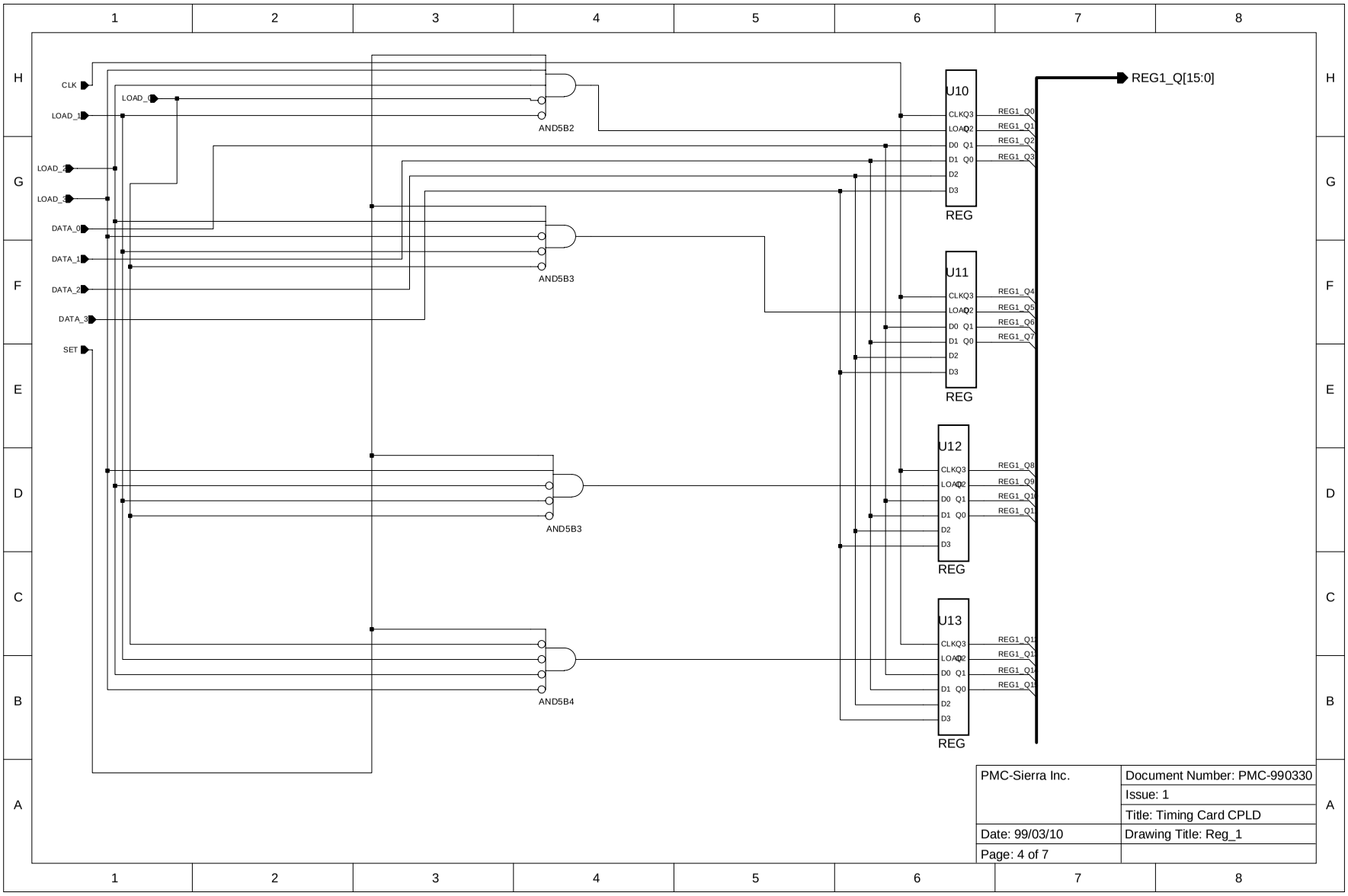
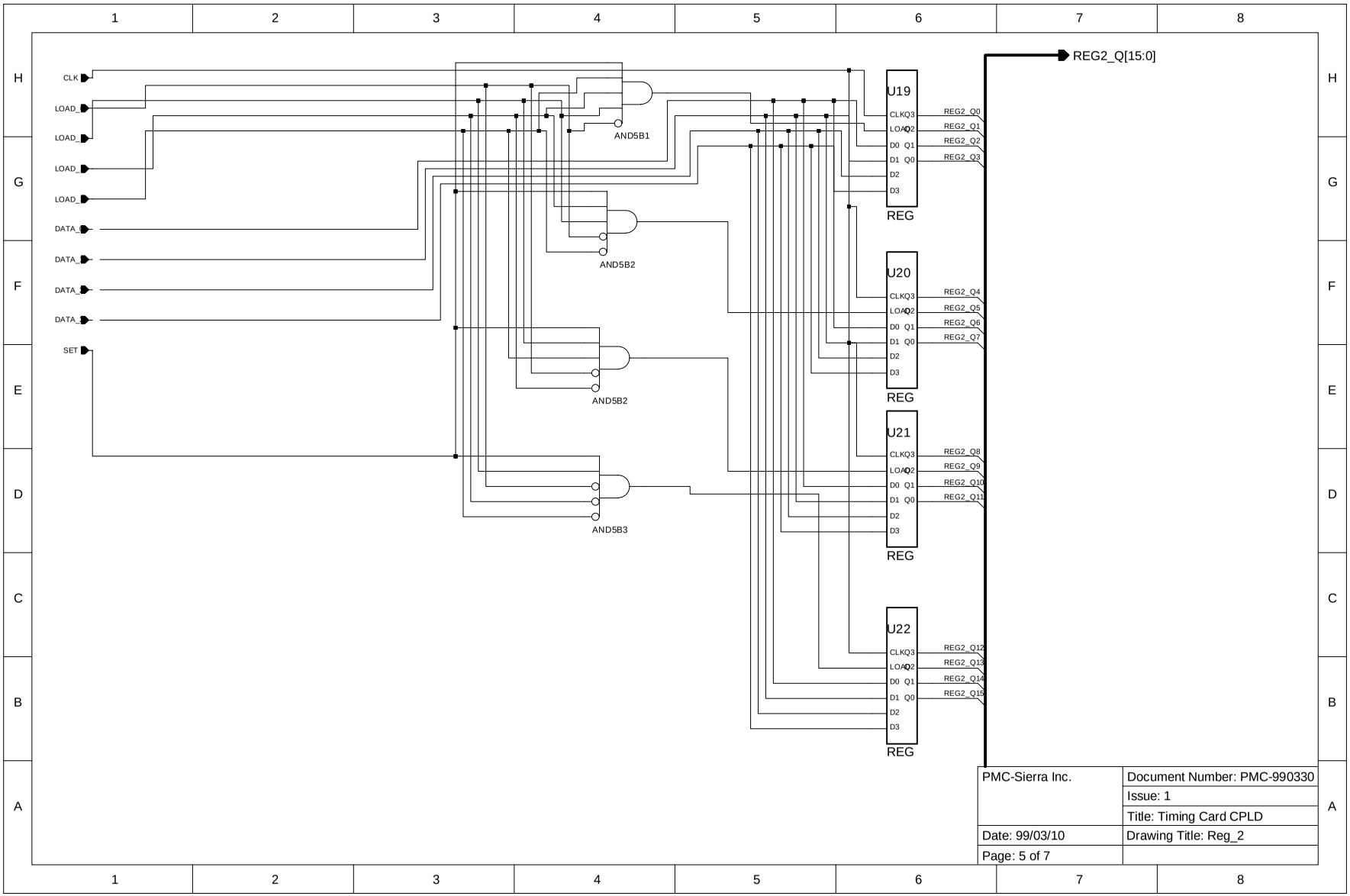
2
3
4
5
6
7
8
H
G
F
E
D
C
B
A
CB8RE
Q[7:0]
CE
CEO
C
TC
R
VCC
CLK
Q[7:0]
Q2
Q0
Q1
Q3
AND4B3
Q4
Q5
Q6
Q7
AND4B1
Q[7:0]
AND2
FD
D
Q
C
FD
D
Q
C
CELL_START
CB4RE
Q0
Q1
Q2
Q3
CE
CEO
C
TC
R
AND4B3
CELL_24_START
PMC-Sierra Inc.
Document Number: 990330
Issue: 1
Title: Timing Card CPLD
Date: 99/03/10
Drawing Title: CLK_COUNT
Page: 2 of 7


1
2
3
4
5
6
7
8
H
G
F
E
D
C
B
A
CLK
SWITCH_0
SWITCH_1
SWITCH_2
SWITCH_3
SWITCH_
SWITCH_
SWITCH_
SWITCH_
SET
U14
U23
U28
SET
CLK
REG1_Q[15:0]
REG2_Q[15:0]
REG3_Q[15:0]
LOAD_0
LOAD_1
LOAD_2
LOAD_3
DATA_0
DATA_1
DATA_2
DATA_3
REG_1
REG_2
REG_3
A[15:0]
B[15:0]
C[15:0]
OBUFT
ROBO_A[7:0]
ROBO_B[7:0]
ROBO_C[7:0]
PMC-Sierra Inc.
Document Number: PMC-990330
Issue: 1
Title: Timing Card CPLD
Date: 99/03/10
Drawing Title: Robocontrol
Page: 3 of 7



PMC-Sierra Inc.	Document Number: PMC-990330
	Issue: 1
	Title: Timing Card CPLD
Date: 99/03/10	Drawing Title: Reg_1
Page: 4 of 7	


1
2
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H
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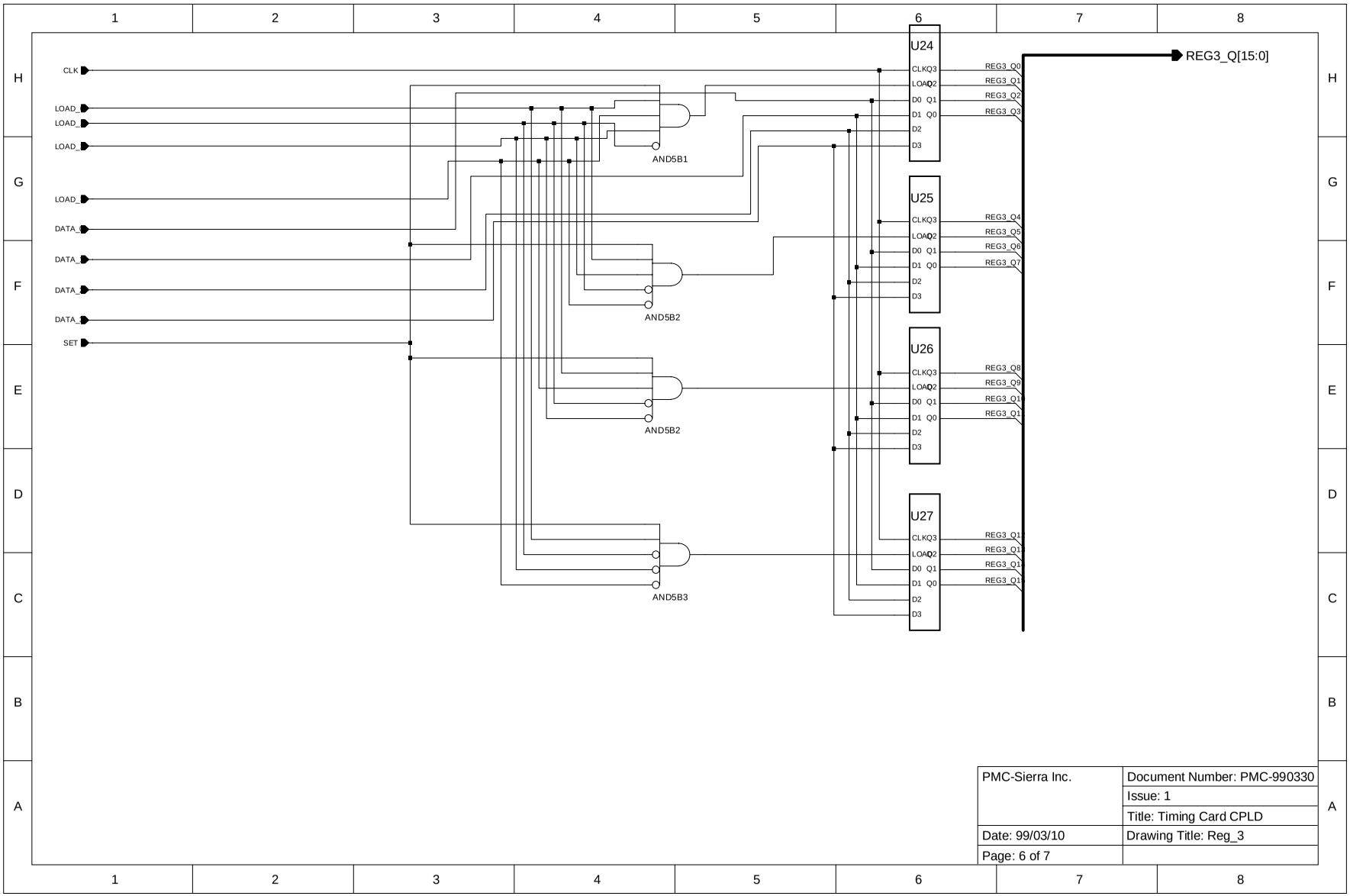
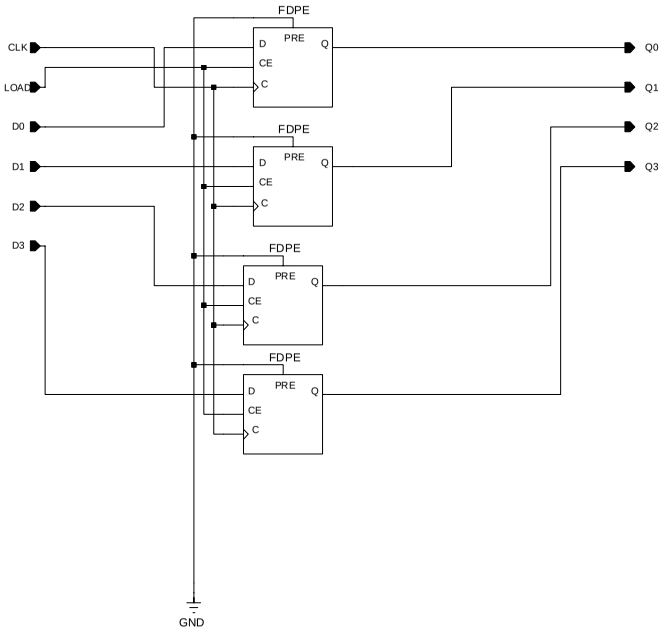
F
E
D
C
B
A
CLK
LOAD_
LOAD_
LOAD_
LOAD_
DATA_
DATA_
DATA_
DATA_
SET
AND5B1
AND5B2
AND5B2
AND5B3
U19
U20
U21
U22
REG
CLKQ3
LOAD
D0 Q1
D1 Q0
D2
D3
REG2_Q0
REG2_Q1
REG2_Q2
REG2_Q3
REG2_Q4
REG2_Q5
REG2_Q6
REG2_Q7
REG2_Q8
REG2_Q9
REG2_Q10
REG2_Q11
REG2_Q12
REG2_Q13
REG2_Q14
REG2_Q15
REG2_Q[15:0]
PMC-Sierra Inc.
Document Number: PMC-990330
Issue: 1
Title: Timing Card CPLD
Date: 99/03/10
Drawing Title: Reg_2
Page: 5 of 7



PMC-Sierra Inc.	Document Number: PMC-990330
	Issue: 1
	Title: Timing Card CPLD
Date: 99/03/10	Drawing Title: Reg_3
Page: 6 of 7	



PMC-Sierra Inc.	Document Number: PMC-990330
	Issue: 1
	Title: Timing Card CPLD
Date: 99/03/10	Drawing Title: Reg
Page: 7 of 7	

NOTES

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PMC-990330 (P2) Issue date: May 1999