



LC7153, 7153M

Universal Dual-PLL Frequency Synthesizers



Overview

The LC7153 and LC7153M are universal dual-PLL frequency synthesizers for use in cordless telephone applications in the USA, South Korea and Australia, and satellite broadcast tuners in the USA and Europe.

The LC7153 and LC7153M both have two PLLs with a 16-bit programmable divider to generate a 1.5 to 160MHz local-oscillator frequency, and a phase detector.

They also have a dual charge pump and fast lock-up circuitry for rapid PLL locking when changing frequency, an unlock indication output and an uncommitted output under external control. The PLLs share a 14-bit divider to generate a 320Hz to 640kHz reference frequency using a 10.24MHz crystal.

The LC7153 and LC7153M can be controlled from an external microcontroller using a C²B serial interface.

They also have a standby mode for single PLL operation. The LC7153 and LC7153M operate from a 4.0 to 5.5V supply. The LC7153 is available in 24-pin DIPs, and the LC7153M, in 24-pin MFPs.

Features

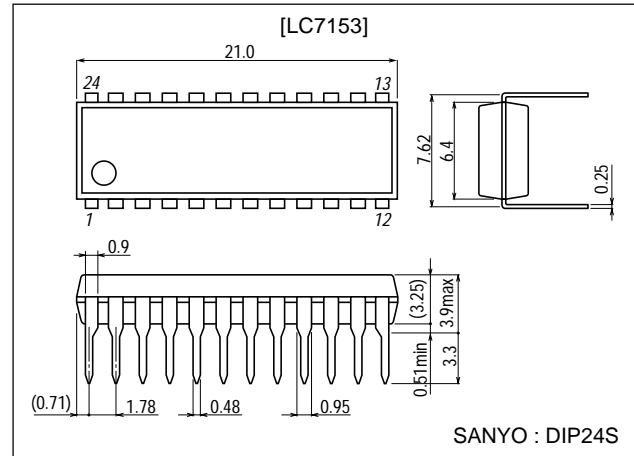
- Dual charge pump and fast lock-up circuitry for rapid PLL locking.
- PLL unlock indication.
- 16-bit programmable local-oscillator divider.
- 1.5 to 160MHz local-oscillator frequency ($V_{DD}=4.0$ to 5.5V).
- 14-bit programmable reference-frequency divider.
- 320Hz to 640kHz reference frequency using a 10.24MHz crystal.
- LPF transistor.
- C²B serial interface.
- 4.0 to 5.5V supply.
- 24-pin DIP (LC7153) and 24-pin MFP (LC7153M)

- CCB is a trademark of SANYO ELECTRIC CO., LTD.
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Package Dimensions

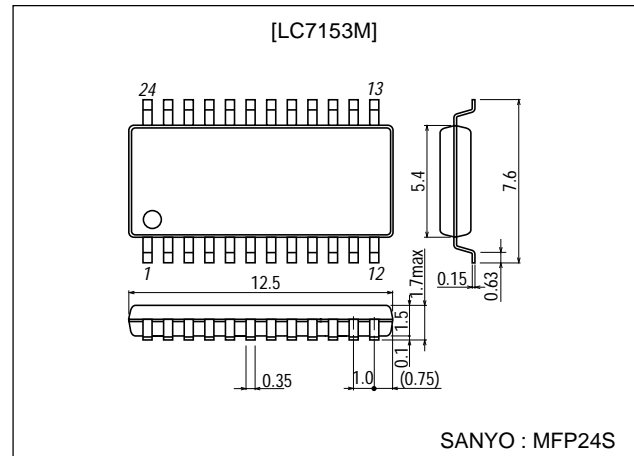
unit:mm

3067A-DIP24S



unit:mm

3112A-MFP24S



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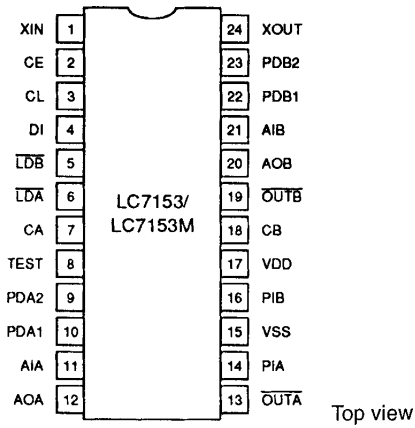
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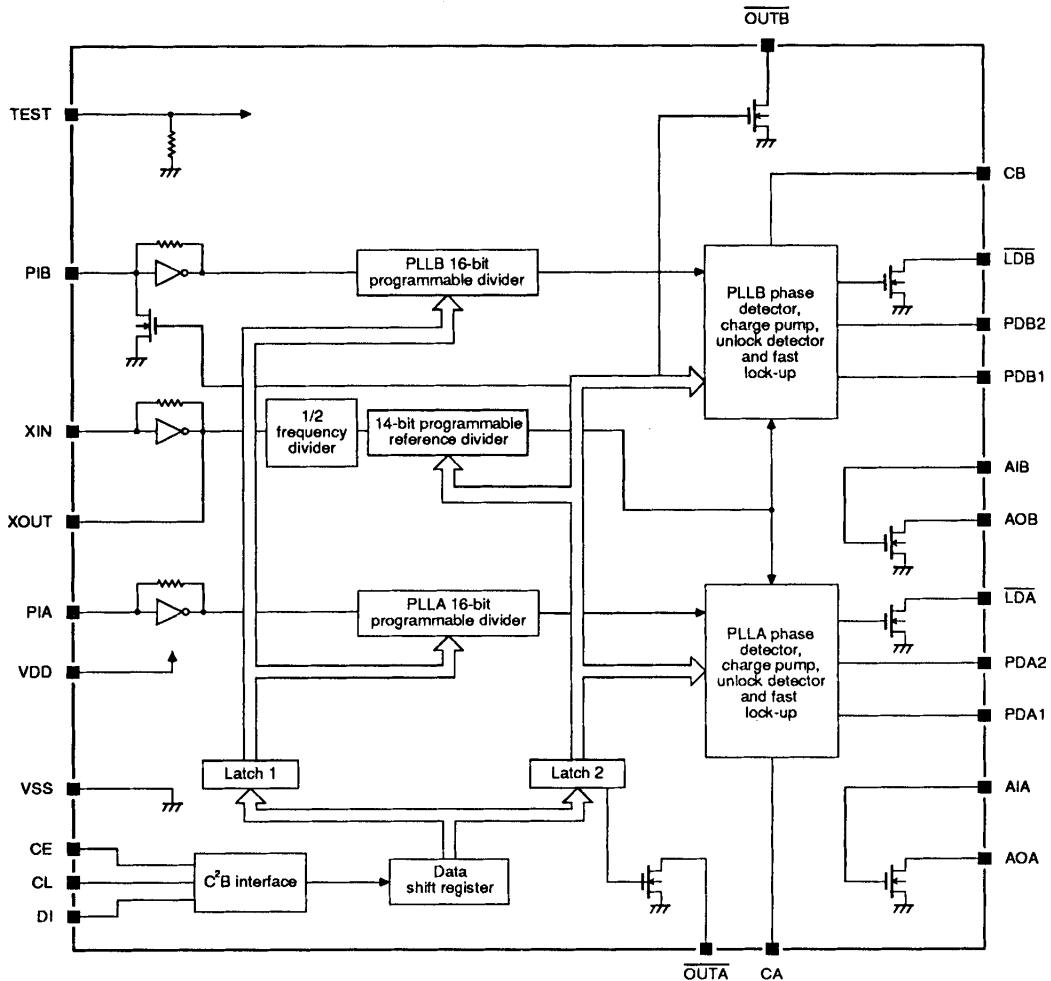
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Pin Assignment



Block Diagram



LC7153, 7153M

Pin Functions

| Number | Name | Function |
|--------|--------------------------|--------------------------------------|
| 1 | XIN | Crystal oscillator input |
| 2 | CE | Chip enable input |
| 3 | CL | Clock input |
| 4 | DI | Serial data input |
| 5 | $\overline{\text{LDB}}$ | PLLB unlock-detector output |
| 6 | $\overline{\text{LDA}}$ | PLLA unlock-detector output |
| 7 | CA | Fast lock-up capacitor A connection |
| 8 | TEST | Test input |
| 9 | PDA2 | PLLA phase-detector secondary output |
| 10 | PDA1 | PLLA phase-detector main output |
| 11 | AIA | LPF transistor A input |
| 12 | AOA | LPF transistor A output |
| 13 | $\overline{\text{OUTA}}$ | Uncommitted output A |
| 14 | PIA | PLLA local-oscillator input |
| 15 | V _{SS} | Ground |
| 16 | PIB | PLLB local-oscillator input |
| 17 | V _{DD} | 5V supply |
| 18 | CB | Fast lock-up capacitor B connection |
| 19 | $\overline{\text{OUTB}}$ | Uncommitted output B |
| 20 | AOB | LPF transistor B output |
| 21 | AIB | LPF transistor B input |
| 22 | PDB1 | PLLB phase-detector main output |
| 23 | PDB2 | PLLB phase-detector secondary output |
| 24 | XOUT | Crystal oscillator output |

Specifications

Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|--|------------------|------------|------------------------------|------|
| Supply voltage range | V _{DD} | | -0.3 to +7.0 | V |
| CE, CL, DI, AIA and AIB input voltage range | V _{I1} | | -0.3 to +7.0 | V |
| XIN, PIA, PIB, CA, CB and TEST input voltage range | V _{I2} | | -0.3 to V _{DD} +0.3 | V |
| $\overline{\text{LDA}}$, $\overline{\text{LDB}}$, $\overline{\text{OUTA}}$ and $\overline{\text{OUTB}}$ output current range | I _{O1} | | 0 to 3 | mA |
| AOA and AOB output current range | I _{O2} | | 0 to 6 | mA |
| CA and CB output current range | I _{O3} | | 0 to 1 | mA |
| $\overline{\text{LDA}}$ and $\overline{\text{LDB}}$ output voltage range | V _{O1} | | -0.3 to +7.0 | V |
| AOA, AOB, $\overline{\text{OUTA}}$ and $\overline{\text{OUTB}}$ output voltage range | V _{O2} | | -0.3 to 15.0 | V |
| PDA1, PDA2, PDB1, PDB2, CA, CB and XOUT output voltage range | V _{O3} | | -0.3 to V _{DD} +0.3 | V |
| Allowable power dissipation | Pd max | LC7153 | 350 | mW |
| | | LC7153M | 240 | mW |
| Operating temperature | T _{opr} | | -40 to +85 | °C |
| Storage temperature | T _{stg} | | -55 to +125 | °C |

(Note) Pins PIA, PIB, CA and CB have a weaker electrostatic breakdown strength than the other pins.

Recommended Operating Conditions at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------------|-----------------|------------|------------|------|
| Supply voltage | V _{DD} | | 5 | V |
| Supply voltage range | V _{DD} | | 4.0 to 5.5 | V |

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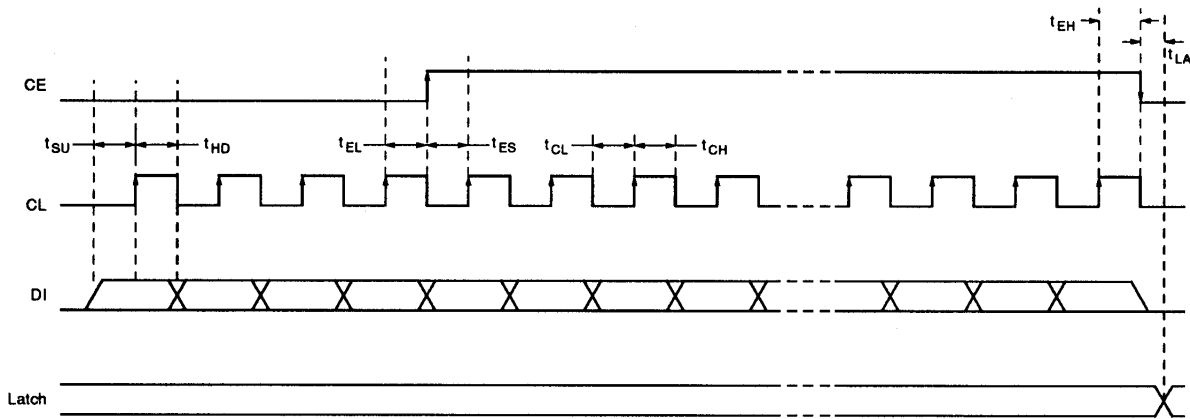
Electrical Characteristics at Ta = -40 to +85°C, V_{DD}=4.0 to 5.5V, V_{SS}=0V, unless otherwise noted.

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|-----------------------------|---|-----------------------|-----------------------|-----------------------|------|
| | | | min | typ | max | |
| Supply current | I _{DD} | V _{DD} =4.5V, f _i =60MHz. See note 1. | | 9.0 | 18.0 | mA |
| | | V _{DD} =5.5V, f _i =160MHz. See note 1. | | 20.0 | 40.0 | mA |
| | | V _{DD} =4.5V, f _i =60MHz. See note 2. | | 5.0 | 10.0 | mA |
| | | V _{DD} =5.5V, f _i =160MHz. See note 2. | | 11.0 | 22.0 | mA |
| CE, CL and DI low-level input voltage | V _{IL1} | | 0 | | 0.8 | V |
| CE, CL and DI high-level input voltage | V _{IH1} | | 2.2 | | 5.5 | V |
| PDA1 and PDB1 low-level output voltage | V _{OL1} | I _O =1mA | | | 1.0 | V |
| PDA2 and PDB2 low-level output voltage | V _{OL2} | I _O =2mA | | | 1.0 | V |
| LDA, LDB, O _{UT} A and O _{UT} B low-level output voltage | V _{OL3} | I _O =2mA | 0 | | 1.0 | V |
| AOA and AOB low-level output voltage | V _{OL4} | I _O =0.5mA, V _{AIA} =V _{AIB} =1.2V | 0 | | 0.5 | V |
| | | I _O =1mA, V _{AIA} =V _{AIB} =1.3V | 0 | | 0.5 | V |
| PDA1 and PDB1 high-level output voltage | V _{OH1} | I _O =1mA | V _{DD} -1 | | | V |
| PDA2 and PDB2 high-level output voltage | V _{OH2} | I _O =2mA | V _{DD} -1 | | | V |
| LDA and LDB output voltage | V _{O1} | | 0 | | 5.5 | V |
| AOA, AOB, O _{UT} A and O _{UT} B output voltage | V _{O2} | | 0 | | 13.0 | V |
| CA and CB output voltage | V _{O3} | | 0 | | V _{DD} | V |
| CA and CB low-level threshold voltage | V _T ⁻ | | | | 0.2V _{DD} | V |
| CA and CB high-level threshold voltage | V _T ⁺ | | 0.5V _{DD} | | | V |
| CE, CL and DI low-level input current | I _{IL1} | V _i =0V | | | 5.0 | μA |
| XIN low-level input current | I _{IL2} | V _i =0V, V _{DD} =5.0V | 3.5 | | 11 | μA |
| PIA and PIB low-level input current | I _{IL3} | V _i =0V, V _{DD} =5.0V | 6.0 | | 18.0 | μA |
| AIA and AIB low-level input current | I _{IL4} | V _i =0V | | 0.01 | 10.0 | nA |
| TEST low-level input current | I _{IL5} | V _i =0V, V _{DD} =5.0V | | | 5.0 | μA |
| CE, CL and DI high-level input current | I _{IH1} | V _i =5.5V | | | 5.0 | μA |
| XIN high-level input current | I _{IH2} | V _i =5.0V, V _{DD} =5.0V | 3.5 | | 11.0 | μA |
| PIA and PIB high-level input current | I _{IH3} | V _i =5.0V, V _{DD} =5.0V | 6.0 | | 18.0 | μA |
| AIA and AIB high-level input current | I _{IH4} | V _i =5.0V | | 0.01 | 10.0 | nA |
| TEST high-level input current | I _{IH5} | V _i =5.0V, V _{DD} =5.0V | | 160 | | μA |
| LDA and LDB output leakage current | I _{OFF1} | V _O =5.5V | | | 5.0 | μA |
| PDA1, PDB1, PDA2 and PDB2 output leakage current | I _{OFF2} | V _O =0 or 5.5V | | 0.01 | 10.0 | nA |
| AOA, AOB, O _{UT} A and O _{UT} B output leakage current | I _{OFF3} | V _O =13V | | | 5.0 | μA |
| CA and CB output leakage current | I _{OFF4} | V _O =0 V or V _{DD} | | | 100 | nA |
| CA and CB source current | I _{S1} | V _O =0V, V _{DD} =5.0V | -95 | -190 | -380 | μA |
| Fast lock-up mode 0 CA and CB sink current | I _{S2(0)} | V _O =3.0V, V _{DD} =5.0V | 3.5I _{S2(3)} | 4.0I _{S2(3)} | 4.5I _{S2(3)} | μA |
| Fast lock-up mode 1 CA and CB sink current | I _{S2(1)} | V _O =3.0V, V _{DD} =5.0V | 2.5I _{S2(3)} | 3.0I _{S2(3)} | 3.4I _{S2(3)} | μA |
| Fast lock-up mode 2 CA and CB sink current | I _{S2(2)} | V _O =3.0V, V _{DD} =5.0V | 1.5I _{S2(3)} | 2.0I _{S2(3)} | 2.4I _{S2(3)} | μA |
| Fast lock-up mode 3 CA and CB sink current | I _{S2(3)} | V _O =3.0V, V _{DD} =5.0V | 18 | 35 | 70 | μA |
| XIN input frequency | f _{i1} | Capacitively coupled sine wave | 1 | | 13 | MHz |
| PIA and PIB input frequency | f _{i2} | Capacitively coupled sine wave, V _{DD} =5.0V | 1.5 | | 160 | MHz |
| XIN rms input amplitude | V _{i1} | Capacitively coupled sine wave | 100 | | 800 | mV |
| PIA and PIB rms input amplitude | V _{i2} | Capacitively coupled sine wave | 70 | | 800 | mV |
| Crystal oscillator frequency | f _{XTAL} | C _i ≤50Ω. See note 3. | 4.0 | 10.24 | 13.0 | MHz |
| XIN internal feedback resistor | R _{f1} | V _{DD} =5.0V | | | 0.7 | MΩ |
| PIA and PIB internal feedback resistor | R _{f2} | V _{DD} =5.0V | | | 430 | kΩ |
| TEST internal pull-down resistor | R _d | V _{DD} =5.0V | | | 30 | kΩ |
| XIN, PIA and PIB input capacitance | C _i | | | 6.0 | | pF |

Notes

- Dual PLL, both PLLA and PLLB operating, SB=0, f_{XTAL}=10.24MHz, V_{PIA}=V_{PIB}=70mV, all other inputs=0V, all outputs open.
- Standby mode, PLLB stopped, SB=1, f_{XTAL}=10.24MHz, V_{PIA}=70mV, all other inputs=0V, all outputs open.
- C_i in the crystal impedance. Contact Nihon Denpa Kogyo for further information.

Serial Data Input Timing



| Parameter | Symbol | Conditions | Ratings | | Unit |
|--------------------------------|----------|---------------------------|--------------|--------------|------|
| | | | min | max | |
| Data setup time | t_{SU} | 10.24MHz crystal | 400 | | ns |
| | | Other crystal frequencies | $4/f_{XTAL}$ | | ns |
| Data hold time | t_{HD} | 10.24MHz crystal | 400 | | ns |
| | | Other crystal frequencies | $4/f_{XTAL}$ | | ns |
| LOW-level chip enable time | t_{EL} | 10.24MHz crystal | 400 | | ns |
| | | Other crystal frequencies | $4/f_{XTAL}$ | | ns |
| Chip enable setup time | t_{ES} | 10.24MHz crystal | 400 | | ns |
| | | Other crystal frequencies | $4/f_{XTAL}$ | | ns |
| Chip enable hold time | t_{EH} | 10.24MHz crystal | 400 | | ns |
| | | Other crystal frequencies | $4/f_{XTAL}$ | | ns |
| LOW-level clock pulsewidth | t_{CL} | 10.24MHz crystal | 400 | | ns |
| | | Other crystal frequencies | $4/f_{XTAL}$ | | ns |
| HIGH-level clock pulsewidth | t_{CH} | 10.24MHz crystal | 400 | | ns |
| | | Other crystal frequencies | $4/f_{XTAL}$ | | ns |
| Chip enable to data latch time | t_{LA} | 10.24MHz crystal | | 400 | ns |
| | | Other crystal frequencies | | $4/f_{XTAL}$ | ns |

Functional Description

PLLA and PLLB Programmable Dividers

PLLA and PLLB input frequency ranges are set by Mode 2 command bits FA and FB, respectively. Their divider ratios, N_A and N_B , are set by Mode 1 command bits DA0 to DA15 and DB0 to DB15, respectively.

Programmable Reference Divider

The divider ratio, NR, is set by Mode 2 command bits R0 to R13. The reference frequency is given by $f_{XIN}/(2 \times NR)$.

Phase Detector

The state of the phase-detector output as a function of the divider ratio and reference frequency is shown in table 1. Table 1. Phase-detector output states

| Condition | PDA1, PDB1 |
|-------------------|----------------|
| $f_i/N > f_{ref}$ | HIGH |
| $f_i/N < f_{ref}$ | LOW |
| $f_i/N = f_{ref}$ | HIGH impedance |

Note

$N=N_A$ for PLLA, and N_B for PLLB

When PLLA is unlocked, \overline{LDA} is pulled LOW and both PDA1 and PDA2 are active. PLLB operates identically to PLLA. Mode 2 command bits UL0 and UL1 set the unlock phase-error threshold, and bits UE0 and UE1, the \overline{LDA} and \overline{LDB} output extension.

Dual Charge Pump

A typical dual charge-pump configuration is shown in figure 1. The phase-detector secondary output is active after a change in frequency, and the phase error causes the PLL to unlock. In this case, the load resistance R1 becomes $R1M||R1S$, decreasing the LPF time constant and the time required to lock the PLL.

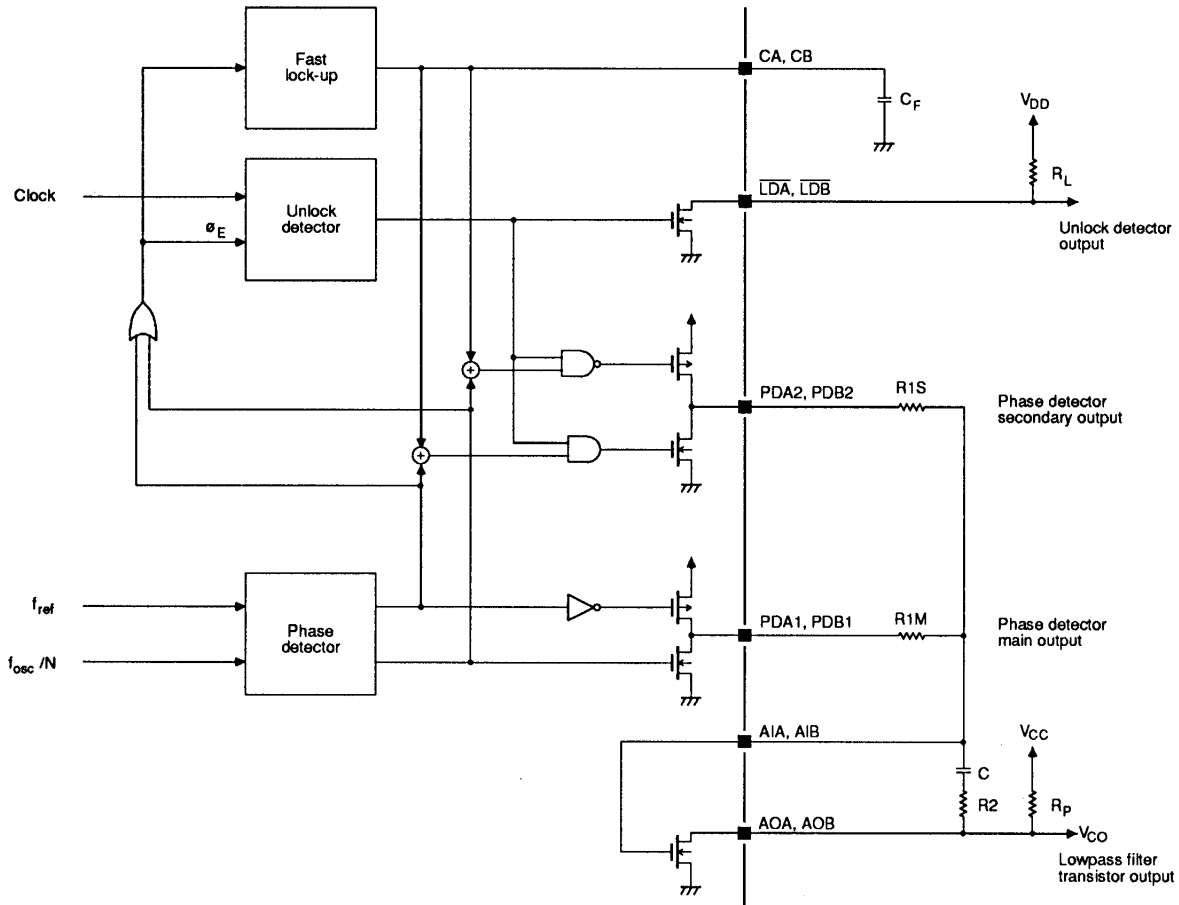


Figure 1. Dual charge-pump circuit

The phase-detector secondary output is high impedance when the PLL is locked. In this case, R1 becomes R1M,

increasing the LPF time constant and improving sideband and modulation response.

Test Mode

TEST should be LOW or open for normal operation.

Serial Input Data

Serial data should be input only after f_{XIN} has become stable.

The command format is shown in figure 2. Bits DA0 to DA15 and DB0 to DB15 determine the PLLA and PLLB programmable divider ratios, respectively. Bit DA0 is the first bit received. The range of allowable divider ratios is $N = 256$ (0100H) to 65535 (FFFFH).

Mode 1 command format and functions

The Mode 1 command comprises the data bits which determine the PLLA and PLLB programmable divider ratios.

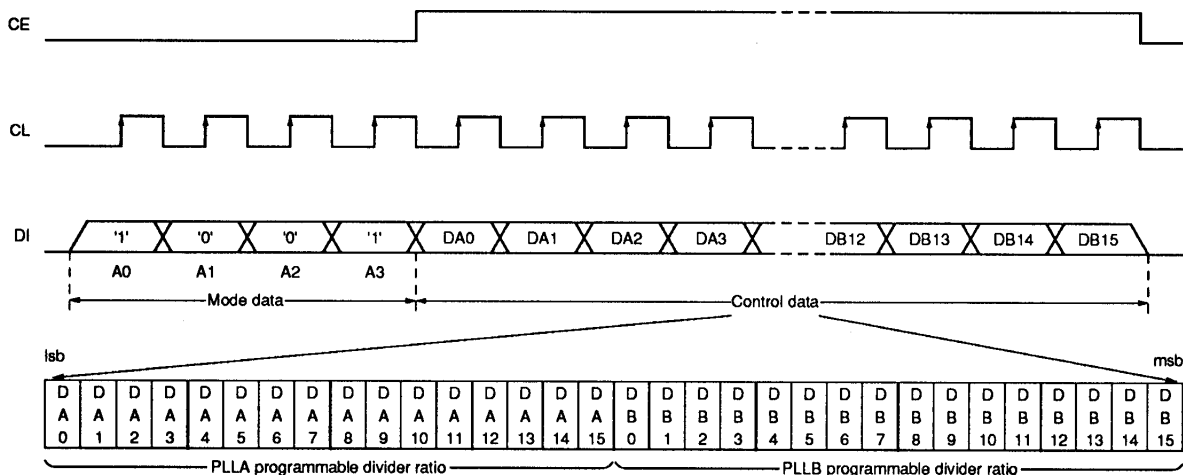


Figure 2. Mode 1 command (programmable divider data)

Mode 2 command format and functions

The Mode 2 command comprises the data bits which determine the reference frequency divider ratio and control

functions. The command format is shown in figure 3. Bit R0 is the first bit received.

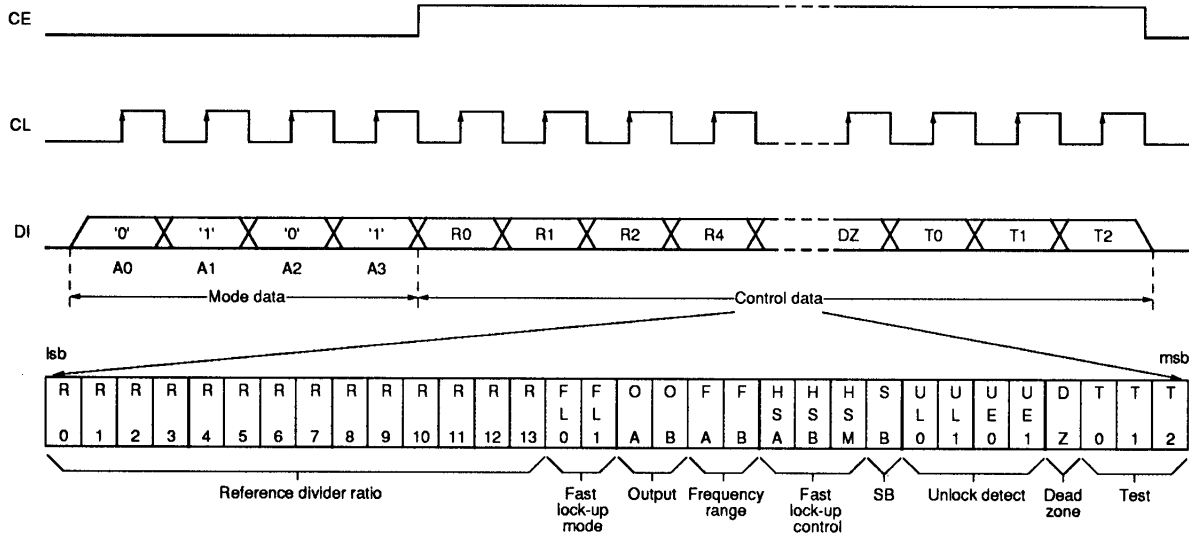


Figure 3. Mode 2 command (reference divider and control data)

Bits R0 to R13 determine the reference divider ratio. The range of allowable divider ratios is $N_R=8$ (0008H) to 16383 (3FFFH).

Bits FL0 and FL1 are the fast lock-up mode select bits. The fast lock-up modes are shown in table 2. The higher the mode number, the greater the expansion width of the detected phase error signal.

| FL0 | FL1 | Fast lock-up mode |
|-----|-----|-------------------|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 1 | 3 |

Bits OA and OB are the uncommitted output control bits. They are latched and then inverted to control \overline{OUTA} and \overline{OUTB} , respectively. If either bit is 1, the open-drain output is pulled LOW.

Bits FA and FB are the input frequency range select bits. The PIA and PIB frequency ranges, set by FA and FB, respectively, are shown in table 3.

Table 3. Frequency ranges

| FA, FB | Input frequency range | Unit |
|--------|-----------------------|------|
| 0 | 1.5 to 40.0 | MHz |
| 1 | 35 to 160 | MHz |

Bits HSA, HSB and HSM are the fast lock-up control bits. When HSA or HSB=1, the fast lock-up circuits for PLLA or PLLB, respectively, are ON. When HSA or HSB=0, the respective circuits are OFF. For use with FM, the fast lock-up circuits should be OFF. HSM determines the fast lock-up operating mode. When HSM=0, operating mode 0 is selected and the fast lock-up only operates when the PLLs are unlocked. When HSM=1, operating mode 1 is selected and the fast lock-up operates normally, as shown in figure 4.

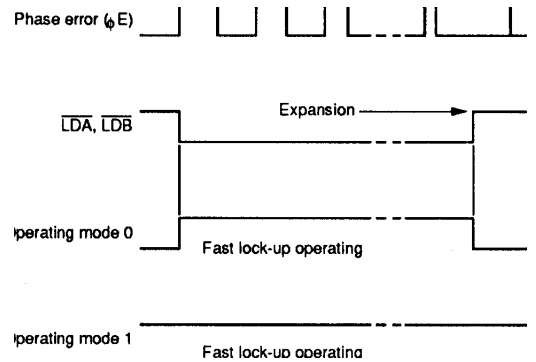


Figure 4. Fast lock-up operating modes

Bit SB is the standby mode control bit. When SB=1, standby mode is selected. In standby mode, PLLB is stopped, PIB is pulled LOW, and PDB1 and PDB2 are high impedance. When SB=0, normal operation is selected.

Bits UL0 and UL1 determine the unlock detection threshold. The PLL unlock detector output, \overline{LDA} or \overline{LDB} , is pulled LOW when the phase differential between the reference and the divider inputs exceeds the threshold set by UL0 and UL1. The threshold for different crystal frequencies is shown in table 4, and the threshold for other frequencies can be calculated. The threshold is common to both PLLs. Note that a PLL will temporarily lose lock when either UL0 or UL1 is changed.

Table 4. Unlock detector thresholds

| UL0 | UL1 | $\overline{\text{LDA}}, \overline{\text{LDB}}$ phase error threshold | Example phase error thresholds (μs) | | | | |
|-----|-----|--|--|--------------------------------|------------------------------|----------------------------------|---------------------------------|
| | | | $f_{\text{XIN}}=4\text{MHz}$ | $f_{\text{XIN}}=7.2\text{MHz}$ | $f_{\text{XIN}}=8\text{MHz}$ | $f_{\text{XIN}}=10.24\text{MHz}$ | $f_{\text{XIN}}=12.8\text{MHz}$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | $\pm 4/f_{\text{XIN}}$ | ± 1.00 | ± 0.55 | ± 0.50 | ± 0.39 | ± 0.31 |
| 0 | 1 | $\pm 16/f_{\text{XIN}}$ | ± 4.00 | ± 2.22 | ± 2.00 | ± 1.56 | ± 1.20 |
| 1 | 1 | $\pm 64/f_{\text{XIN}}$ | ± 16.00 | ± 8.88 | ± 8.00 | ± 6.25 | ± 5.00 |

Bits UE0 and UE1 determine the unlock extension, or delay, before the unlock detector outputs, $\overline{\text{LDA}}$ and $\overline{\text{LDB}}$, can change state. The extension for different reference frequen-

cies is shown in table 5. However, if a phase-error threshold of zero is set using UL0 and UL1, no output extension occurs.

Table 5. $\overline{\text{LDA}}, \overline{\text{LDB}}$ output extension

| UE0 | UE1 | $\overline{\text{LDA}}, \overline{\text{LDB}}$ output extension | Example output extensions (ms) | | |
|-----|-----|---|--------------------------------|------------------------------|---------------------------------|
| | | | $f_{\text{ref}}=1\text{kHz}$ | $f_{\text{ref}}=5\text{kHz}$ | $f_{\text{ref}}=12.5\text{kHz}$ |
| 0 | 0 | $4/f_{\text{ref}}$ | 4.0 (typ) | 0.8 | 0.32 |
| 1 | 0 | $8/f_{\text{ref}}$ | 8.0 | 1.6 | 0.64 |
| 0 | 1 | $32/f_{\text{ref}}$ | 32.0 | 6.4 (typ) | 2.56 |
| 1 | 1 | $64/f_{\text{ref}}$ | 64.0 | 12.8 | 5.12 (typ) |

Bit DZ is the dead-zone selection bit. It selects the phase-insensitive bandwidth, or dead zone, of the phase comparator. When DZ=1, DZB mode is selected, and when DZ=0, DZA mode. DZB mode has larger dead zone than DZA mode.

Bits T0, T1 and T2 are test bits. They should be set to 0 for normal operation.

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Typical Application

A LC7153 or LC7153M cordless telephone application circuit is shown in figure 5. The telephone is tuned to channel 1, which has a transmit VCO frequency of 46.610MHz and a receive VCO frequency of 38.975MHz.

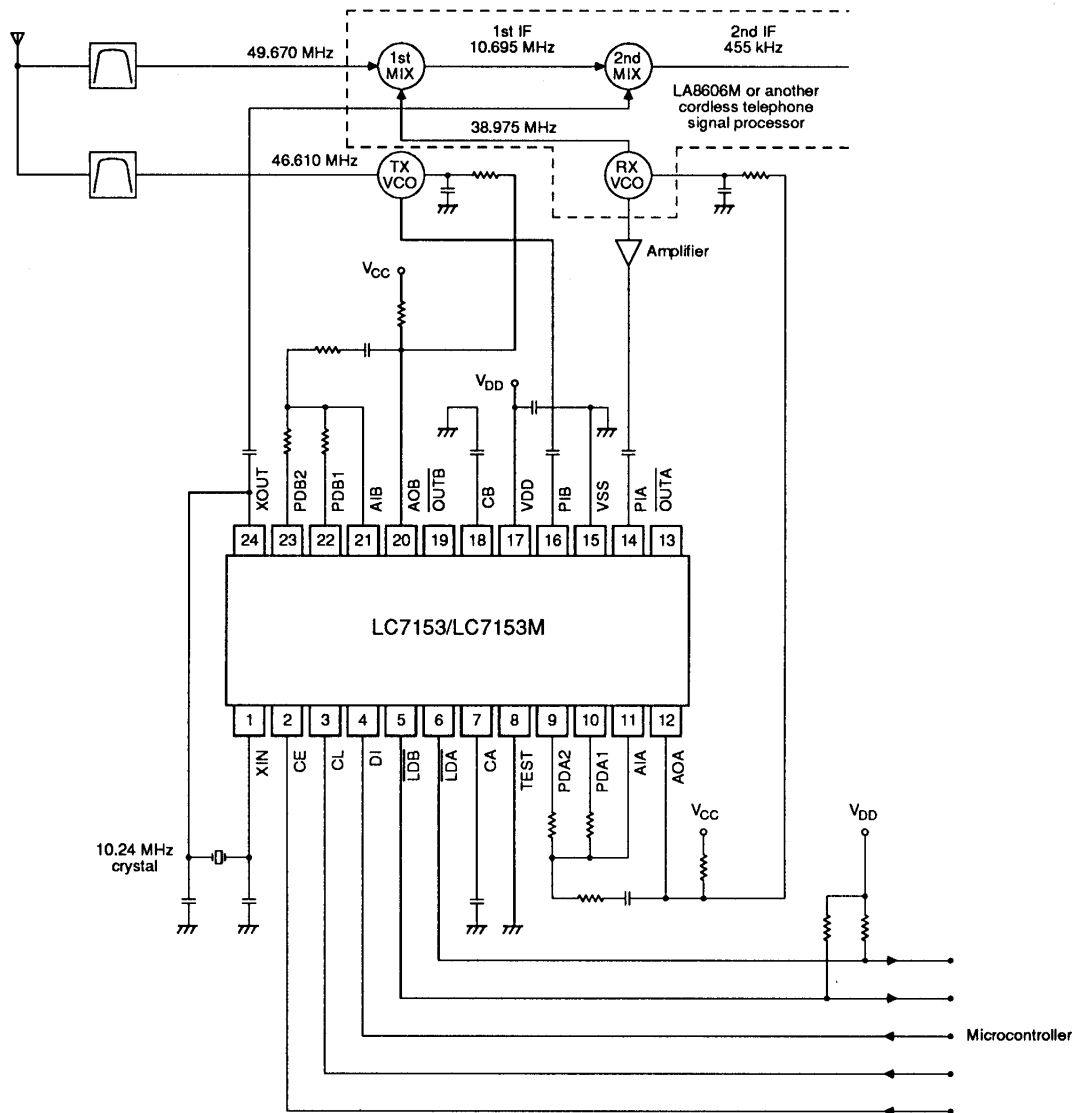


Figure 5. American 10-channel, 46/49 MHz, cordless telephone base station

For $f_{ref} = 5\text{kHz}$, the divider ratios are as follows.

$$N_A = \frac{f_{IA}}{f_{ref}} = \frac{\text{RX VCO}}{f_{ref}} = \frac{38.975\text{MHz}}{5\text{kHz}} = 7795 \text{ (1E73H)}$$

$$N_B = \frac{f_{IB}}{f_{ref}} = \frac{\text{TX VCO}}{f_{ref}} = \frac{46.610\text{MHz}}{5\text{kHz}} = 9322 \text{ (246AH)}$$

$$N_R = \frac{f_{XIN}}{2 \times f_{ref}} = \frac{10.24\text{MHz}}{2 \times 5\text{kHz}} = 1024 \text{ (400H)}$$

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The Mode 1 and Mode 2 commands are shown in tables 6 and 7, respectively, and in figures 6 and 7, respectively.

Table 6. Mode 1 command

| Field | Value | Comment |
|-------------|-------|-------------------------|
| DA0 to DA15 | 1E73H | PLLA divider ratio 7795 |
| DB0 to DB15 | 246AH | PLLB divider ratio 9322 |

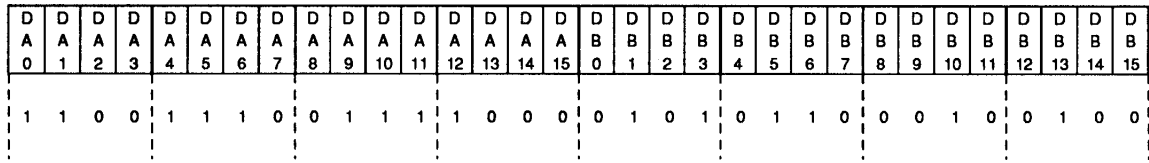


Figure 6. Mode 1 command

Table 7. Mode 2 command

| Field | Value | Comment |
|------------|--------|--|
| R0 to R13 | 0400H | Reference divider ratio of 1024 |
| FL0, FL1 | 00 | Fast lock-up mode 0 |
| OA | 0 | OUTA and OUTB left open. |
| OB | 0 | |
| FA | 1 | 20 to 55MHz RX VCO input frequency range |
| FB | 1 | 20 to 55MHz TX VCO input frequency range |
| HSA, HSB | 00 | PLLA and PLLB fast lock-up OFF |
| HSM | 0 | Fast lock-up operating mode 0 |
| SB | 0 or 1 | Standby mode selection |
| UL0, UL1 | 11 | ±6.25µs lock/unlock detection threshold |
| UE0, UE1 | 01 | 6.4ms $\overline{LD\bar{A}}$ and $\overline{LD\bar{B}}$ output extension |
| DZ | 1 | DZB dead-zone mode |
| T0, T1, T2 | 000 | Test mode deselected |

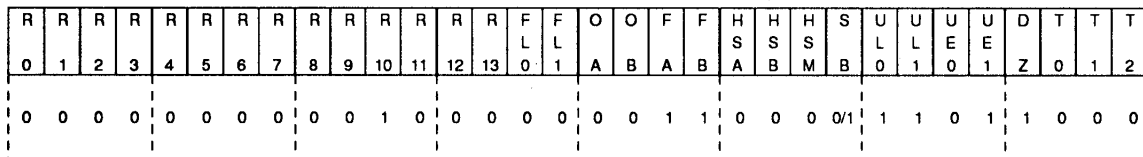


Figure 7. Mode 2 command

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