HM51W4405BS Series

1,048,576-word × 4-bit Dynamic Random Access Memory

HITACHI

ADE-203-686A (Z)
Rev. 1.0
Nov. 29, 1996

Description

The Hitachi HM51W4405BS Series is a CMOS dynamic RAM organized 1,048,576-word × 4-bit. HM51W4405BS Series has realized higher density, higher performance and various functions by employing 0.8 µm CMOS process technology and some new CMOS circuit design technologies. The HM51W4405BS Series offers Extended Data Out (EDO) Page Mode as a high speed access mode. It has the package variations of standard 26-pin plastic SOJ.

Features

- Single 3.3 V (±0.3 V) (HM51W4405BS-7)
- Single 3.3 V (+0.3 V/–0.15 V) (HM51W4405BS-6R)
- High speed
  - Access time: 60/70 ns (max)
- Low power dissipation
  - Active mode: 288/252 mW (max)
  - Standby mode: 7.2 mW (max)
- EDO page mode capability
- 1024 refresh cycles : 16 ms
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh

Ordering Information

Type No.	Access time	Package
HM51W4405BS-6R	60 ns	300-mil 26-pin plastic SOJ (CP-26/20D)
HM51W4405BS-7	70 ns	

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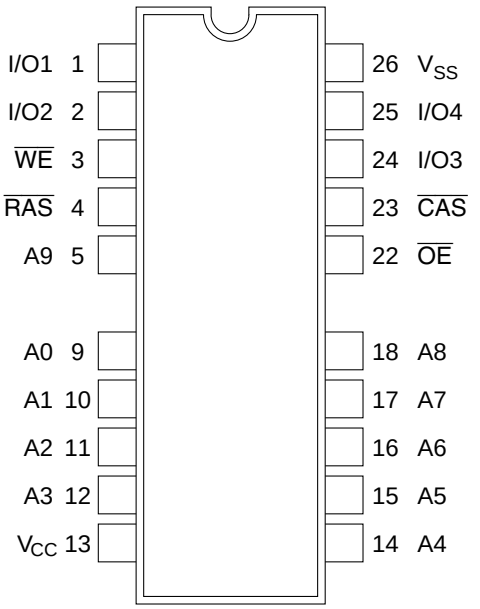
Pin Arrangement

HM51W4405BS Series

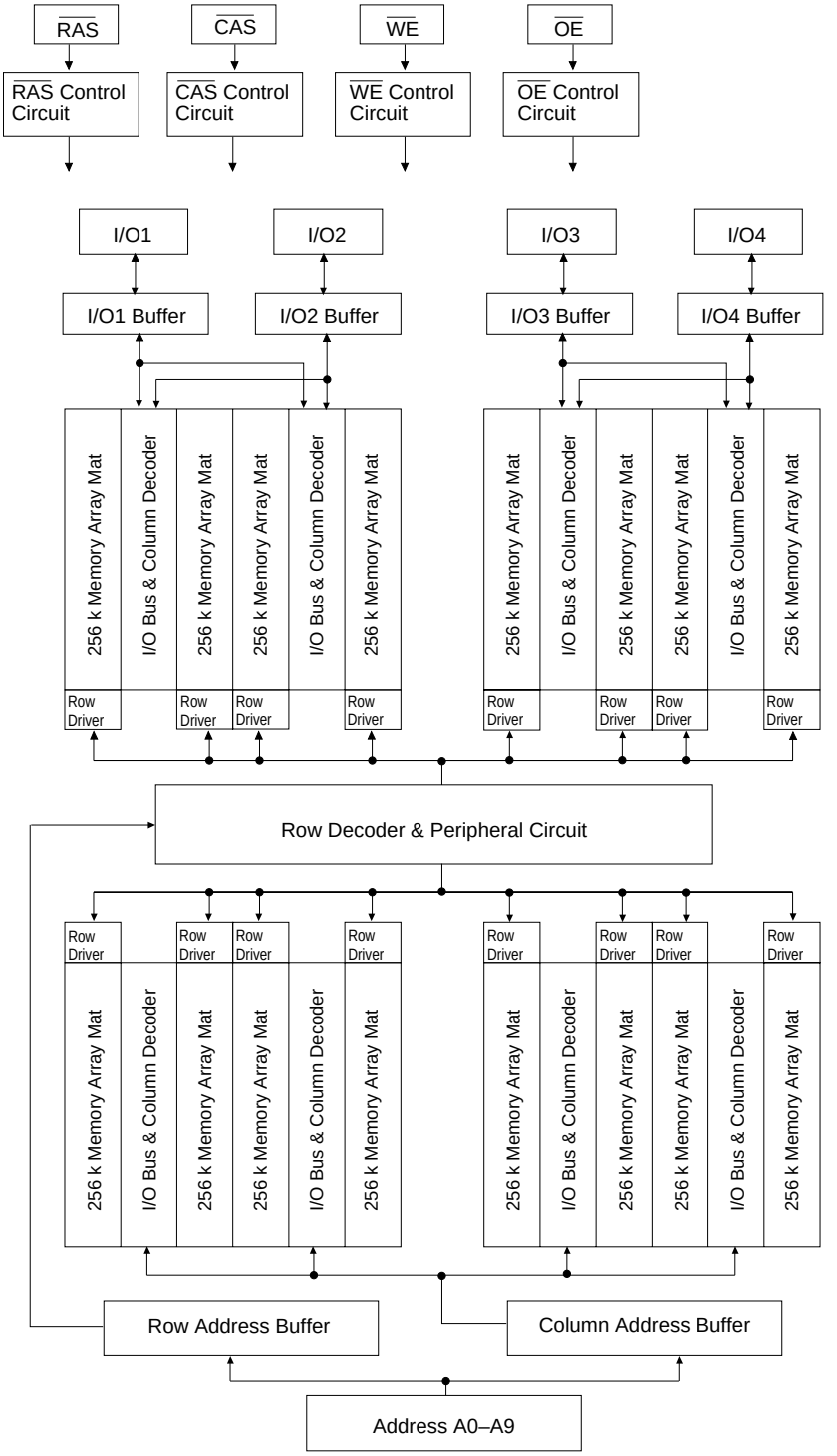


(Top view)

Pin Description

Pin name	Function
A0 to A9	Address input — Row/Refresh A0 to A9 — Column A0 to A9
I/O1 to I/O4	Data-in/Data-out
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/Write enable
$\overline{OE}$	Output enable
V_{cc}	Power supply
V_{ss}	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
(HM51W4405BS-6R)	V_{CC}	3.15	3.3	3.6	V	1
(HM51W4405BS-7)	V_{CC}	3.0	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}.

DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V +0.3 V/–0.15 V, V_{SS} = 0 V) (HM51W4405BS-6R)
(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (HM51W4405BS-7)

		HM51W4405B					
		-6R		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Operating current*[1, 2]	I_{CC1}	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min
Standby current	I_{CC2}	—	2	—	2	mA	TTL interface, $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z
		—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current*[2]	I_{CC3}	—	80	—	70	mA	t_{RC} = min
Standby current*[1]	I_{CC5}	—	4	—	4	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	80	—	70	mA	t_{RC} = min
EDO page mode current*[1, 3]	I_{CC4}	—	100	—	85	mA	t_{HPC} = min
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 4.6 V
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 4.6 V Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed twice or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance

(Ta = 25°C, V_{CC} = 3.3 V +0.3 V/–0.15 V) (HM51W4405BS-6R)
(Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V) (HM51W4405BS-7)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{RAS}$ and $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V +0.3 V/–0.15 V, V_{SS} = 0 V) (HM51W4405BS-6R)[*1, *14, *15]
(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (HM51W4405BS-7)[*1, *14, *15]

Test Conditions

- Input rise and fall time : 2 ns
- Input level : V_{IL} = 0 V, V_{IH} = 3.0 V
- Input timing reference levels : 0.8 V, 2.0 V
- Output timing reference levels : 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM51W4405B					
		-6R		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	104	—	124	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns	17
$\overline{CAS}$ pulse width	t_{CAS}	10	10000	13	10000	ns	18
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	10	—	13	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	ns	9
$\overline{RAS}$ hold time	t_{RSH}	15	—	18	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	48	—	58	—	ns	21
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	15	—	18	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	ns	
$\overline{CAS}$ setup time from Din	t_{DZC}	0	—	0	—	ns	
Transition time (rise and fall)	t_T	2	50	2	50	ns	7
Refresh period	t_{REF}	—	16	—	16	ms	

Read Cycle

		HM51W4405B					
		-6R		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	2, 3
Access time from $\overline{CAS}$	t_{CAC}	—	15	—	18	ns	3, 4, 13
Access time from address	t_{AA}	—	30	—	35	ns	3, 5, 13
Access time from $\overline{OE}$	t_{OAC}	—	15	—	18	ns	3
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	16
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	16
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	18	—	23	—	ns	
Output buffer turn-off time	t_{OFF1}	—	15	—	15	ns	6,19
Output buffer turn-off time to $\overline{OE}$	t_{OFF2}	—	15	—	15	ns	6
$\overline{CAS}$ to Din delay time	t_{CDD}	15	—	18	—	ns	
$\overline{RAS}$ to Din delay time	t_{RDD}	15	—	18	—	ns	
$\overline{WE}$ to Din delay time	t_{WDD}	15	—	18	—	ns	
$\overline{OE}$ pulse width	t_{OEP}	15	—	18	—	ns	
Turn-off to $\overline{RAS}$	t_{OFR}	—	15	—	15	ns	6, 19
Turn-off to $\overline{WE}$	t_{WEZ}	—	15	—	15	ns	6
Output data hold time	t_{OH}	5	—	5	—	ns	
Output data hold time from $\overline{RAS}$	t_{OHR}	5	—	5	—	ns	
Read command hold time from $\overline{RAS}$	t_{RCHR}	60	—	70	—	ns	
Read command hold time from $\overline{CAS}$	t_{RCHC}	15	—	18	—	ns	
Read command hold time from column address	t_{RCHA}	30	—	35	—	ns	

Write Cycle

		HM51W4405B					
		-6R		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	ns	10
Write command hold time	t_{WCH}	10	—	13	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	—	13	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	—	13	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	11
Data-in hold time	t_{DH}	10	—	13	—	ns	11

Read-Modify-Write Cycle

		HM51W4405B					
		-6R		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	133	—	159	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	77	—	90	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	32	—	38	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	47	—	55	—	ns	10
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	15	—	18	—	ns	

Refresh Cycle

		HM51W4405B					
		-6R		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	ns	
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	—	13	—	ns	
CBR refresh cycle $\overline{WE}$ setup time	t_{WS}	0	—	0	—	ns	
CBR refresh cycle $\overline{WE}$ hold time	t_{WH}	10	—	10	—	ns	

EDO Page Mode Cycle

		HM51W4405B					
		-6R		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode cycle time	t_{HPC}	25	—	30	—	ns	20
EDO page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	13	—	ns	
EDO page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	ns	12
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	35	—	40	ns	3, 13
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	—	40	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	ns	
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	10	—	13	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHP}	35	—	40	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		HM51W4405B					
		-6R		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode read-modify-write cycle time	t_{HPCM}	66	—	77	—	ns	
EDO page mode read-modify-write cycle $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPW}	52	—	60	—	ns	10

Counter Test Cycle

		HM51W4405B					
		-6R		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ precharge time in counter test cycle	t_{CPT}	40	—	40	—	ns	

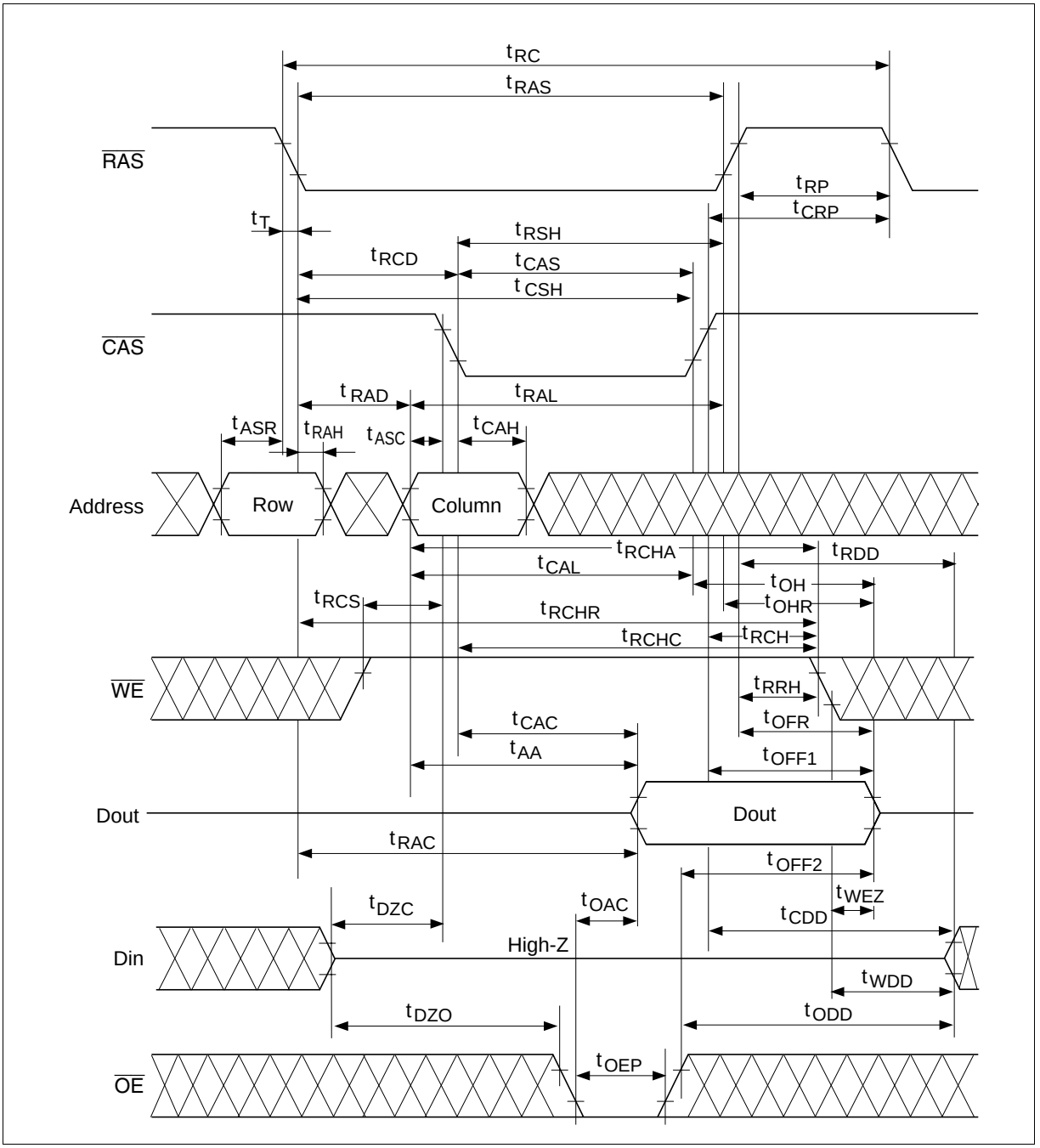
Notes:
1. AC measurements assume t_T = 2 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF1} (max), t_{OFF2} (max), t_{OFR} (max) and t_{WEZ} (max) define the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPW} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{CPW} \geq t_{CPW}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referred to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Either t_{RCH} or t_{RRH} must be satisfied
17. t_{RAS} (min) = t_{RWD} (min) + t_{RWL} (min) + t_T in read-modify-write cycle.
18. t_{CAS} (min) = t_{CWD} (min) + t_{CWL} (min) + t_T in read-modify-write cycle.
19. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH}, and between t_{OFR} and t_{OFF}.
20. t_{HPC} (min) can be achieved during a series of EDO page mode early write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle t_{HPC} (t_{CAS} + t_{CP} + 2t_T) becomes greater than the specified t_{HPC} (min) value.
21. t_{CSH} (min) can be achieved when $t_{RCD} \leq t_{CSH}$ (min) – t_{CAS} (min).
22. XXX: H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))

    ///////: Invalid Dout

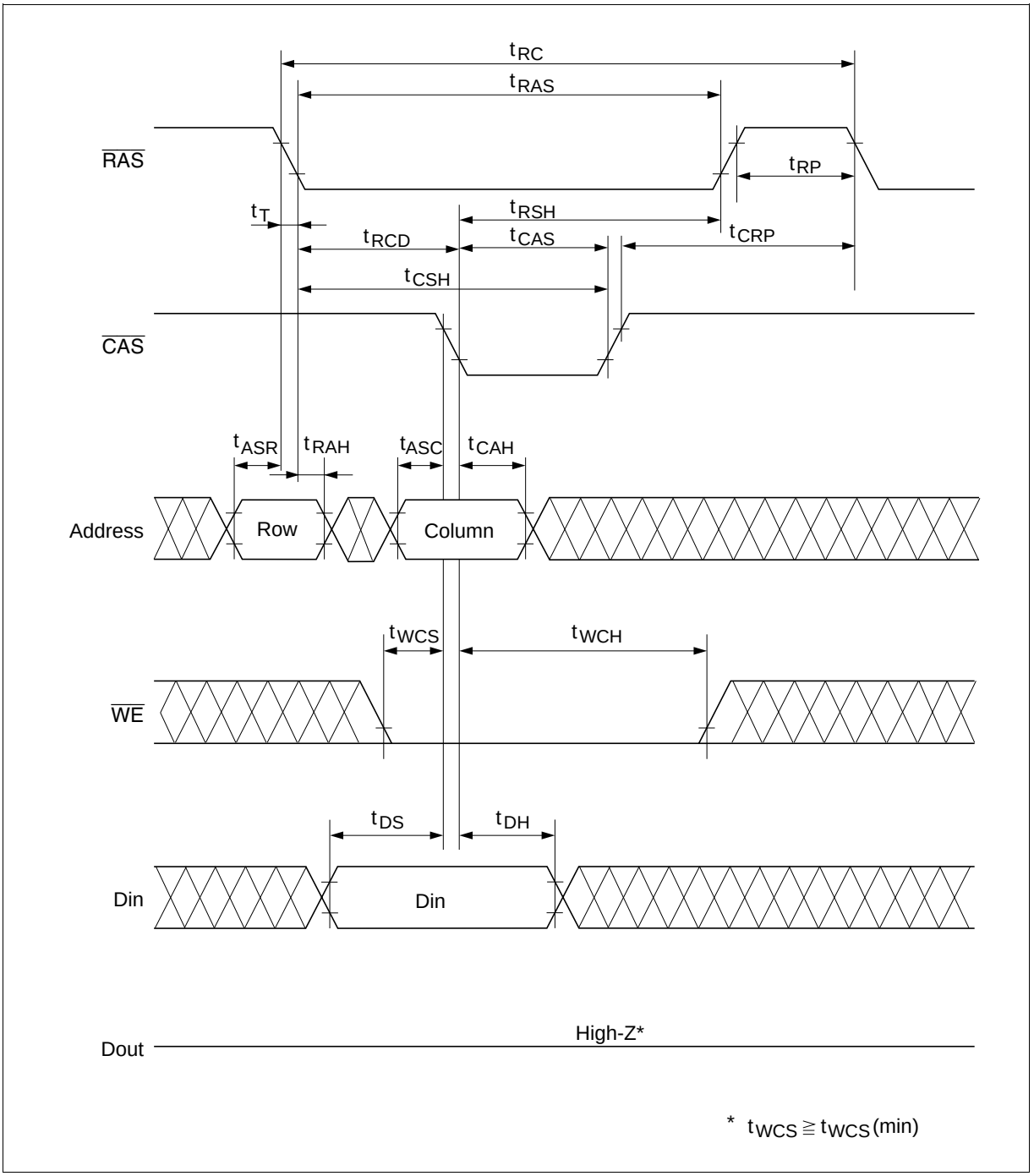
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

Timing Waveforms[*22]

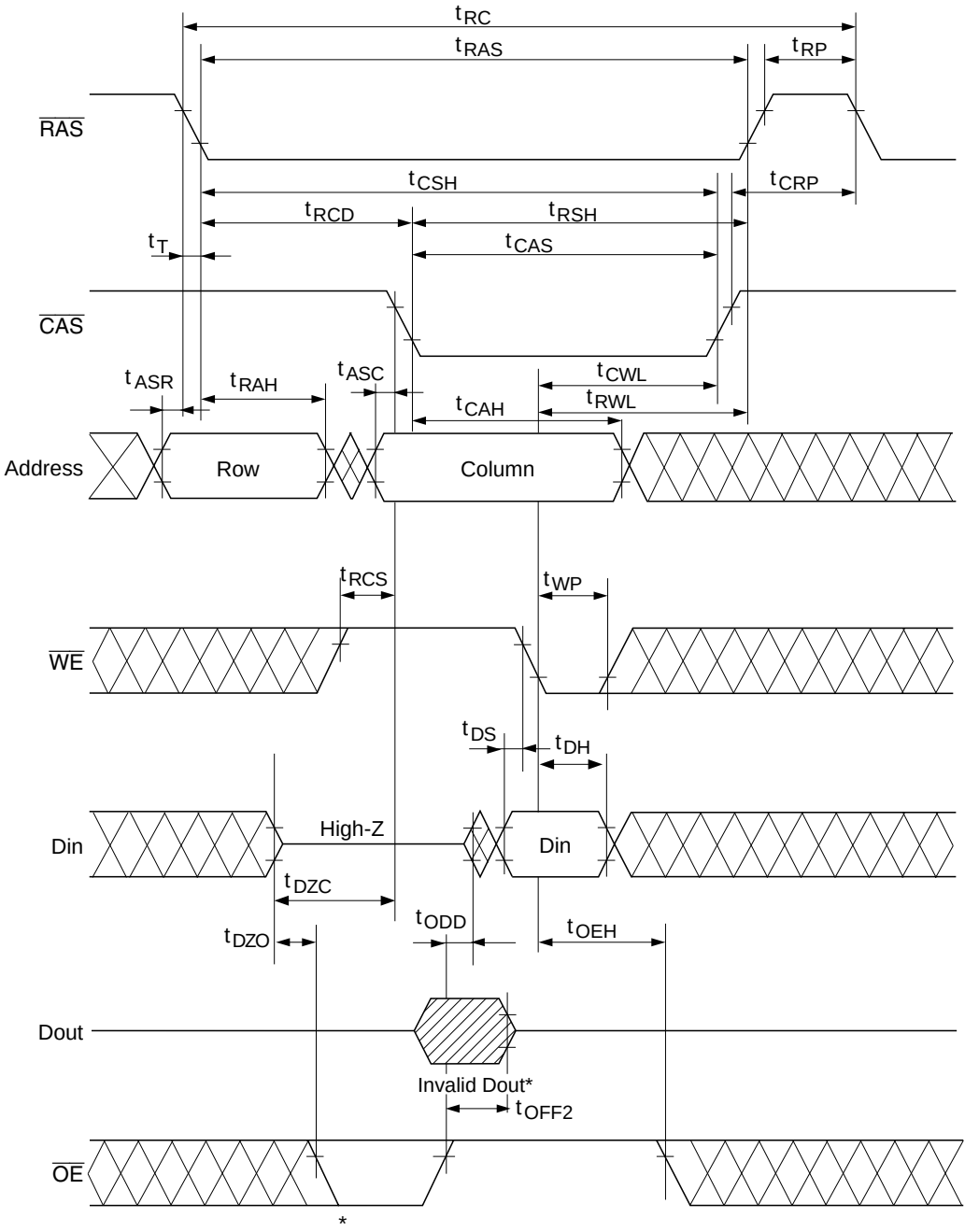
Read Cycle



Early Write Cycle

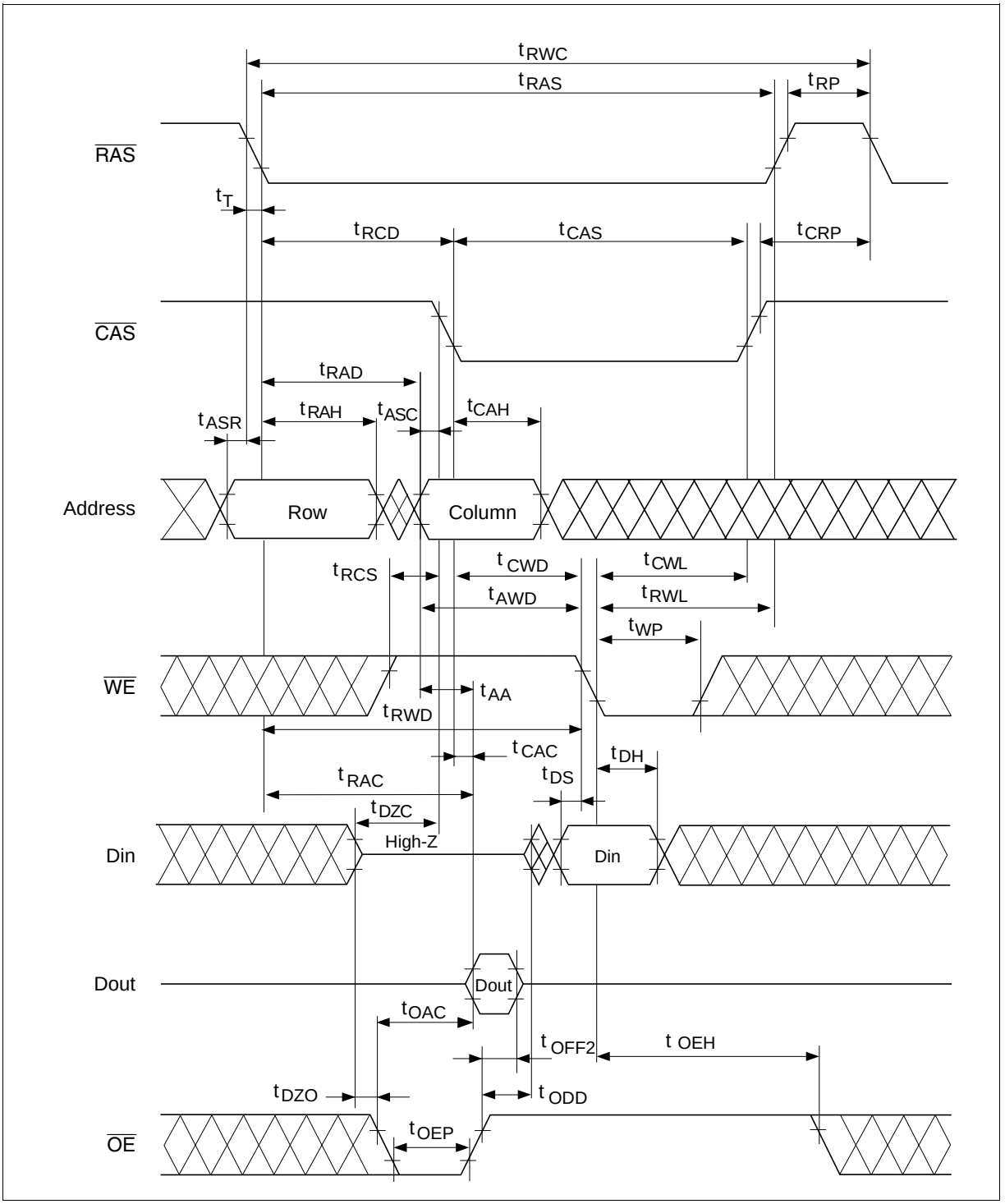


Delayed Write Cycle

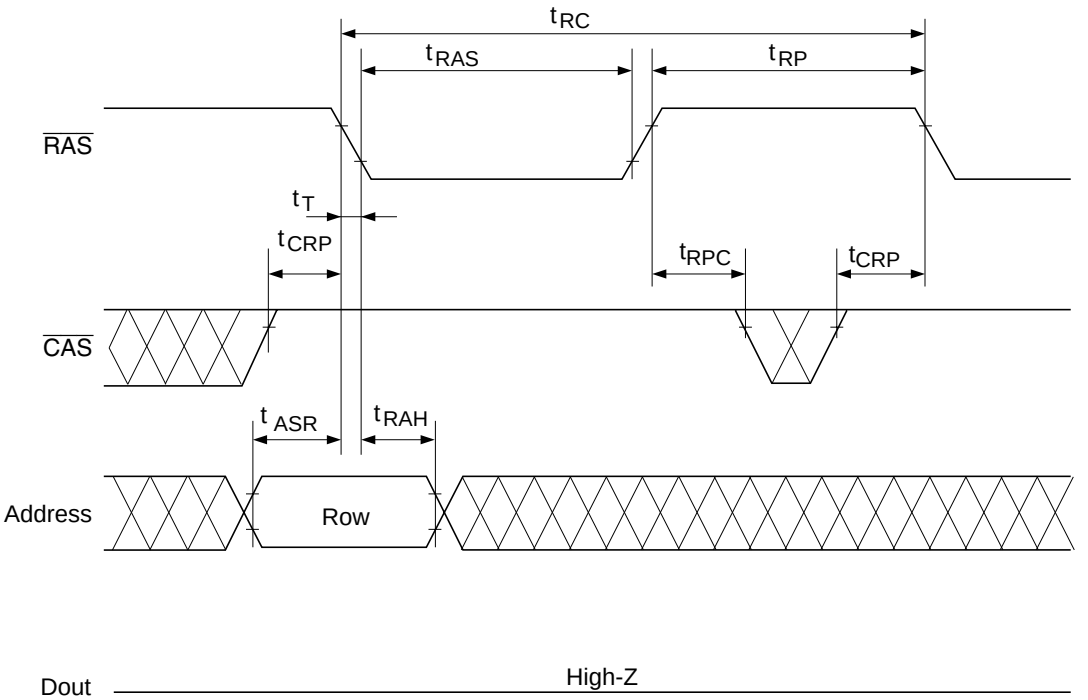


* Invalid Dout comes out, when $\overline{OE}$ is low level.

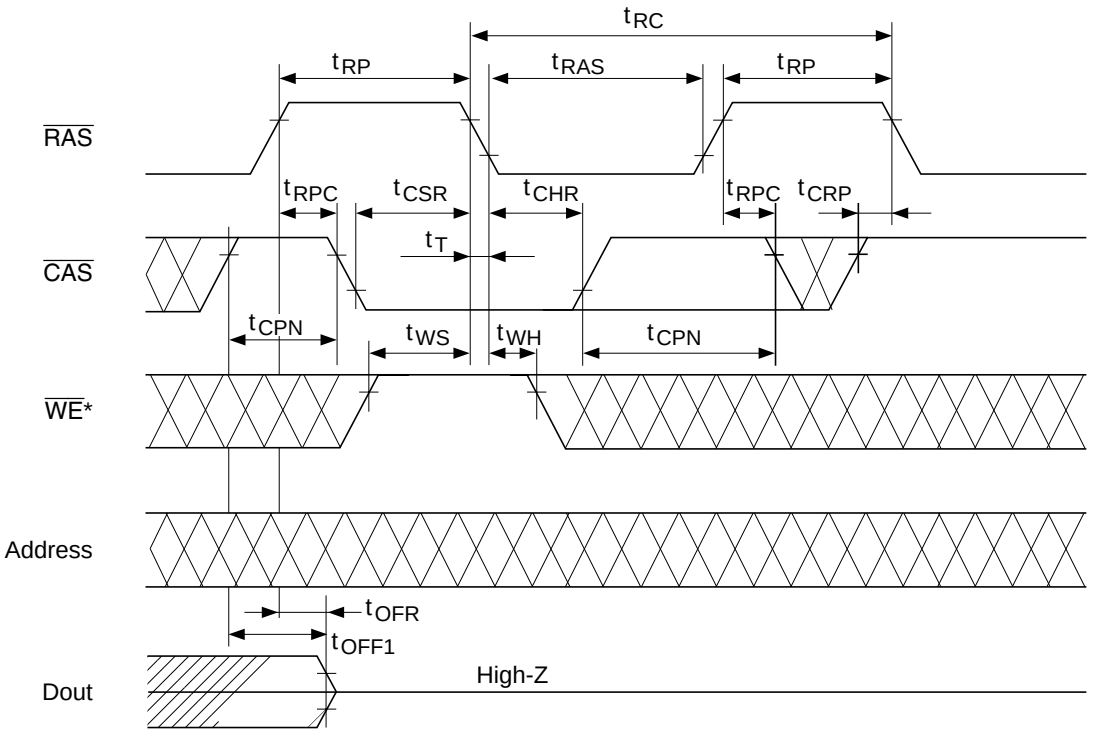
Read-Modify-Write Cycle



$\overline{\text{RAS}}$-Only Refresh Cycle

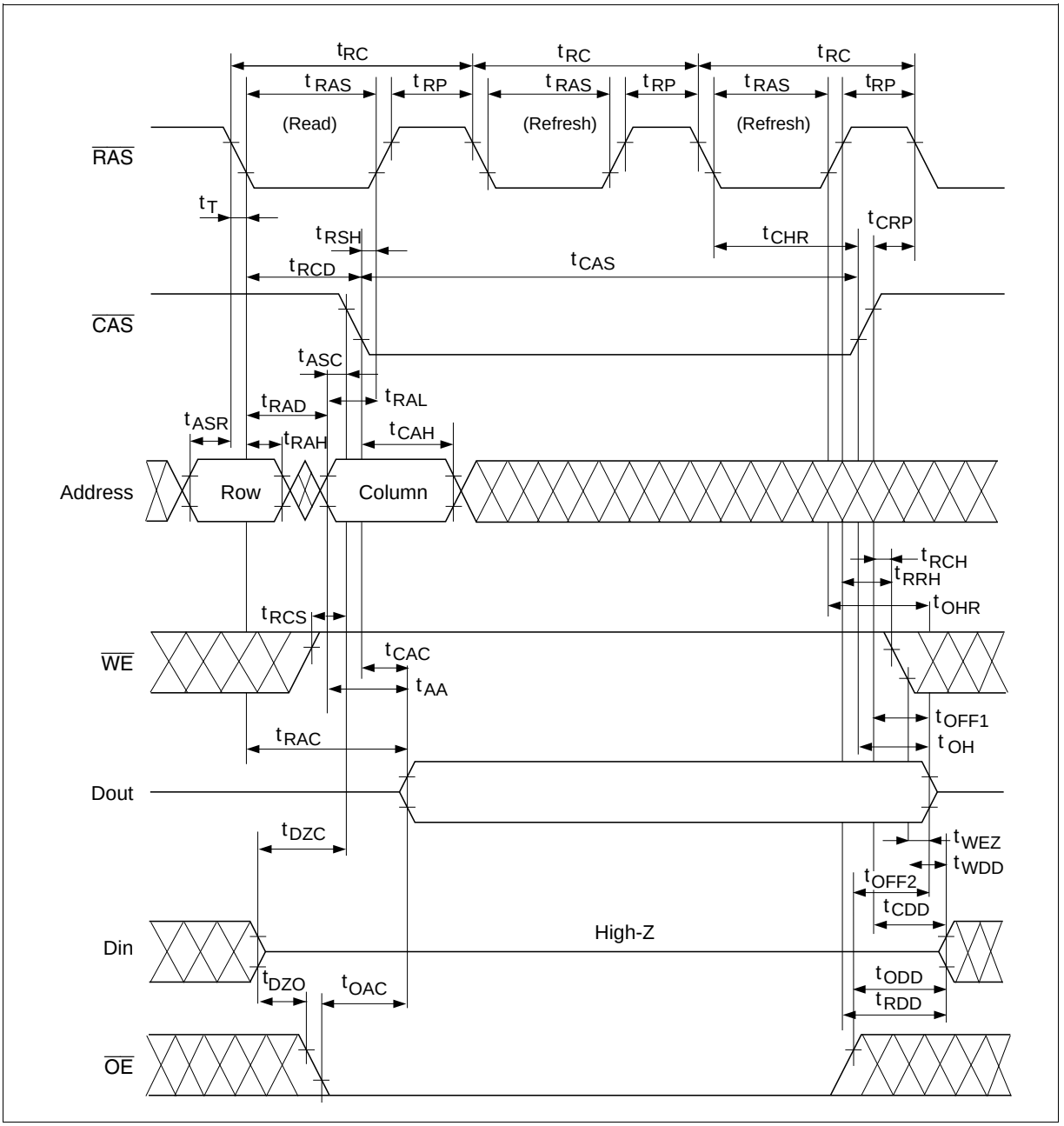


$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle

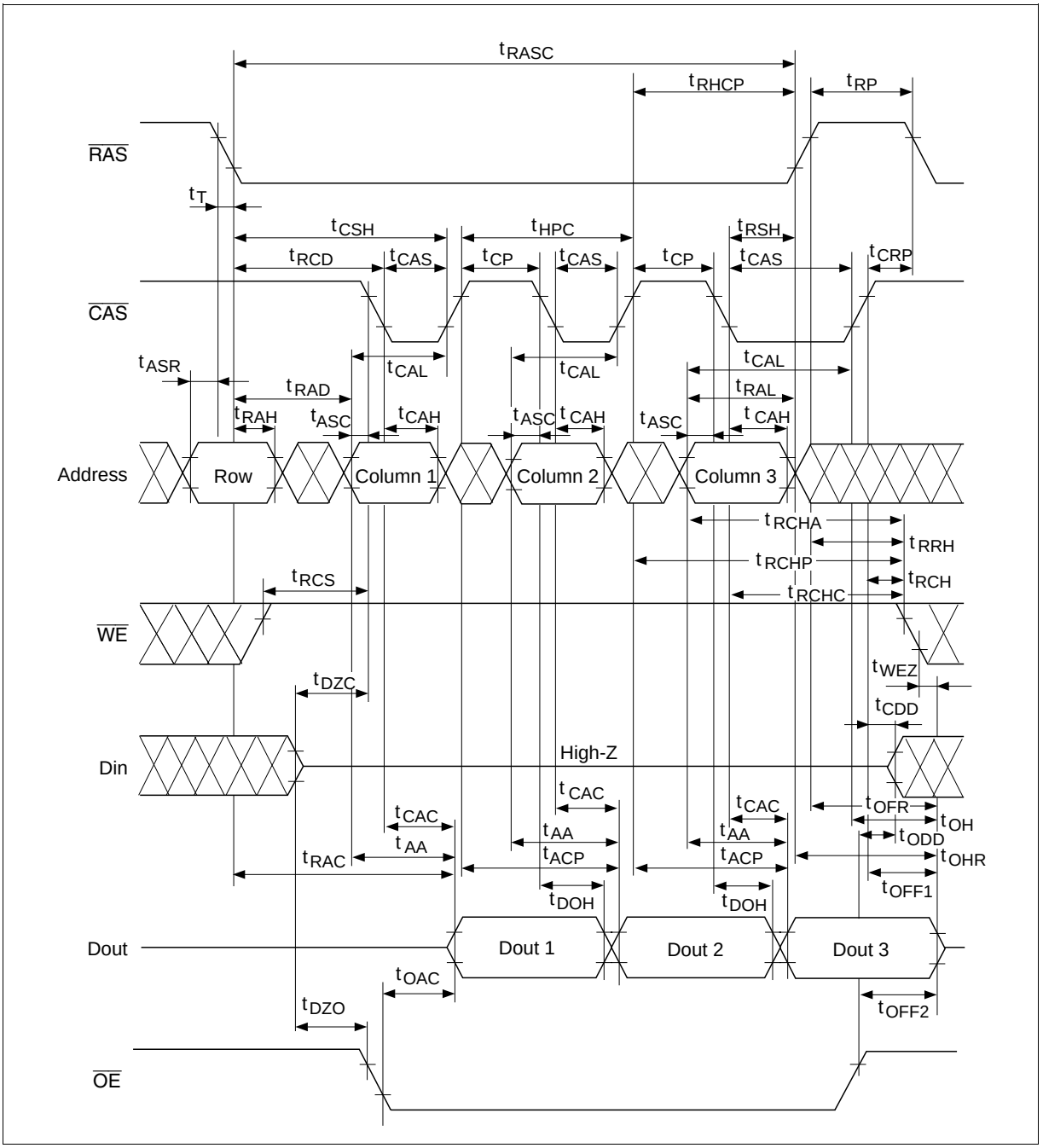


* t_{WS} and t_{WH} must be satisfied while $\overline{\text{CAS}}$ = V_{IL}.

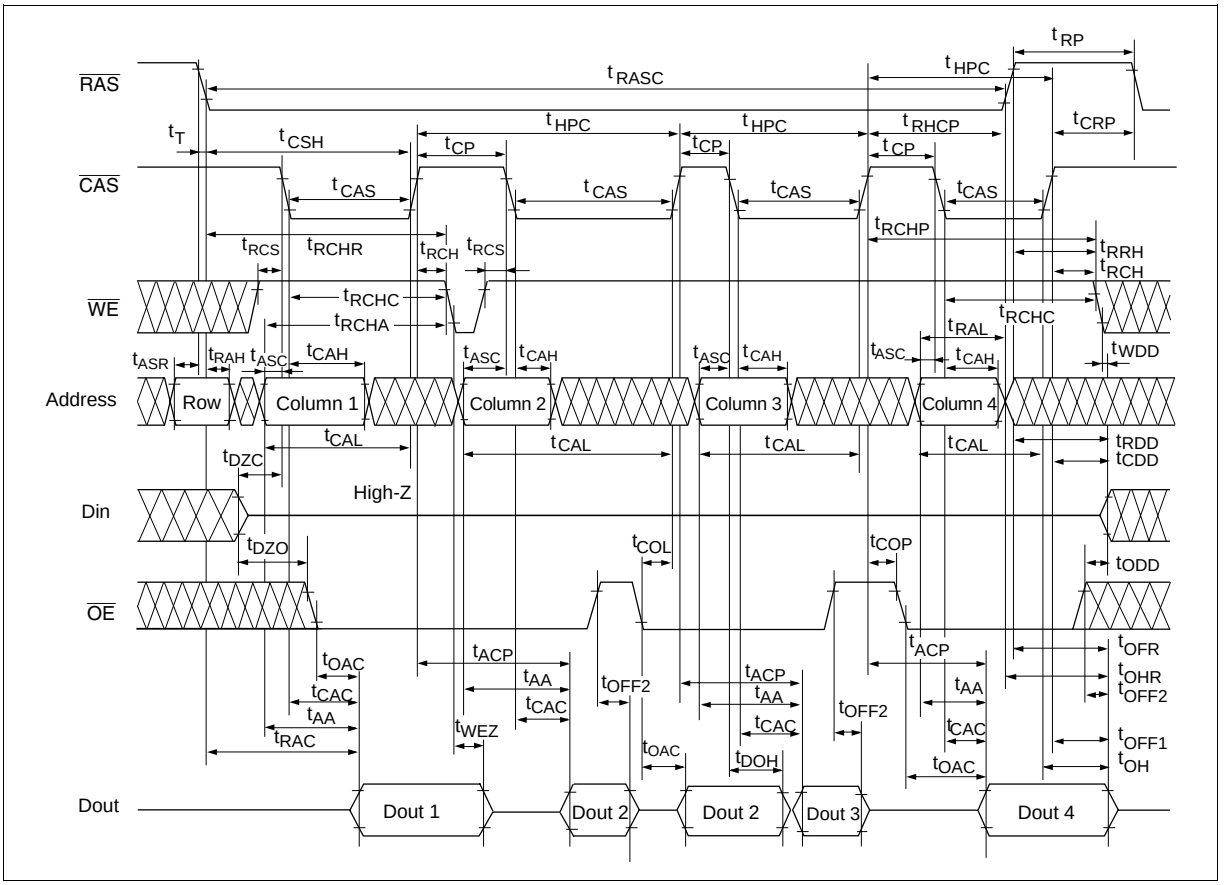
Hidden Refresh Cycle



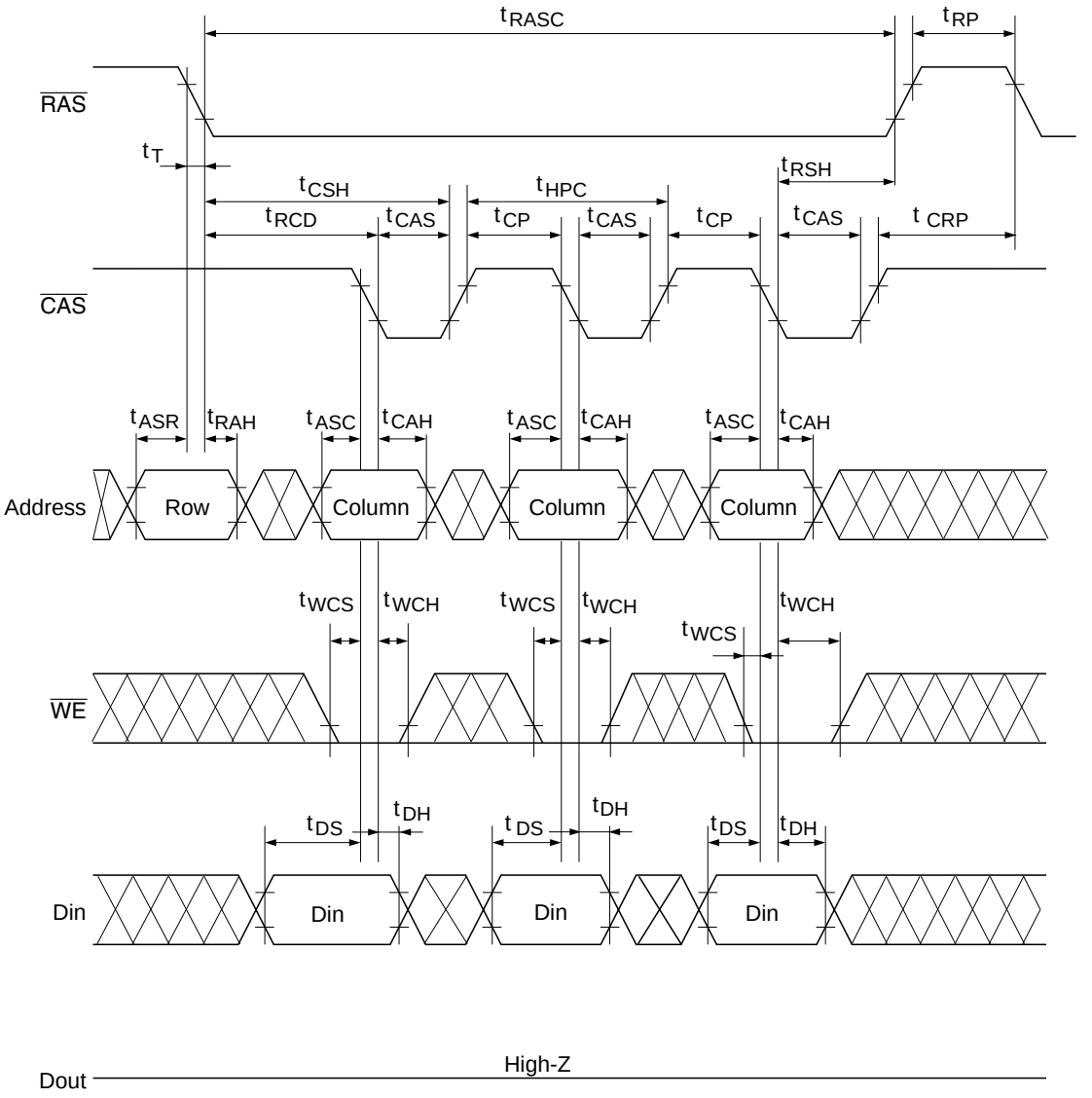
EDO Page Mode Read Cycle (t_{HPC} minimum cycle operation)



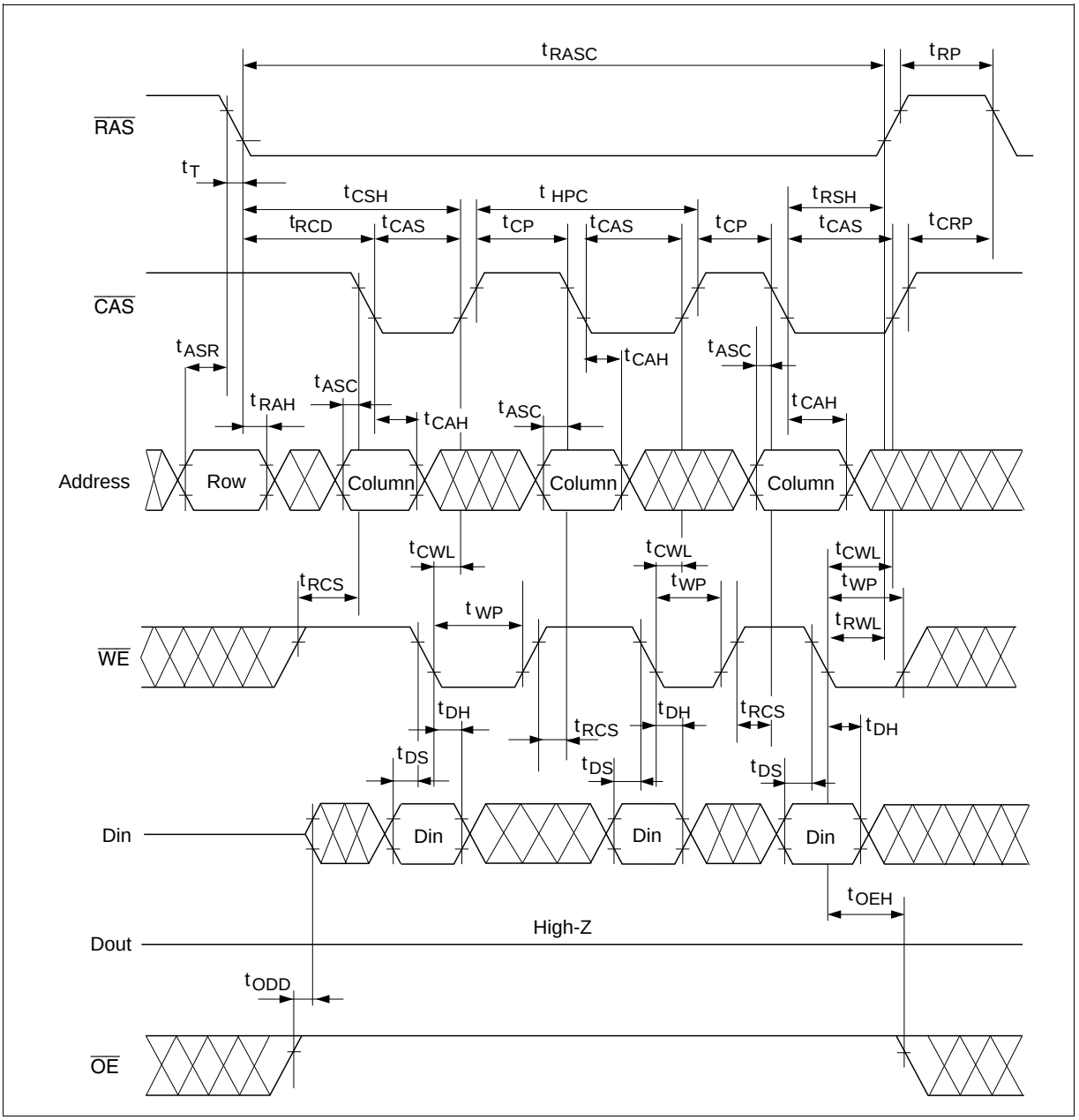
EDO Page Mode Read Cycle (High-Z control by $\overline{WE}$ and $\overline{OE}$)



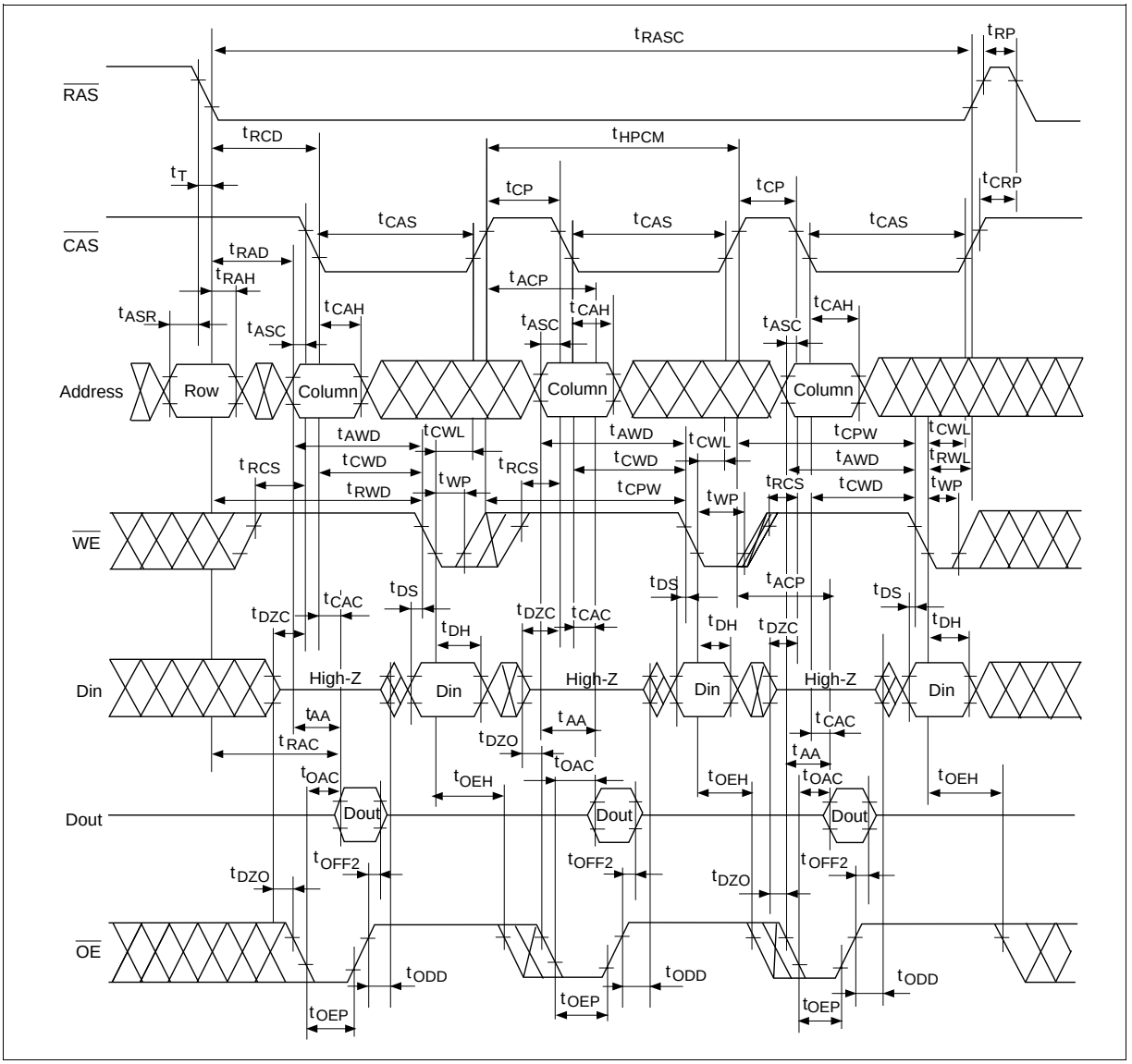
EDO Page Mode Early Write Cycle (t_{HPC} minimum cycle operation)



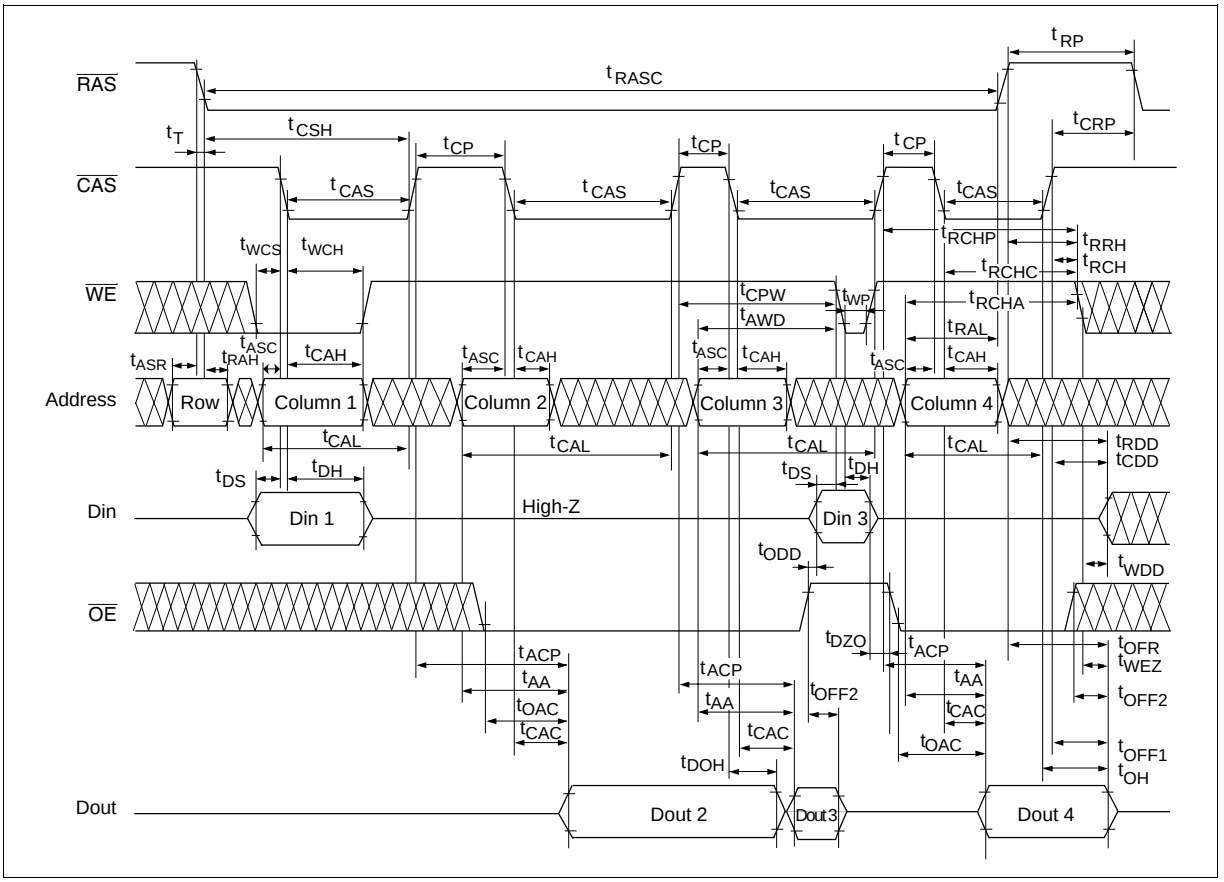
EDO Page Mode Delayed Write Cycle



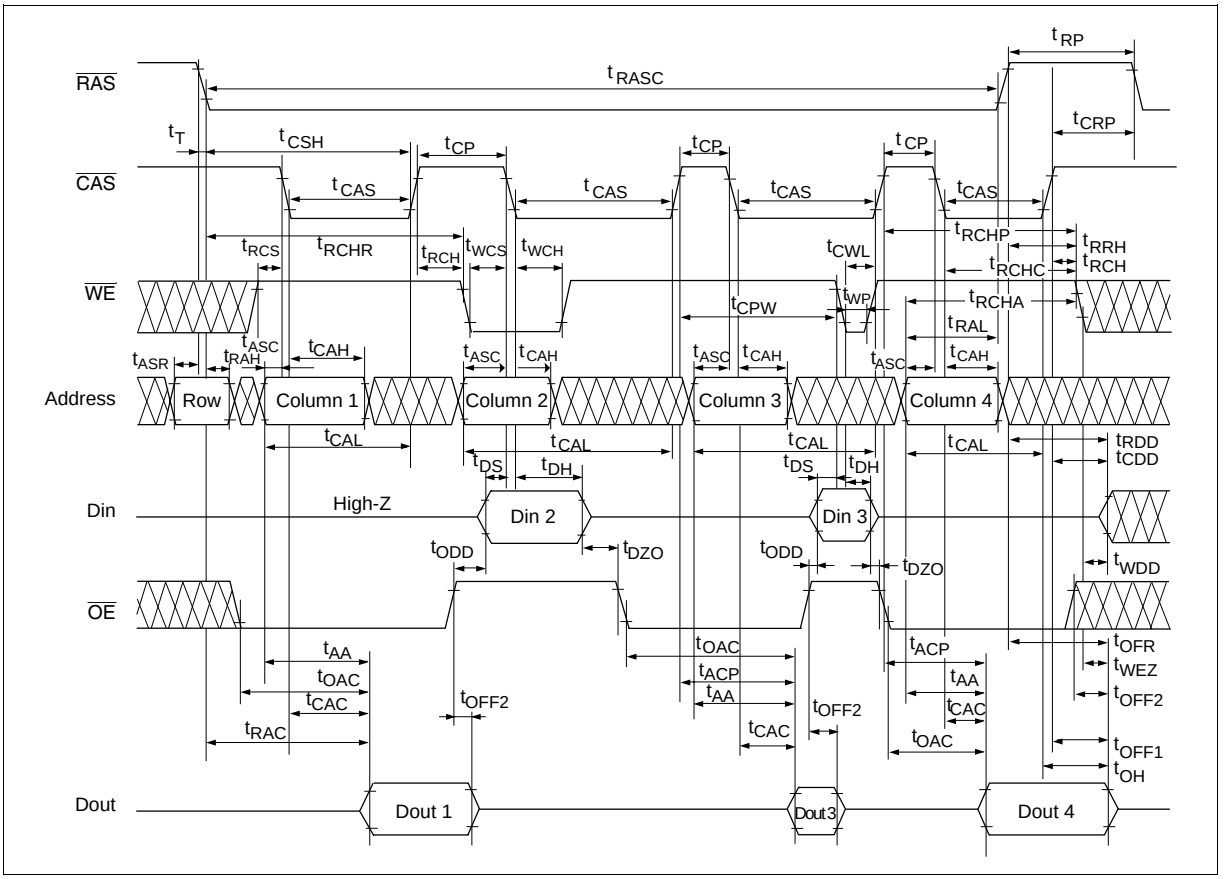
EDO Page Mode Read-Modify-Write Cycle



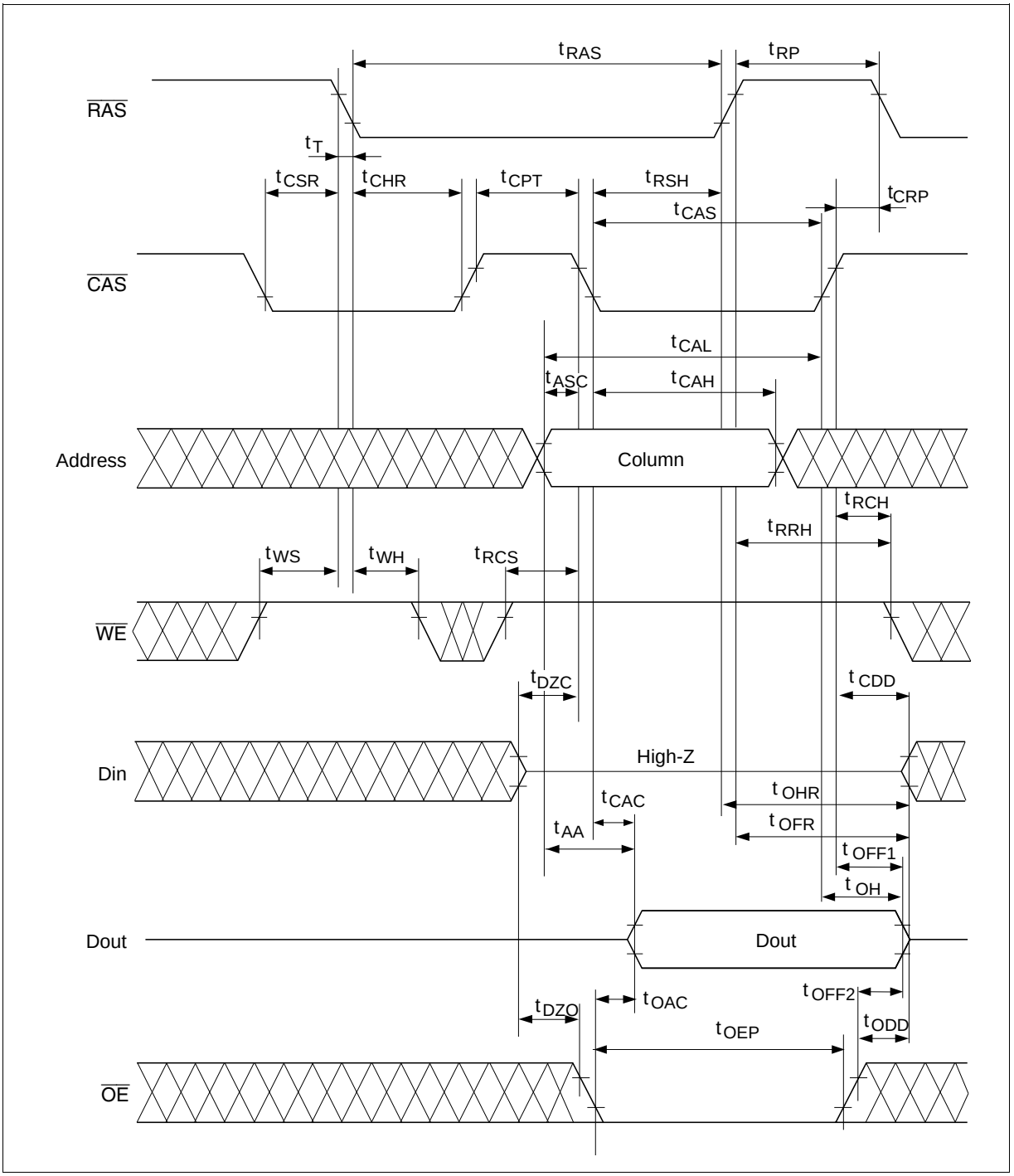
EDO Page Mode Mix Cycle (1)[*20]



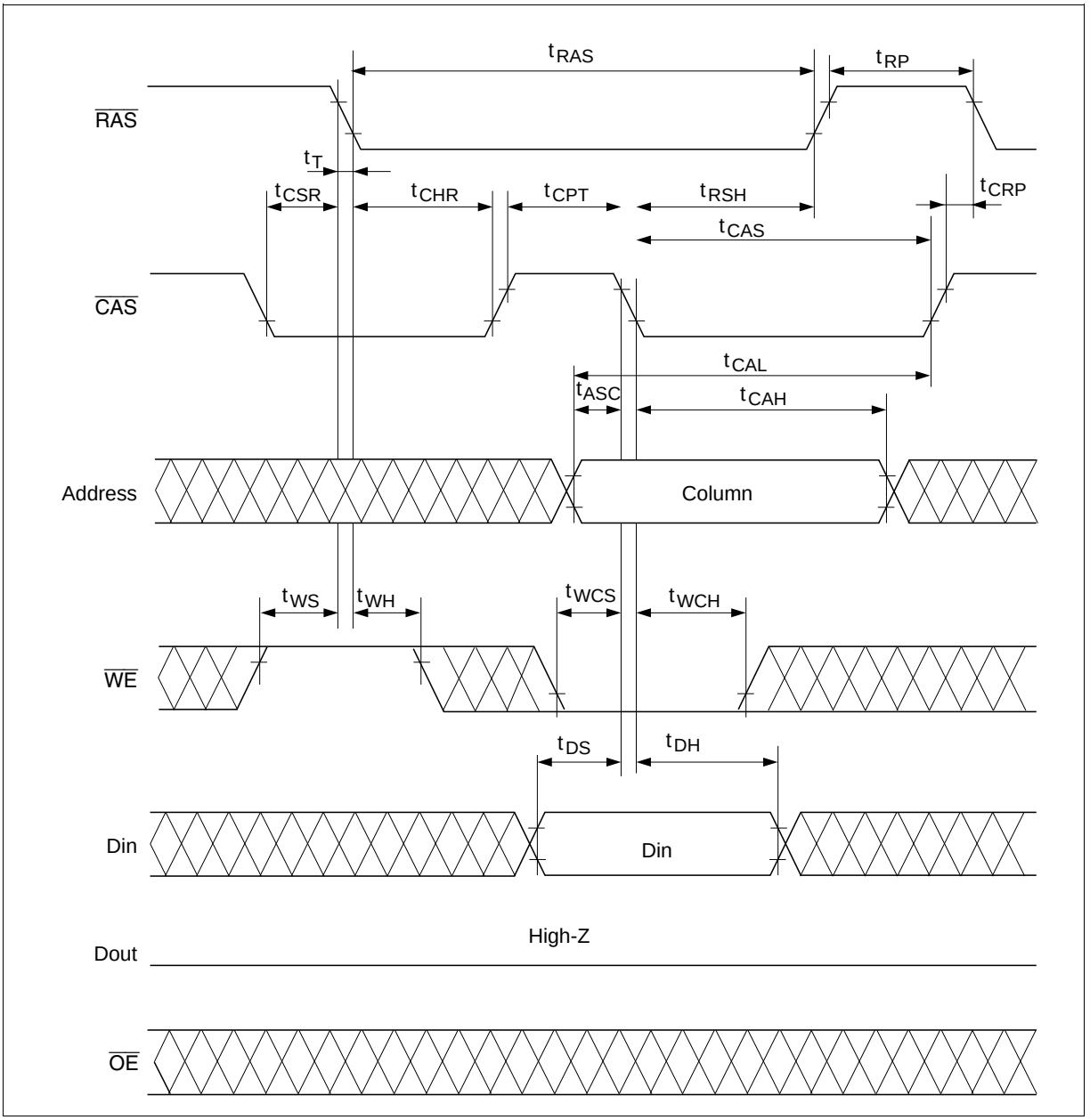
EDO Page Mode Mix Cycle (2) [*20]



$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Counter Check Cycle (Read)

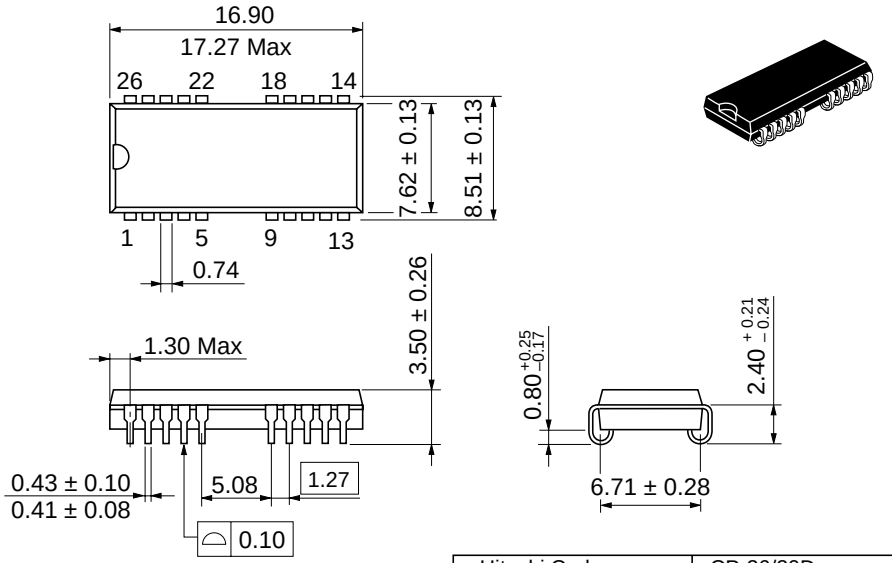


$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Counter Check Cycle (Write)



Package Dimensions

HM51W4405BS Series (CP-26/20D) Unit: mm



Hitachi Code	CP-26/20D
JEDEC Code	MO-077-AA
EIAJ Code	SC-633A
Weight	0.6 g

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Nov. 29, 1996	Initial issue		