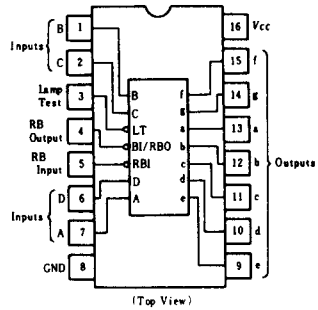
HD74LS248 ●BCD-to-Seven-Segment Decoders/Drivers (internal pull-up outputs)

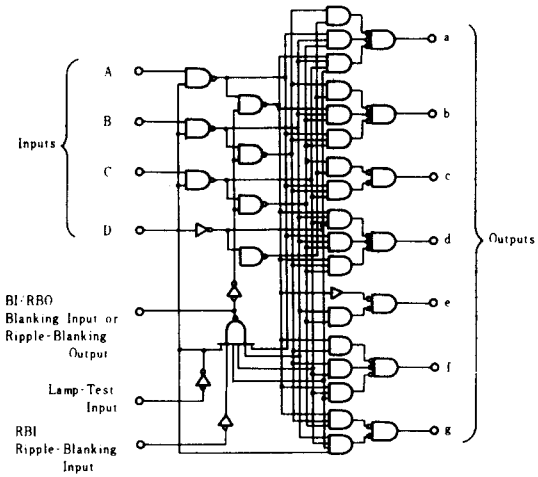
The HD74LS248 is electrically and functionally identical to the HD74LS48, respectively, and has the same pin assignments as its equivalents. It can be used interchangeably in present or future designs to offer designers a choice between two indicator fonts. The HD74LS48 composes the 6 and the 9 without tails and the HD74LS248 composes the 6 and the 9 with tails. Composition of all other characters, including display patterns for BCD inputs above nine, is identical. The HD74LS248 features active-low outputs designed for driving indicators directly. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions. This circuit incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO).

Lamp test (LT) of this type may be performed at any time when the BI/RBO node is at a high level. This type contains an overriding blanking input (BI) which can be used to control the lamp intensity be pulsing or to inhibit the outputs.

■PIN ARRANGEMENT

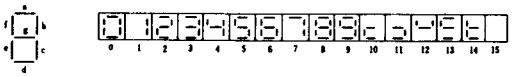


■BLOCK DIAGRAM



■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Output current	a~g	I_{OH}	–	–	−100	μA
	BI/RBO		–	–	−50	
	a~g	I_{OL}	–	–	6	mA
	BI/RBO		–	–	3.2	



■FUNTION TABLE

Decimal or Function	Inputs						BI/RBO	Outputs							Note
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	×	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	×	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	×	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	×	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	×	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	×	L	H	H	L	H	H	L	H	H	H	H	H	
7	H	×	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	×	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	×	H	L	L	H	H	H	H	H	H	L	H	H	
10	H	×	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	×	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	×	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	×	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	×	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	×	H	H	H	H	H	L	L	L	L	L	L	L	
BI	×	×	×	×	×	×	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	×	×	×	×	×	H	H	H	H	H	H	H	H	4

H; high level, L; low level, X; irrelevant

Notes: 1. The blanking input (BI) must be open or held at a high-logic level when output functions 0 through 15 are desired.
2. When a low logic level is applied directly to the blanking input.
3. When ripple-blanking input (RBI) and inputs A B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When a blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	–	–	V
		V_{IL}			–	–	0.8	V
Output voltage	a~g	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$	$I_{OH}=-100\mu A$	2.4	–	–	V
	BI/RBO		$V_{IL}=0.8V$	$I_{OH}=-50\mu A$				
Output current**	a~g	I_O	$V_{CC}=4.75V$, $V_O=0.85V$		−1.3	–	–	mA
Output voltage	a~g	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$	$I_{OL}=2mA$	–	–	0.4	V
				$I_{OL}=6mA$	–	–	0.5	
	BI/RBO		$V_{IL}=0.8V$	$I_{OL}=1.6mA$	–	–	0.4	
				$I_{OL}=3.2mA$	–	–	0.5	
Input current	except BI/RBO	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	except BI/RBO	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	mA
	BI/RBO				–	–	−1.2	
	except BI/RBO	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	mA
Short-circuit output current	BI/RBO	I_{OS}	$V_{CC}=5.25V$		−0.3	–	−2	mA
Supply current***		I_{CC}	$V_{CC}=5.25V$		–	25	38	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

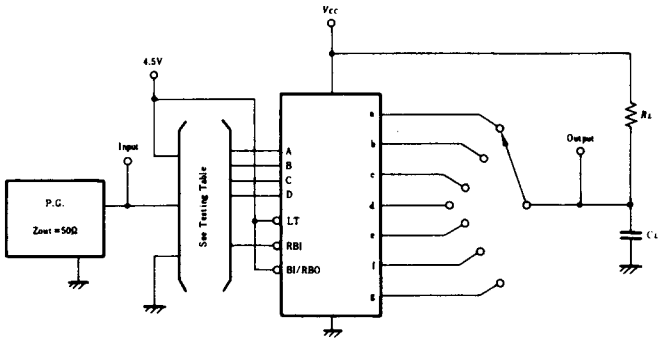
* V_{CC}=5V, Ta=25°C
** Input condition as for V_{OH}
*** I_{CC} is measured with all outputs open and all inputs at 4.5V.

■SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃)

Item	Symbol	Input	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	A	C_L=15pF, R_L=4kΩ	–	–	100	ns
	t_{PHL}			–	–	100	
	t_{PLH}	RBI	C_L=15pF, R_L=6kΩ	–	–	100	ns
	t_{PHL}			–	–	100	

■TESTING METHOD

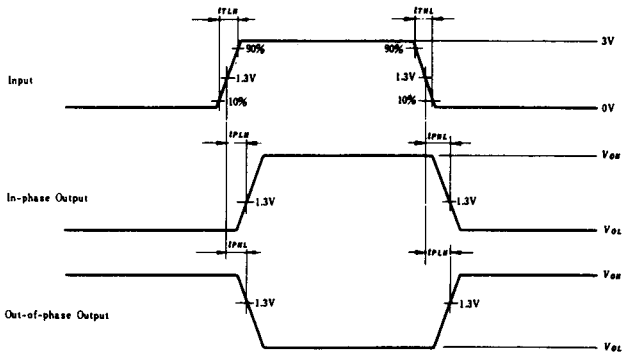
1) Test Circuit



2) Testing Table

Item	Inputs					Outputs						
	RBI	D	C	B	A	a	b	c	d	e	f	g
	4.5V	GND	GND	GND	IN	OUT	–	–	OUT	OUT	OUT	–
t_{PLH}	4.5V	GND	GND	4.5V	IN	–	–	OUT	–	OUT	–	–
t_{PHL}	4.5V	GND	4.5V	4.5V	IN	–	OUT	–	OUT	OUT	OUT	OUT
	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	–

Waveform



Notes) 1. Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, PRR=1MHz, duty cycle=50%
2. C_L includes probe and jig capacitance.

PACKAGING INFORMATIONS

T-90-20

Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

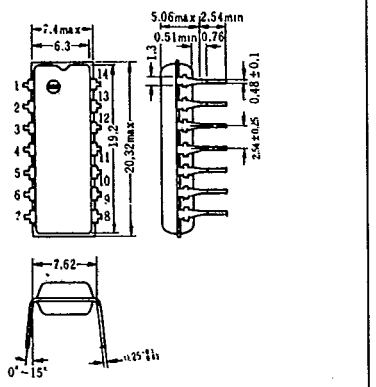
HD 74LS00 P

- Package ; Plastic DIP ; letters P
  Cerdip ; non-letters
- Circuit description
- Prefix : HD ; Hitachi Digital IC

■Plastic DIP

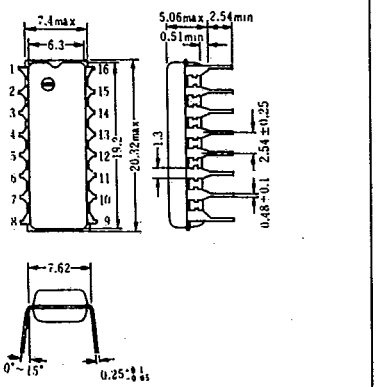
●14 Pin

DP-14



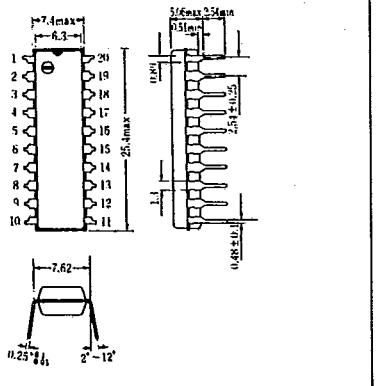
●16 Pin

DP-16



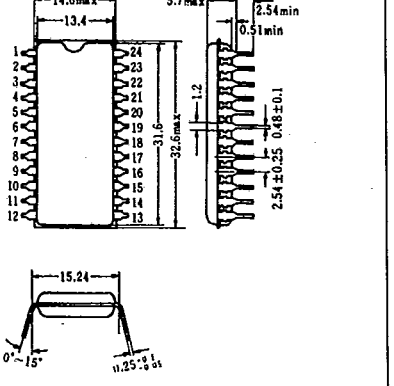
●20 Pin

DP-20



●24 Pin

DP-24

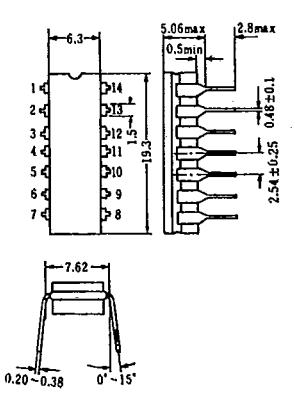


PACKAGING INFORMATIONS

■Cerdip

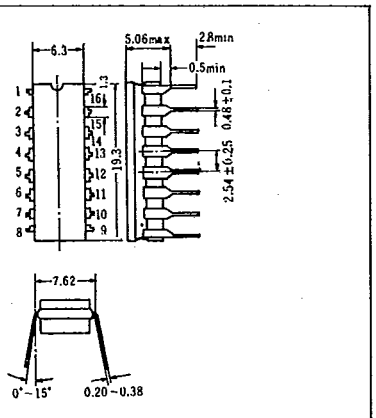
●14 Pin

DG-14



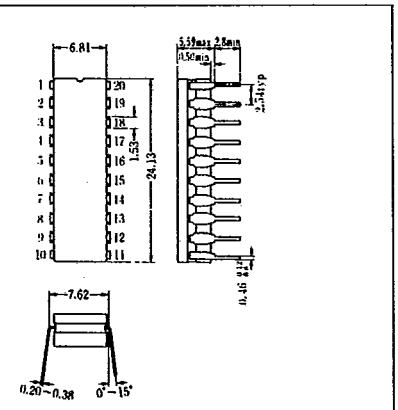
●16 Pin

DG-16



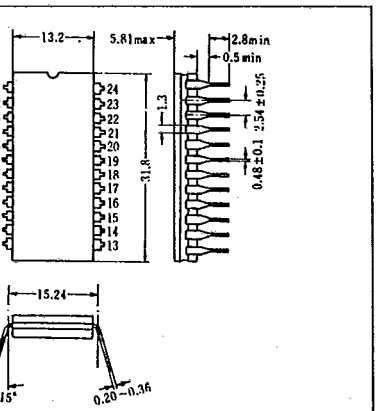
●20 Pin

DG-20



●24 Pin

DG-24



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