**FAIRCHILD**

SEMICONDUCTOR ™

FDP4030L / FDB4030L
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC/DC converters and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 20 A, 30 V. $R_{DS(ON)}$ = 0.035 Ω @ V_{GS}=10 V
  $R_{DS(ON)}$ = 0.055 Ω @ V_{GS}=4.5V.

- Critical DC electrical parameters specified at elevated temperature.

- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.

- High density cell design for extremely low $R_{DS(ON)}$.

- 175°C maximum junction temperature rating.

TO-220
FDP Series

TO-263AB
FDB Series
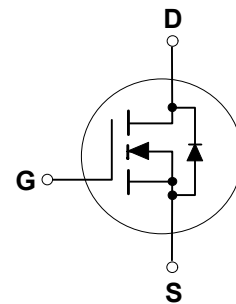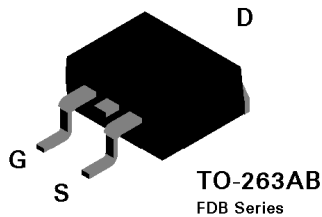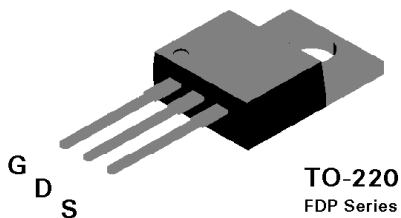
Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	FDP4030L	FDB4030L	Units
V_{DSS}	Drain-Source Voltage	30		V
V_{GSS}	Gate-Source Voltage	±20		V
I_D	Drain Current - Continuous (Note 1)	20		A
	- Pulsed (Note 1)	60		
P_D	Total Power Dissipation @ T_C = 25°C	37.5		W
	Derate above 25°C	0.25		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C
THERMAL CHARACTERISTICS				
$R_{θJC}$	Thermal Resistance, Junction-to-Case	4		°C/W
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient	62.5		°C/W

Electrical Characteristics (T$_C$ = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
OFF CHARACTERISTICS						
W$_{DSS}$	Single Pulse Drain-Source Avalanche Energy	V$_{DD}$ = 15 V, I$_D$ = 7 A			50	mJ
I$_{AR}$	Maximum Drain-Source Avalanche Current				7	A
BV$_{DSS}$	Drain-Source Breakdown Voltage	V$_{GS}$ = 0 V, I$_D$ = 250 µA	30			V
ΔBV$_{DSS}$/ΔT$_J$	Breakdown Voltage Temp. Coefficient	I$_D$ = 250 µA, Referenced to 25°C		33		mV/°C
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$ = 24 V, V$_{GS}$ = 0 V			10	µA
		T$_J$ = 125°C			1	mA
I$_{GSSF}$	Gate - Body Leakage, Forward	V$_{GS}$ = 20 V, V$_{DS}$ = 0 V			100	nA
I$_{GSSR}$	Gate - Body Leakage, Reverse	V$_{GS}$ = -20 V, V$_{DS}$ = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$ = V$_{GS}$, I$_D$ = 250 µA	1	1.6	2	V
ΔV$_{GS(th)}$/ΔT$_J$	Gate Threshold Voltage Temp. Coefficient	I$_D$ = 250 µA, Referenced to 25°C		-4.1		mV/°C
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$ = 10 V, I$_D$ = 10 A		0.025	0.035	Ω
		T$_J$ = 125°C		0.048	0.06	
		V$_{GS}$ = 10 V, I$_D$ = 4.5 A		0.046	0.055	
I$_{D(on)}$	On-State Drain Current	V$_{GS}$ = 10 V, V$_{DS}$ = 10 V	30			A
g$_{FS}$	Forward Transconductance	V$_{DS}$ = 10 V, I$_D$ = 10 A		11		S
DYNAMIC CHARACTERISTICS						
C$_{iss}$	Input Capacitance	V$_{DS}$ = 15 V, V$_{GS}$ = 0 V, f = 1.0 MHz		365		pF
C$_{oss}$	Output Capacitance			210		pF
C$_{rss}$	Reverse Transfer Capacitance			70		pF
SWITCHING CHARACTERISTICS (Note 1)						
t$_{D(on)}$	Turn - On Delay Time	V$_{DD}$ = 15 V, I$_D$ = 10 A, V$_{GS}$ = 10 V, R$_{GEN}$ = 10 Ω		8	15	nS
t$_r$	Turn - On Rise Time			8	15	nS
t$_{D(off)}$	Turn - Off Delay Time			20	40	nS
t$_f$	Turn - Off Fall Time			10	20	nS
Q$_g$	Total Gate Charge	V$_{DS}$ = 24 V, I$_D$ = 10 A, V$_{GS}$ = 10 V		13	18	nC
Q$_{gs}$	Gate-Source Charge			2		nC
Q$_{gd}$	Gate-Drain Charge			4		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
I$_S$	Maximum Continuos Drain-Source Diode Forward Current				20	A
I$_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current				60	A
V$_{SD}$	Drain-Source Diode Forward Voltage	V$_{GS}$ = 0 V, I$_S$ = 10 A (Note 1)		1.12	1.3	V
		T$_J$ = 125°C		1.08	1.2	

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

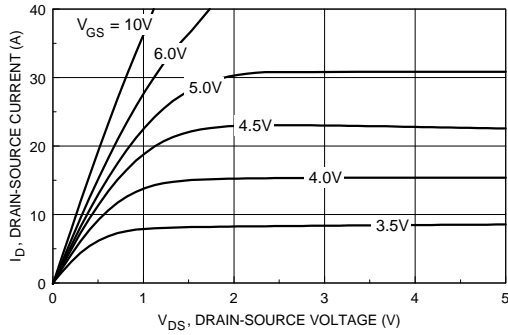# Typical Electrical Characteristics

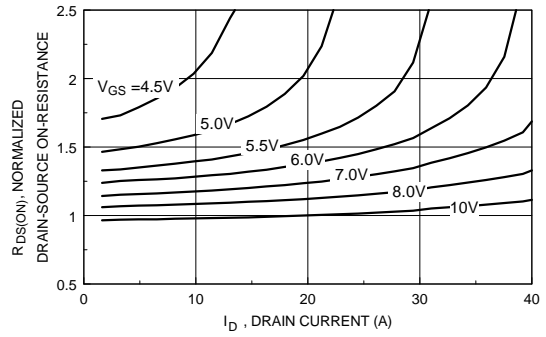**Figure 1. On-Region Characteristics.**

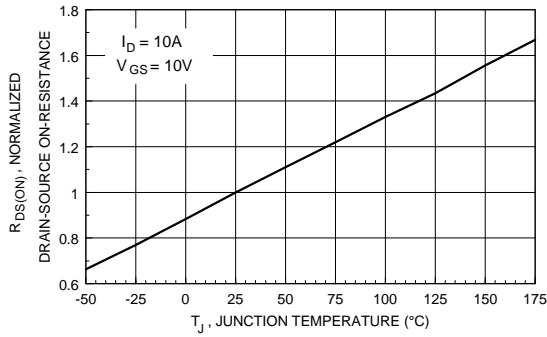**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

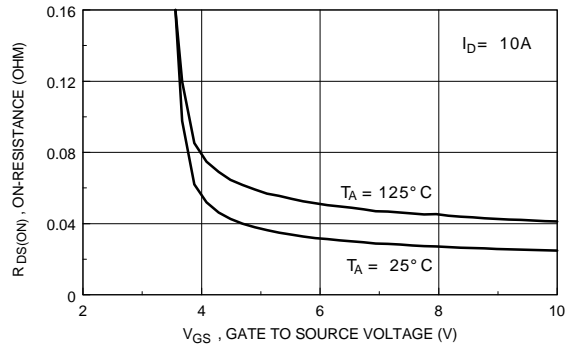**Figure 3. On-Resistance Variation with Temperature.**

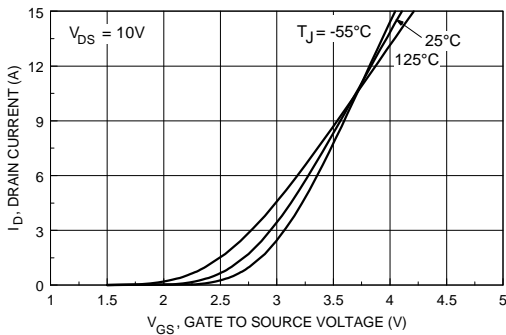**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

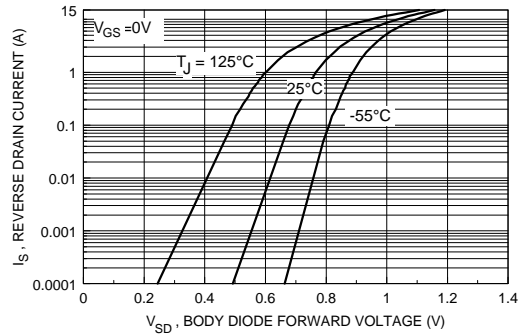**Figure 5. Transfer Characteristics.**

Figure 6 . Body Diode Forward Voltage Variation with Source Current and Temperature.

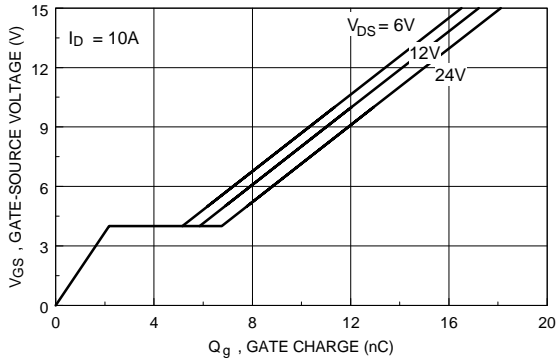# Typical Electrical Characteristics (continued)

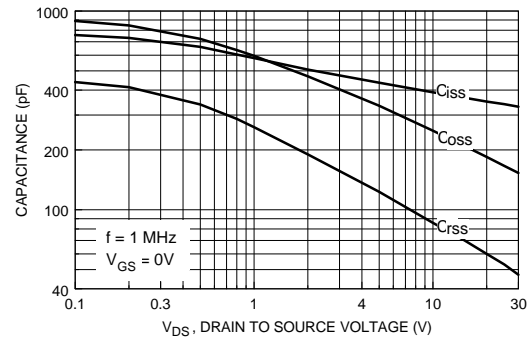
Figure 7. Gate Charge Characteristics.

Figure 8. Capacitance Characteristics.

EFFECTIVE
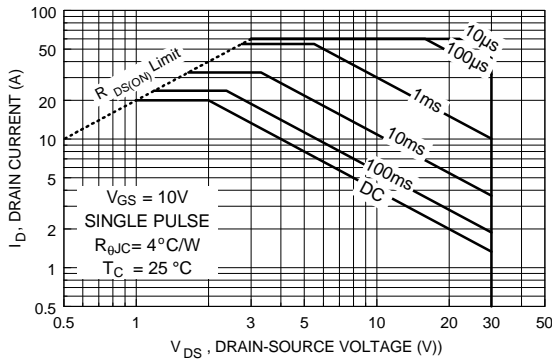
Figure 9. Maximum Safe Operating Area.

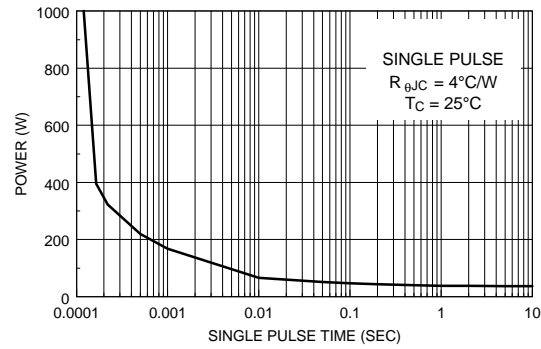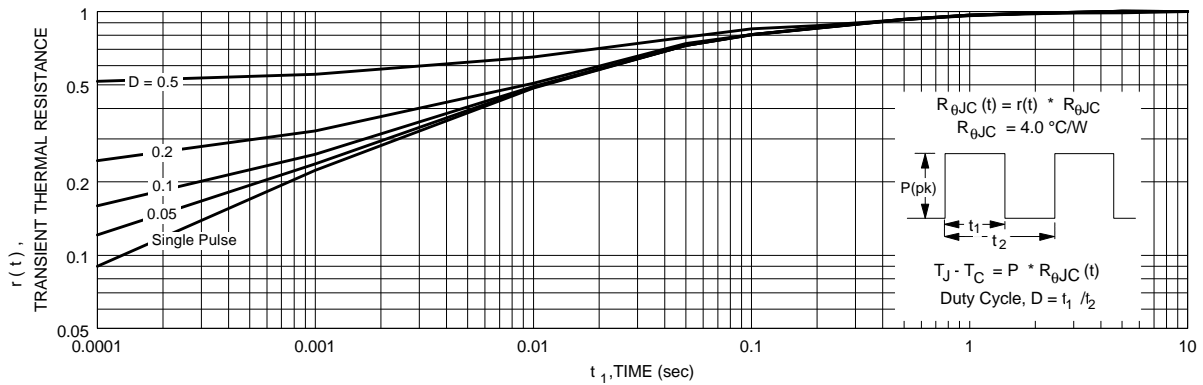Figure 10. Single Pulse Maximum Power
Dissipation.

NORMALIZED

$$R_{\theta JC}(t) = r(t) * R_{\theta JC}$$
$$R_{\theta JC} = 4.0 \text{ °C/W}$$

$$T_J - T_C = P * R_{\theta JC}(t)$$
Duty Cycle, $D = t_1/t_2$

Figure 11. Transient Thermal Response Curve.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST ®	OPTOLOGIC™	SMART START™	VCX™
Bottomless™	FASTr™	OPTOPLANAR™	STAR*POWER™	
CoolFET™	FRFET™	PACMAN™	Stealth™	
CROSSVOLT™	GlobalOptoisolator™	POP™	SuperSOT™-3	
DenseTrench™	GTO™	Power247™	SuperSOT™-6	
DOME™	HiSeC™	PowerTrench®	SuperSOT™-8	
EcoSPARK™	ISOPLANAR™	QFET™	SyncFET™	
E²CMOS™	LittleFET™	QS™	TinyLogic™	
EnSigna™	MicroFET™	QT Optoelectronics™	TruTranslation™	
FACT™	MicroPak™	Quiet Series™	UHC™	
FACT Quiet Series™	MICROWIRE™	SILENT SWITCHER ®	UltraFET ®	

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. H4