

# M50197P, FP

SINGLE CHIP DIGITAL ECHO

## DESCRIPTION

The M50197P, FP is a single chip digital echo IC fabricated with silicon-gate CMOS technology.

The M50197P, FP converts an input analog signal and writes it external memory. After a delay it reads out the digital signal from memory and then converts to an analog signal again.

## FEATURES

- Includes an A-D D-A converter (Adaptive Delta Modulation), two low pass filters and a 20K-bit SRAM, making it possible to form a low cost digital delay system.
- Low noise, Low distortion  
 Surround mode: Noise(-90dBV typ), Distortion(0.3% typ)  
 Echo mode : Noise(-90dBV typ), Distortion(1.8% typ)
- Delay times : Surround mode...From 4.1 msec to 41 msec by 5 msec (eight steps)  
 Echo mode...From 20.5 msec to 163.8 msec (eight steps)
- Delay time and mode can be controlled by  $\mu$ -COM or manual setting
- Includes auto mute circuit, to protest sound from digital noise caused by delay time mode change or power
- Two control mode can be selected for delay time and mode setting, Easy mode contol by 4-bit parallel data and  $\mu$ -COM mode control by serial data
- Includes auto reset circuit

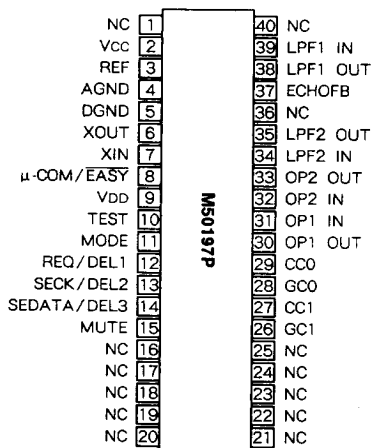
## APPLICATION

Karaoke, TV, VCR, Surround processor, Electronic instrument

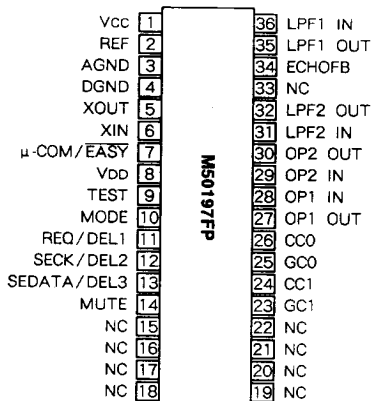
## RECOMMENDED OPERATING CONDITIONS

Supply voltage range.....4.5~5.5V  
 Rated supply voltage.....5V

## PIN CONFIGURATION (TOP VIEW)



Outline 40P4B

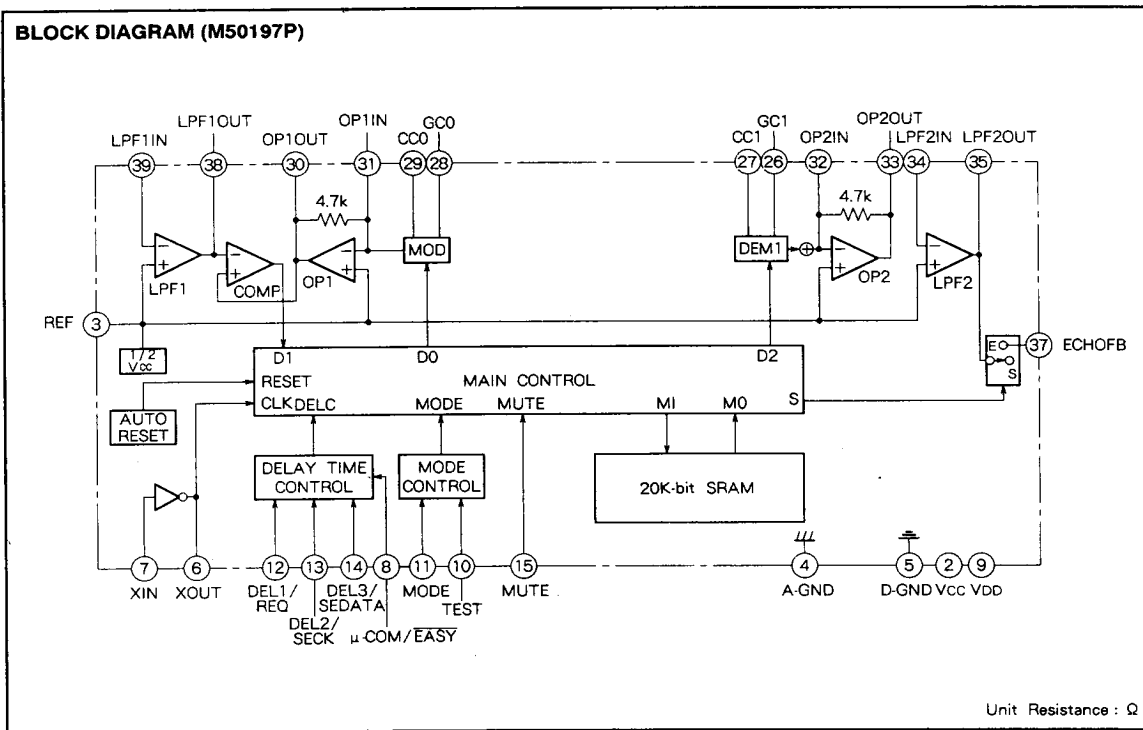


Outline 36P2R-A

NC : NO CONNECTION

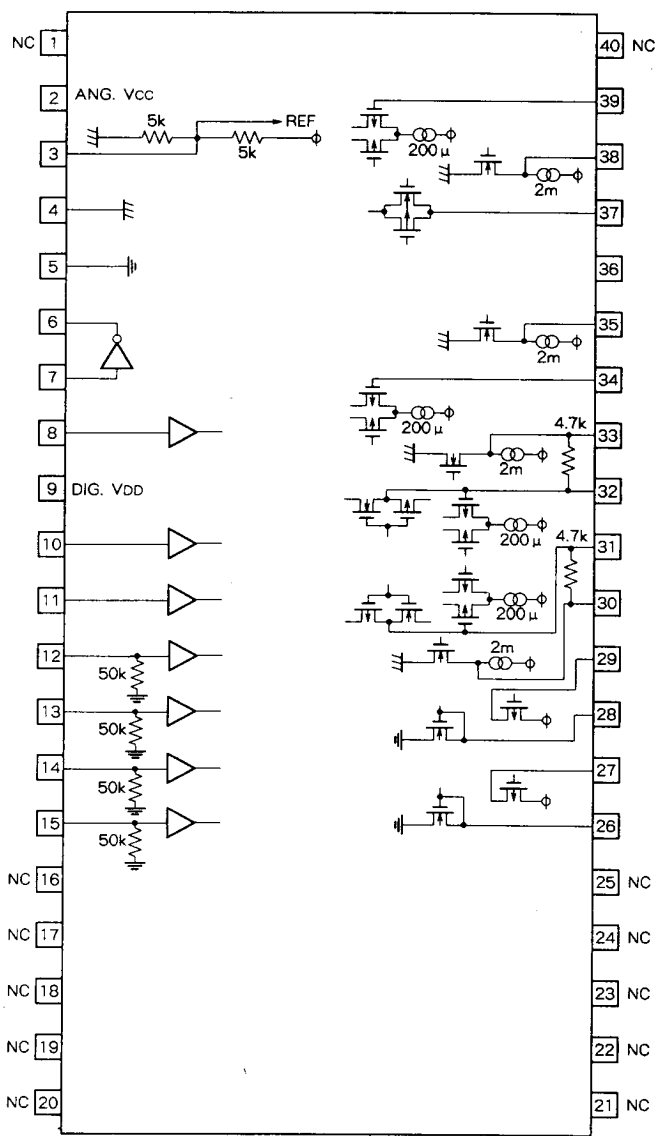







**BLOCK DIAGRAM (M50197P)**



Unit Resistance : Ω

M50197P I/O INTERFACE



-  CMOS INPUT BUFFER
-  Pch MOS Tr
-  Nch MOS Tr
-  DIG. GND
-  ANG. GND
- NC : NO CONNECTION
- Units Resistance : Ω
- Current : A

Note : Resistances and currents are typical values.

**M50197P,FP**

**SINGLE CHIP DIGITAL ECHO**

**ABSOLUTE MAXIMUM RATINGS** (Ta = 25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>cc</sub>	Supply voltage		6.5	V
I <sub>cc</sub>	Circuit current		150	mA
P <sub>d</sub>	Power dissipation		1.7	W
T <sub>opr</sub>	Operating temperature		-20~+75	°C
T <sub>stg</sub>	Storage temperature		-40~+125	°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V <sub>cc</sub>	Supply voltage		4.5	5	5.5	V
f <sub>ck</sub>	Clock frequency		3	4	6	MHz
V <sub>IH</sub>	High input voltage		0.7V <sub>DD</sub>			V
V <sub>IL</sub>	Low input voltage		0		0.3V <sub>DD</sub>	V

**ELECTRICAL CHARACTERISTICS** (V<sub>cc</sub> = 5V, f = 1kHz, V<sub>i</sub> = 100mV<sub>rms</sub>, f<sub>ck</sub> = 4MHz, Ta = 25 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I <sub>cc</sub>	Circuit current			65	100	mA
G <sub>v</sub>	Voltage gain	R <sub>L</sub> = 47k Ω	-3.5	-0.5	2.5	dB
V <sub>Omax</sub>	Maximum output voltage	THD = 10 %	0.7	1.4		V <sub>rms</sub>
THD	Output distortion	30kHz L.P.F	Echo mode	1.8	3	%
			Surround mode	0.3	1	
N <sub>o</sub>	Output noise voltage	DIN Audio	Echo mode	-90	-70	dBV
			Surround mode	-90	-75	
SVRR	Supply voltage rejection ratio	ΔV <sub>cc</sub> = -20dBv, f = 100Hz		-40	-25	dB
TMUTE	Mute time	Echo mode	515		525	ms
		Surround mode	122		132	



**DELAY TIME**

**1. MODE**

Mode	Mode	Echofb output
L	Surround mode	OFF
H	Echo mode	ON

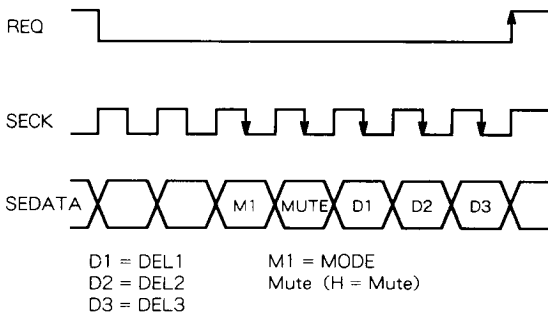
**2. EASY MODE (Parallel Data Input)  $\mu$ -COM/EASY=L (fck=4.0MHz)**

Pin name (Note1)			Surround mode		Echo mode		
$\mu$ -COM/EASY	DEL1	DEL2	DEL3	fs	Td	fs	Td
L	L	L	L	500	4.1	250	20.5
	H	H	L		10.2		41.0
	H	L	L		14.3		61.4
	L	H	L		20.5		81.9
	H	L	H	24.6	98.3	125	122.9
	L	L	H	30.7	139.3		
	L	H	H	34.8	163.8		
	H	H	H	41.0			

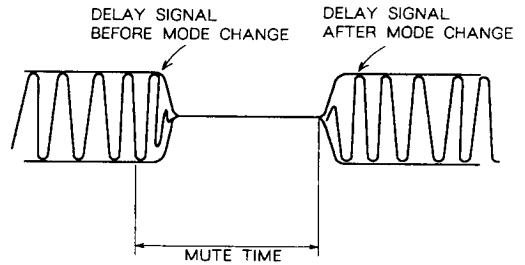
fs = Sampling frequency (kHz), Td = Delay time (msec)  
 Note 1. DEL1, DEL2, DEL3, and MUTE are input pins with pull-down.

**3.  $\mu$ -COM MODE (Serial Data Input)**

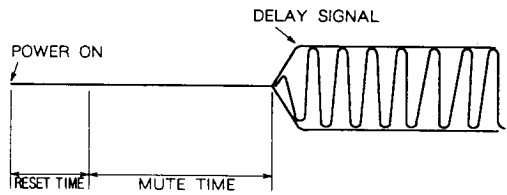
**TIMING DIAGRAM ( $\mu$ -COM/EASY=H)**



**MUTING**



Waveforms of the signal upon change of delay time mode



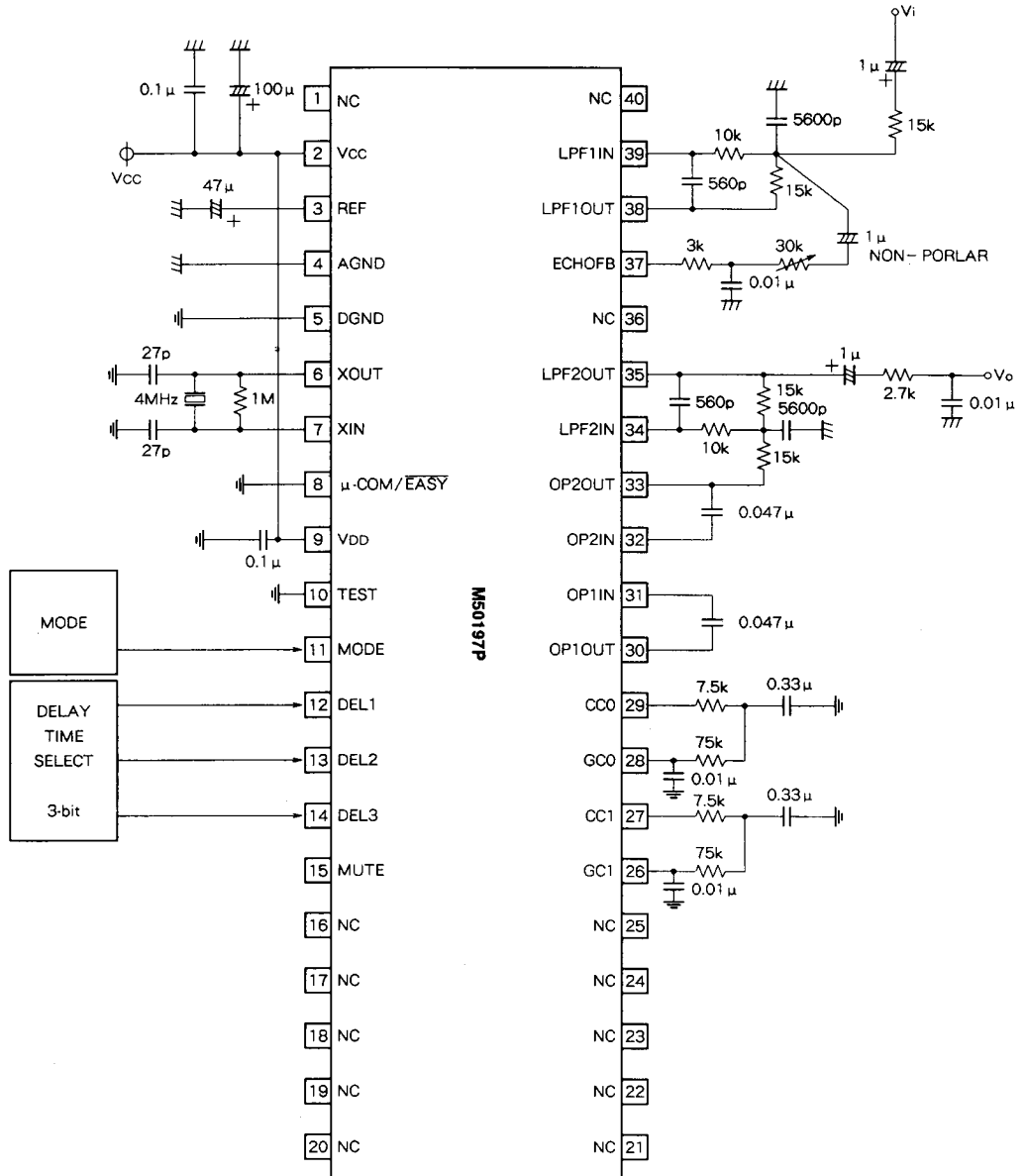
Waveforms of the signal at power-on

Pin name	Mute mode	Mute time (msec)
L	Surround	132.0
H	Echo	525.0

The time chart shown is  $\mu$ -COM mode.

When REQ signal is low-level, SEDATA signal is latched at the falling edge of the SECK signal, and the last 5-delay time mode data are set at the rising edge of the REQ signal.

APPLICATION EXAMPLE (M50197P)



Units Resistance : Ω  
Capacitance : F

