HM-6561

March 1997

256 x 4 CMOS RAM

Features

- **Low Power Standby . . . . . 50μW Max**
- **Low Power Operation . . . . . 20mW/MHz Max**
- **Fast Access Time. . . . . 200ns Max**
- **Data Retention . . . . . .at 2.0V Min**
- **TTL Compatible Input/Output**
- **High Output Drive - 1 TTL Load**
- **On-Chip Address Registers**
- **Common Data In/Out**
- **Three-State Output**
- **Easy Microprocessor Interfacing**

Description

The HM-6561 is a 256 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On-chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

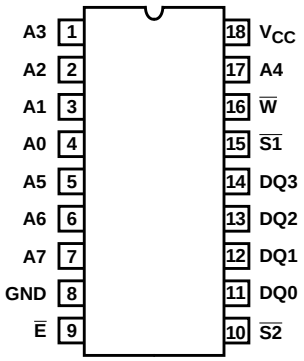
The HM-6561 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

PACKAGE	TEMPERATURE RANGE	220ns	300ns	PKG. NO.
CERDIP	-40^{o}C to +85^{o}C	HM1-6561B-9	HM1-6561-9	F18.3

Pinout

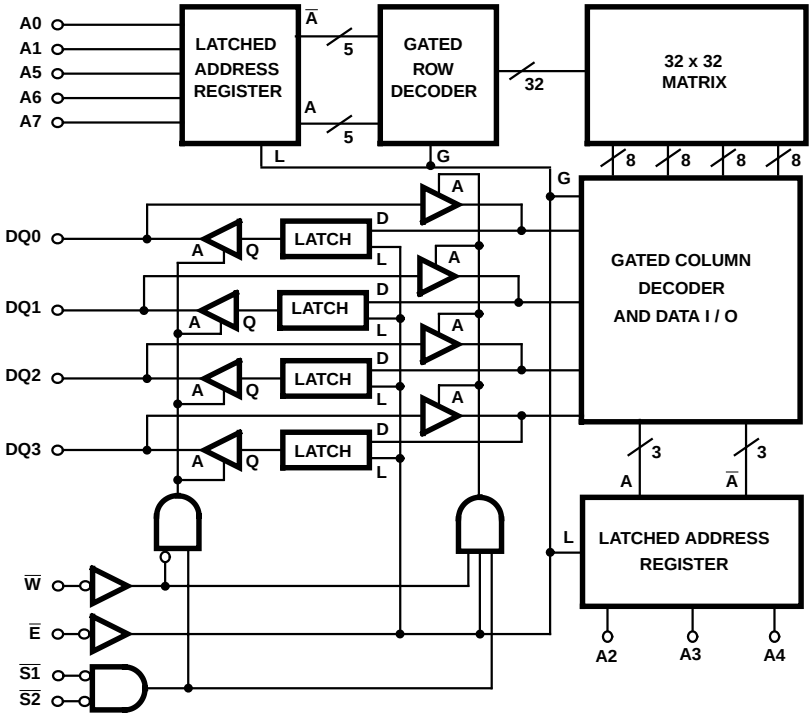
HM-6561
(CERDIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
DQ	Data In/Out

File Number **2991.1**

Functional Diagram



NOTES:

1. All lines positive logic-active high.
2. Three-state Buffers: A high → output active.
3. Data Latches: L high → Q = D and Q latches on falling edge of L.
4. Address Latches and Gated Decoders: Latch on falling edge of $\overline{E}$ and gate on falling edge of $\overline{E}$.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage. . . . . GND -0.3V to V_{CC} +0.3V
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	$74^oC/W$	$18^oC/W$

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature . . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 1944 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V

Operating Temperature Range
HM-6561B-9, HM6561-9 . . . . . -40^oC to $+85^oC$

DC Electrical Specifications V_{CC} = 5V ± 10%; T_A = -40^oC to $+85^oC$ (HM-6561B-9, HM-6561-9)

SYMBOL	PARAMETER	LIMITS		UNITS	TEST CONDITIONS
		MIN	MAX		
ICCSB	Standby Supply Current	-	10	µA	IO = 0mA, VI = V_{CC} or GND, V_{CC} = 5.5V
ICCOP	Operating Supply Current (Note 1)	-	4	mA	$\overline{E}$ = 1MHz, IO = 0mA, V_{CC} = 5.5V, VI = V_{CC} or GND, $\overline{W}$ = GND
ICCDR	Data Retention Supply Current	-	10	µA	V_{CC} = 2.0V, IO = 0mA, VI = V_{CC} or GND, $\overline{E}$ = V_{CC}
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = V_{CC} or GND, V_{CC} = 5.5V
VIL	Input Low Voltage	-0.3	0.8	V	V_{CC} = 4.5V
VIH	Input High Voltage	V_{CC} -2.0	V_{CC} +0.3	V	V_{CC} = 5.5V
VOL	Output Low Voltage	-	0.4	V	IO = 1.6mA, V_{CC} = 4.5V
VOH	Output High Voltage	2.4	-	V	IO = -0.4mA, V_{CC} = 5.5V

Capacitance T_A = $+25^oC$

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	6	pF	f = 1MHz, All measurements are referenced to device GND
CIO	Input/Output Capacitance (Note 2)	10	pF	

NOTES:

1. Typical derating 1.5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

AC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6561B-9, HM-6561-9)

SYMBOL	PARAMETER	LIMITS				UNITS	TEST CONDITIONS
		HM-6561B-9		HM-6561-9			
		MIN	MAX	MIN	MAX		
(1) TELQV	Chip Enable Access Time	-	220	-	300	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	220	-	300	ns	(Notes 1, 3, 4)
(3) TSLQX	Chip Select Output Enable Time	5	120	5	150	ns	(Notes 2, 3)
(4) TSHQZ	Chip Select Output Disable Time	-	120	-	150	ns	(Notes 2, 3)
(5) TELEH	Chip Enable Pulse Negative Width	220	-	300	-	ns	(Notes 1, 3)
(6) TEHEL	Chip Enable Pulse Positive Width	100	-	100	-	ns	(Notes 1, 3)
(7) TAVEL	Address Setup Time	0	-	0	-	ns	(Notes 1, 3)
(8) TELAX	Address Hold Time	40	-	50	-	ns	(Notes 1, 3)
(9) TDVWH	Data Setup Time	100	-	150	-	ns	(Notes 1, 3)
(10) TWHDX	Data Hold Time	0	-	0	-	ns	(Notes 1, 3)
(11) TWLDV	Write Data Delay Time	20	-	30	-	ns	(Notes 1, 3)
(12) TWLSH	Chip Select Write Pulse Setup Time	120	-	180	-	ns	(Notes 1, 3)
(13) TWLEH	Chip Enable Write Pulse Setup Time	120	-	180	-	ns	(Notes 1, 3)
(14) TSLWH	Chip Select Write Pulse Hold Time	120	-	180	-	ns	(Notes 1, 3)
(15) TELWH	Chip Enable Write Pulse Hold Time	120	-	180	-	ns	(Notes 1, 3)
(16) TWLWH	Write Enable Pulse Width	120	-	180	-	ns	(Notes 1, 3)
(17) TELEL	Read or Write Cycle Time	320	-	400	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5V and 5.5V.
4. TAVQV = TELQV + TAVEL.

Timing Waveforms

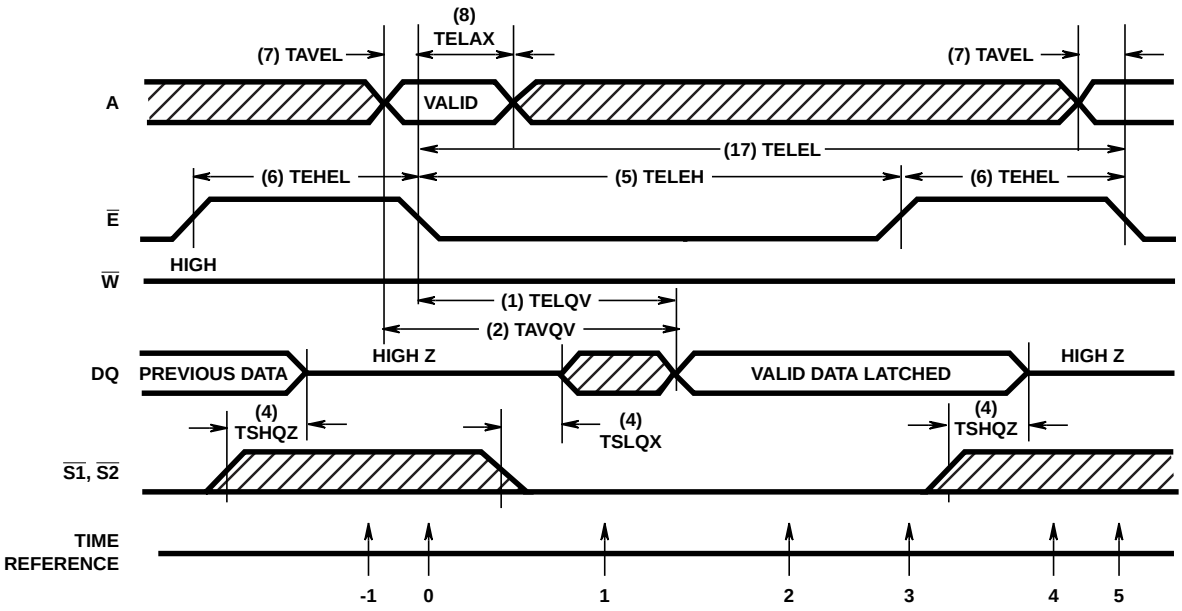


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUT	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{W}$	A	DQ	
-1	H	H	X	X	Z	Memory Disabled
0	↘	X	H	V	Z	Cycle Begins, Addresses are Latched
1	L	L	H	X	X	Output Enabled
2	L	L	H	X	V	Output Valid
3	↗	L	H	X	V	Output Latched
4	H	H	X	X	Z	Device Disabled, Prepare for Next Cycle (Same as -1)
5	↘	X	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE:

1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The HM-6561 Read Cycle is initiated on the falling edge of $\overline{E}$. This signal latches the input address word into on-chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data $\overline{E}$, $\overline{S1}$ and $\overline{S2}$ must be low and $\overline{W}$ must be high. The output data will be valid at access time (TELQV).

The HM-6561 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains latched until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Timing Waveforms (Continued)

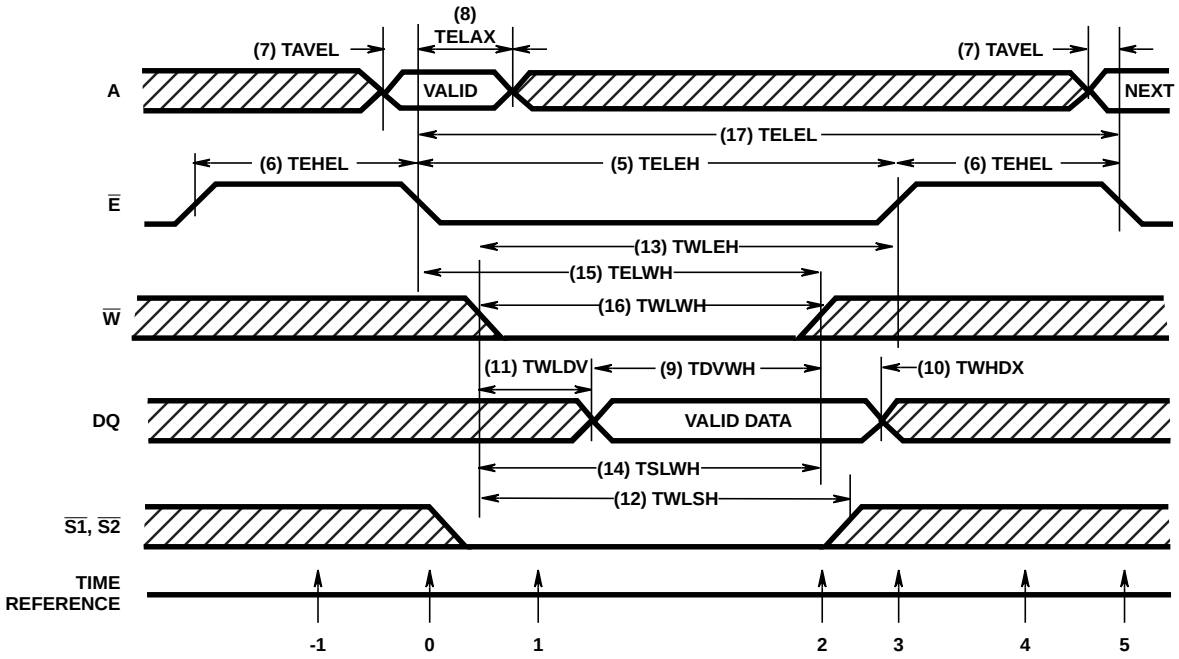


FIGURE 2. WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS					FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{W}$	A	DQ	
-1	H	H	X	X	X	Memory Disabled
0	↓	X	X	V	X	Cycle Begins, Addresses are Latched
1	L	L	L	X	X	Write Period Begins
2	L	L	↑	X	V	Data In is Written
3	↑	X	H	X	X	Write is Completed
4	H	H	X	X	X	Prepare for Next Cycle (Same as -1)
5	↓	X	X	V	X	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE:

1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The write cycle begins with the $\overline{E}$ falling edge latching the address. The write portion of the cycle is defined by $\overline{E}$, $\overline{S1}$, $\overline{S2}$ and $\overline{W}$ all being low simultaneously. The write portion of the cycle is terminated by the first rising edge of any control line, $\overline{E}$, $\overline{S1}$, $\overline{S2}$ or $\overline{W}$. The data setup and data hold times (TDVWH and TWHDX) must be referenced to the terminating signal. For example, if $\overline{S2}$ rises first, data setup and hold times become TDVS2H and TS2HDX; and are numerically equal to TDVWH and TWHDX.

Data input/output multiplexing is controlled by $\overline{W}$. Care must be taken to avoid data bus conflicts, where the RAM outputs become enabled when another device is driving the data inputs. The following two examples illustrate the timing required to avoid bus conflicts.

Case 1: Both $\overline{S1}$ and $\overline{S2}$ Fall Before $\overline{W}$ Falls.

If both selects fall before $\overline{W}$ falls, the RAM outputs will become enabled. $\overline{W}$ is used to disable the outputs, so a disable time (TWLQZ = TWLDV) must pass before any other device can begin to drive the data inputs. This method of operation requires a wider write pulse, because TWLDV + TDVWH is greater than TWLWH. In this case TWLSL + TSHWH are meaningless and can be ignored.

Case 2: $\overline{W}$ Falls Before Both $\overline{S1}$ and $\overline{S2}$ Fall.

If one or both selects are high until W falls, the outputs are guaranteed not to enable at the beginning of the cycle. This eliminates the concern for data bus conflicts and simplifies data input timing. Data input may be applied as early as convenient, and TWLDV is ignored. Since $\overline{W}$ is not used to

disable the outputs it can be shorter than in Case 1; TWLWH is the minimum write pulse. At the end of the write period, if $\overline{W}$ rises before either select, the outputs will enable, reading data just written. They will not disable until either select goes high (TSHQZ).

	IF	OBSERVE	IGNORE
CASE 1	Both $\overline{S1}$ and $\overline{S2}$ = Low Before $\overline{W}$ = Low	TWLQZ TWLDV TDVWH	TWLWH
CASE 2	$\overline{W}$ = Low Before Both $\overline{S1}$ and $\overline{S2}$ = Low	TWLWH TDVWH	TWLQZ TWLDV

If a series of consecutive write cycles are to be performed, W may remain low until all desired locations are written. This is an extension of Case 2.

Read-Modify-Write cycles and Read-Write-Read cycles can be performed (extension of Case 1). In fact data may be modified as many times as desired with $\overline{E}$ remaining low.

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029