MARC4 – 4-bit Microcontroller for LCD Applications

The M43C505 (e3505) is a member of the MARC4 family of low cost, single chip CMOS microcontrollers. This 4-bit µC contains an on-chip RC oscillator, CPU core, RAM, ROM, I/O, 32-kHz crystal oscillator, 15-stage prescaler/interval timer and liquid crystal display driver circuitry.

Features

- 4 bit stack oriented Harvard architecture
- 4 K x 8 bit application ROM
- 253 x 4 bit of on-chip RAM
- 13 bidirectional I/O lines
- 4 input lines with interrupt facility
- Fast on-chip RC oscillator
  core operating frequency min. 1 MHz at 3 Volts
  (2 µs instruction cycle time)
- Separate watch crystal oscillator for time keeping
- 2 external and 2 interval timer / prescaler interrupts
- Master reset and static power-on reset circuitry with brown-out function
- Programmable LCD module for up to 80 segment

Benefits

- Built-in LCD voltage generation with temperature compensation (constant contrast)
- SLEEP mode for battery-operated applications
- RAM and core register contents valid at V_{DD} = 2.0 V (µC in SLEEP mode; T_{amb} = 0 ...+75 °C)
- Independent power supplies (µC-crystal oscillator)
- High level language qFORTH with a highly optimizing compiler
- Piggyback version for program evaluation
- Metal-ROM version M45C535 (e3535) for fast prototyping (see Appendix)
- PC based development system

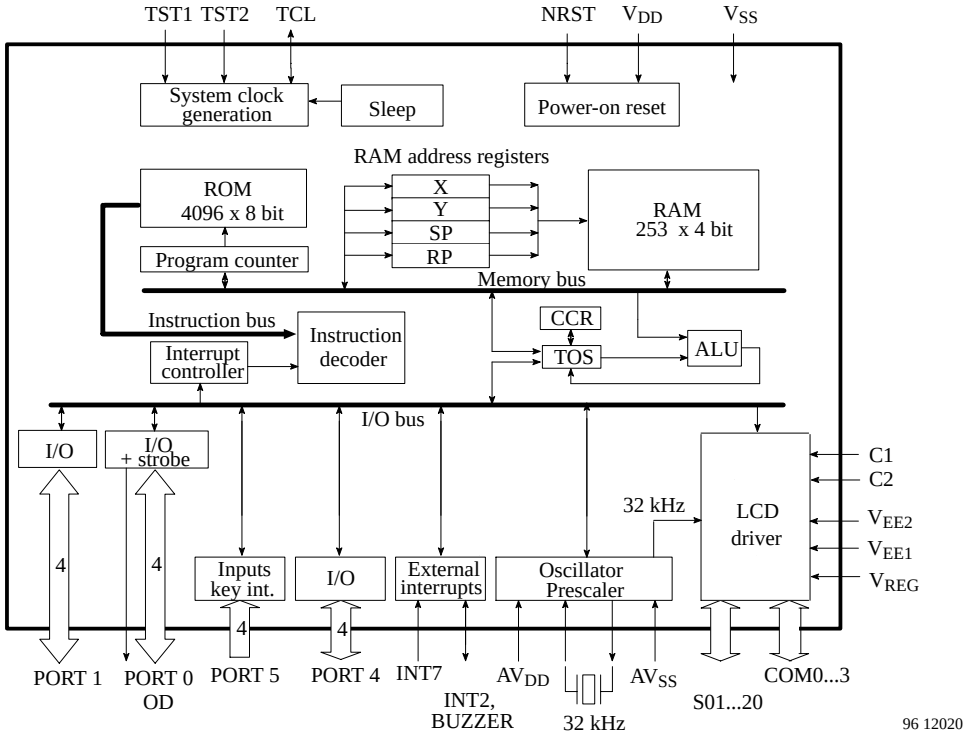

Figure 1. Block diagram of M43C505

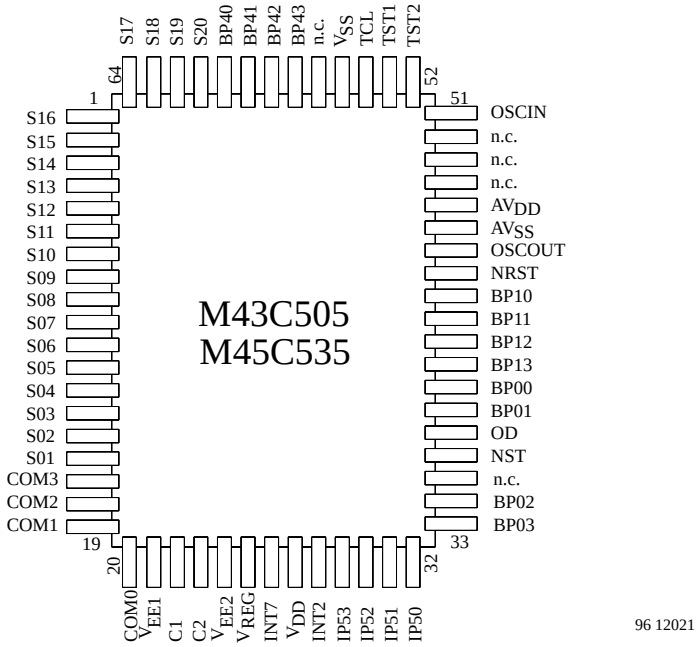

Figure 2. M43C505/ M45C535 in 64-pin plastic QFP (top view)

Table 1. Pin description

Name	Function
V_{DD}	Power supply voltage +2.4 V to 6.2 V
AV_{DD}	Analogue power supply voltage +2.4 V to 6.2 V
V_{SS}	Circuit ground
AV_{SS}	Analogue circuit ground
V_{REG}	Regulated, temperature compensated supply voltage for 5 V LCD panels
V_{EE1}	Storage capacitor pin for doubled LCD voltage
V_{EE2}	Storage capacitor pin for tripled LCD voltage
C1, C2	Pump capacitor connection pins for LCD
BP00 – BP03	4 bidirectional I/O lines of Port 0 – automatic nibblewise configurable I/O
BP10 – BP13	4 bidirectional I/O lines of Port 1 – automatic nibblewise configurable I/O
OD	Output strobe during read access from Port 0 (see figure 6)
NST	Output strobe during write access to Port 0 (see figure 6)
BP40 – BP43	4 bidirectional I/O lines of Port 4 (*) – automatic nibblewise configurable I/O
IP50 – IP53	4 input lines of Port 5 with interrupt facility (*)
COM0–COM3	LCD backplane driver outputs
S01–S20	LCD segment driver outputs
INT7	External interrupt input pin (*)
INT2/BUZ	External interrupt input or buzzer output pin (*)
TST1, TST2	Test mode inputs, used to control different test modes (internal pull-up)
TCL	Clock input/output for system clock (during test mode)
OSCIN;OSCOUT	32-kHz quartz crystal connection pins
NRST	Reset input, a logic low on this pin resets the device

(*) For mask options, please see the ordering information.

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1 Signal Description, I/O Programming, Memory, Core Registers, and Self-Check

This section provides a description of the I/O signals, the input/output programming, memory, core registers, and a description of the self-check.

1.1 Signal Description

1.1.1 V_{DD}, V_{SS}, AV_{DD} and AV_{SS}

Power is supplied to the microcontroller using these pins. **V_{DD}** is power for the µC core, RAM, ROM and the peripherals, **V_{SS}** is ground. **AV_{DD}** is power for the crystal oscillator and **AV_{SS}** is ground.

1.1.2 V_{REG}, V_{EE1}, V_{EE2}, C1 and C2

V_{REG} is the temperature compensated reference for the LCD voltage booster circuitry. It is used for building up the doubled (**V_{EE1}**) and tripled (**V_{EE2}**) voltage levels required by multiplexed LCDs. The pump capacitor for the voltage generator is connected between **C1** and **C2**. Storage capacitors must be attached at **V_{EE1}** and **V_{EE2}** towards V_{SS} (see figure 16). As mask programmable option **V_{REG}** can be either supplied from an external source or generated internally.

1.1.3 NRST

The **NRST** input is not required for startup but can be used to reset the internal state of the microcontroller and provide an orderly software startup procedure. Refer to **Reset modes** in section 2 for a detailed description.

1.1.4 TCL (RC Oscillator)

The system clock for the µC is derived from a fully integrated on-chip RC oscillator circuit. This oscillator tracks the supply and temperature to ensure optimum operation of the microcontroller under all conditions (see figures 29 and 30).

The **TCL** pin can be used as clock input for an external CMOS oscillator. In this configuration the low power SLEEP mode cannot be used and care must be taken with the reset conditions. The **TCL** pin must be held low for at least 1ms after the release of power-on or an external reset to allow the external clocking mode.

1.1.5 TST1, TST2

These two lines contain integrated pull-up transistors and define different production and emulation test modes. When both are high, the µC is in the normal operation mode.

1.1.6 OSCIN, OSCOUT (Crystal Oscillator)

Normally a 32-kHz standard watch crystal is connected to these pins. As mask programmable option a built-in capacitor of 20 pF can be connected to each pin.

To ensure proper operation of the crystal oscillator a chosen crystal should follow the specification given in the table below.

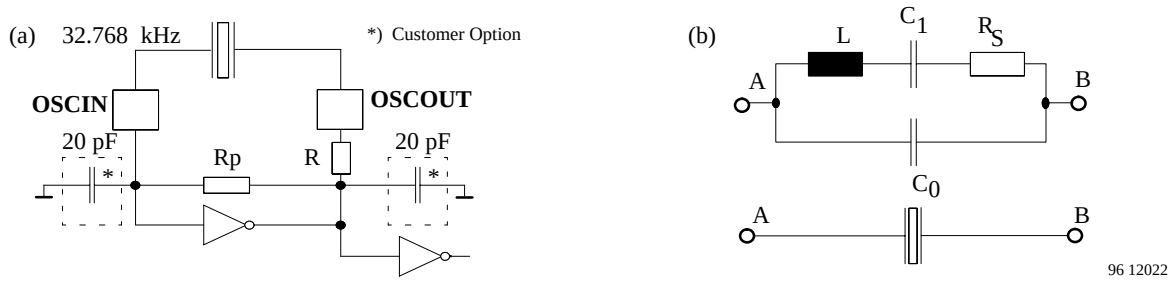


Figure 3. (a) Crystal oscillator – (b) equivalent circuit

Table 1. Standard crystal specification

Parameter	Symbol	Typ.	Max.	Unit
Frequency	f	32.768	100	kHz
Series resistance	R_S	30	50	kΩ
Static/Shunt capacitance	C_0	1.5		pF
Dynamic capacitance	C_1	3		fF
Load capacitance	C_L	10	12.5	pF

The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and startup stabilization time.

Use of an external CMOS oscillator is recommended when crystals outside of the above specified range are to be used.

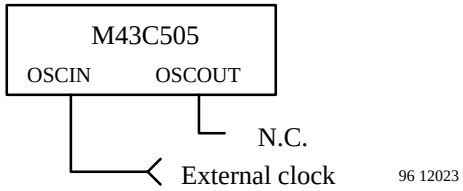


Figure 4. External clocking

1.1.7 I/O Address Map

Table 2. Port address map

Port	Direction	Function
0	I/O	Bidirectional port with two strobe lines (NST, OD)
1	I/O	Bidirectional port
2	Output	LCD control port (see table 6)
3	Output	LCD data port
4	I/O	Bidirectional port (with open drain output as mask option)
5	Input	Input port with interrupt facility
6	Output	Interrupt mask/buzzer output control register (see table 4)
15	Output	Prescaler/interval timer control port (see table 5)

Table 2 contains the port address and a short functional description of the on-chip modules.

1.1.8 BP00-BP03, NST and OD

These four I/O lines and two strobe output lines (**NST**, **OD**) comprise Port 0. The port consists of CMOS output drivers with an integrated pull-up resistor in the input mode. The direction of the port is software programmable and all Port 0 lines are configured as input during power-on or external reset. Refer to the **Input/Output programming** paragraph for a more detailed description.

1.1.9 BP10-BP13

These four I/O lines comprise Port 1. The port contains CMOS output drivers with an integrated pull-up resistor in the input mode. The direction of the port is software programmable and all Port 1 lines are configured as input during power-on or external reset. Refer to the **Input/ Output programming** paragraph for a more detailed description.

1.1.10 BP40-BP43

These four I/O lines comprise Port 4. As mask programmable option each I/O line can be used as CMOS or open drain output and with or without an integrated pull-up resistor in the input mode. See figure 5 in the following paragraph for a port schematic diagram.

The direction of the complete port is software programmable and all Port 4 lines are configured as input during power-on or external reset. Refer to the **Input/Output programming** paragraph for more details concerning the programming.

1.1.11 IP50-IP53

These four input lines comprise Port 5. As a mask programmable option each input line can be used with or without an integrated pull-up resistor. The Port 5 logic is capable of generating an additional interrupt (priority level 4), when any of the four input lines is driven low. This function is disabled after power-on or external reset. Refer to the **Input/Output programming** paragraph for more details concerning the programming.

1.1.12 COM0-COM3

These four output lines provide the backplane drive signals which should be connected directly to the liquid crystal display unit. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs should not be connected.

1.1.13 S01-S20

These 20 segment output lines provide the segment drive signals which should be connected directly to the liquid crystal display unit. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 20 segment outputs are required the unused segment outputs should not be connected.

1.1.14 INT2, INT7 (External Interrupts)

The external interrupt inputs are negative edge triggered and have Schmitt-trigger characteristics to improve the noise immunity.

The microcontroller completes the current instruction before it responds to the interrupt request. When the interrupt input pin is driven low a logic one is latched internally to signify the interrupt request, if the corresponding enable bit in the mask register is set. When the microcontroller completes its current instruction, the interrupt pending register is tested. If an interrupt is pending and the interrupt enable bit in the condition code register is set, the interrupt sequence begins. See **Interrupts** in section 2 for more details.

1.1.15 Buzzer (INT2)

The **INT2** pin is bidirectional. When set to input, this pad functions as an external, maskable interrupt. When set to output the programmer can choose between a static output value or an audio frequency square wave. The buzzer frequency of 2.048 or 4.096 kHz is selectable as a mask programmable option. See **Interrupts** in section 2 for more details on programming.

1.2 Input/Output Programming

1.2.1 Bidirectional Ports

Port 0, 1, and 4 may be programmed as an input or an output under software control. The direction of a port is determined by an IN or OUT instruction and is held until another IN or OUT instruction for this port is executed.

The direction of these bidirectional ports is not switchable on a bit wise basis. The output latches hold the state of the last data value written to the port. At power-on or external reset all pins of Port 0, 1, and 4 are set to input mode and all output latches are set to a logic 1. Whenever the port is switched from input to output the last value stored in the latches will appear on the outputs for one clock cycle (see figure 6).

When switching bidirectional ports from output to input the stray capacitance of the connection wires may cause the data read to be the same as the last data written to this port. This behaviour can be used by connecting large enough capacitors to the pins of the bidirectional port to read back the previous data written to this port.

On the other hand, to avoid the negative effects of stray capacitances one of the following approaches should be used:

- Use two IN instructions, and DROP the first data nibble read.
- Write Fh to the port to be read before executing the IN instruction.

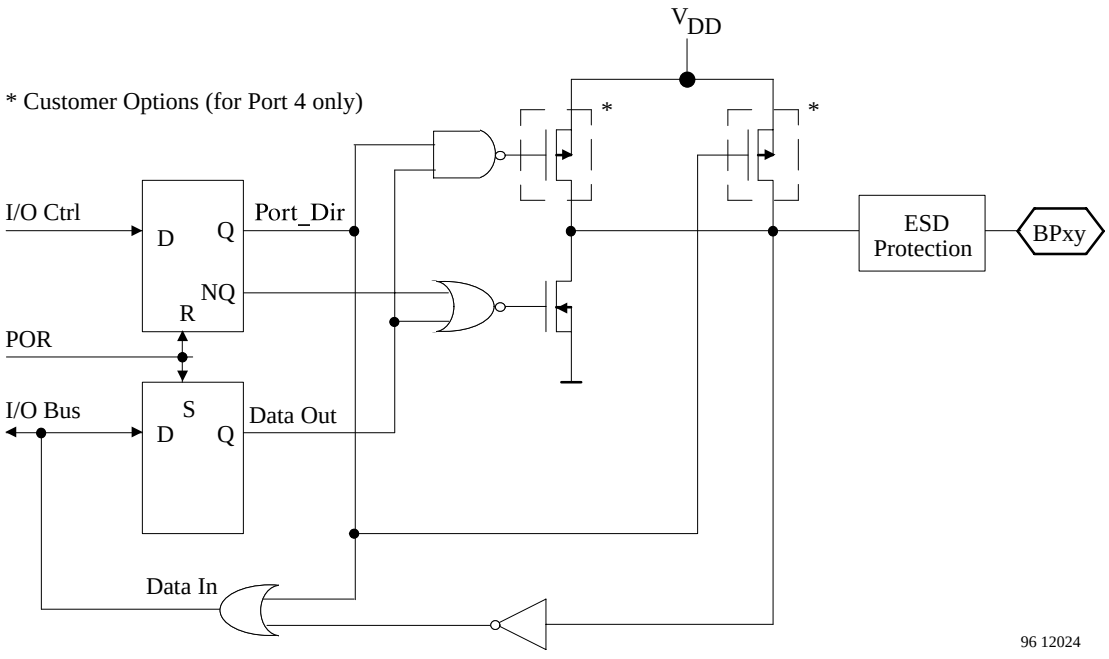


Figure 5. Bidirectional port schematics

Bidirectional Port 0

The bidirectional Port 0 supports a hardware interface for external devices which require a data write strobe and a data read strobe pin.

The **NST** pin is an active low strobe issued when data written to Port 0 is valid. The **OD** signal is a strobe indicating that data is being read from Port 0 by the µC. Data must be valid at the latest 100 ns after the falling edge of **OD** (figure 6).

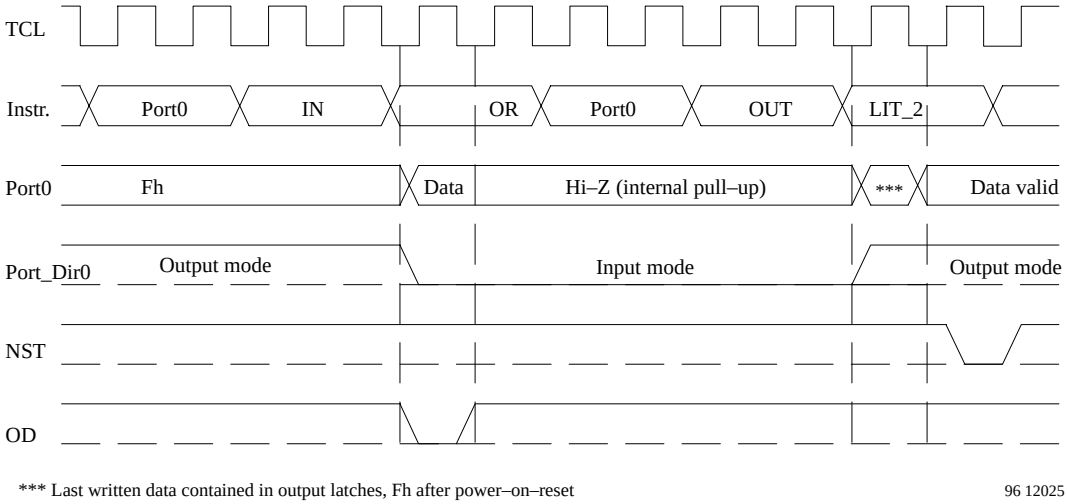


Figure 6. Read and write cycle timing at Port 0 (OD, NST)

1.2.2 Input Port 5

The data on Port 5 is sent to the top of the expression stack whenever an IN instruction (addressing Port 5) is executed. The Port 5 logic may generate an additional interrupt (priority level 4), when any of the four input lines is driven low. This function is useful for implementing an interrupt driven keyboard. It is disabled after power-on or external reset. The corresponding interrupt level 4 is enabled by writing any value to Port 5 and automatically disabled after a read operation from Port 5. The interrupt service routine may use the prescaler to perform a software based keypad debouncing.

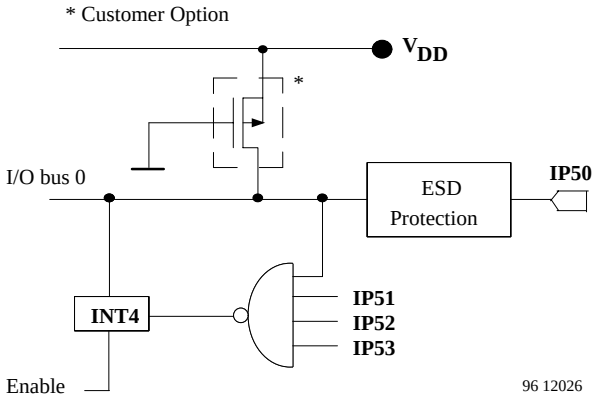


Figure 7. Port 5 with pull-up option

1.3 Memory

The MARC4 family of microcontrollers is based on the Harvard architecture with physically separate program memory (ROM) and data memory (RAM).

The program memory (ROM) is mask programmed with the customer application program during the fabrication of the microcontroller. The ROM is addressed by a 12-bit wide program counter, thus limiting the program size to a maximum of 4096 bytes which cannot be extended by using external memory. The user ROM starts with a 512 byte segment (“Zero Page”) which contains predefined start addresses for interrupt service routines and special subroutines accessible with single byte (SCALL) instructions. The corresponding memory map is shown in figure 8.

The self test routines should be included as part of the free program space. The 16-bit check sum (CRC) is located by the compiler in the last two bytes of ROM.

The on-chip 256 × 4 bit RAM is divided in the 12-bit wide return stack, the 4-bit wide expression stack (both with a user definable depth) and the data memory. The fixed return address (000h) which points to the $AUTOSLEEP routine is located at RAM address FCh.

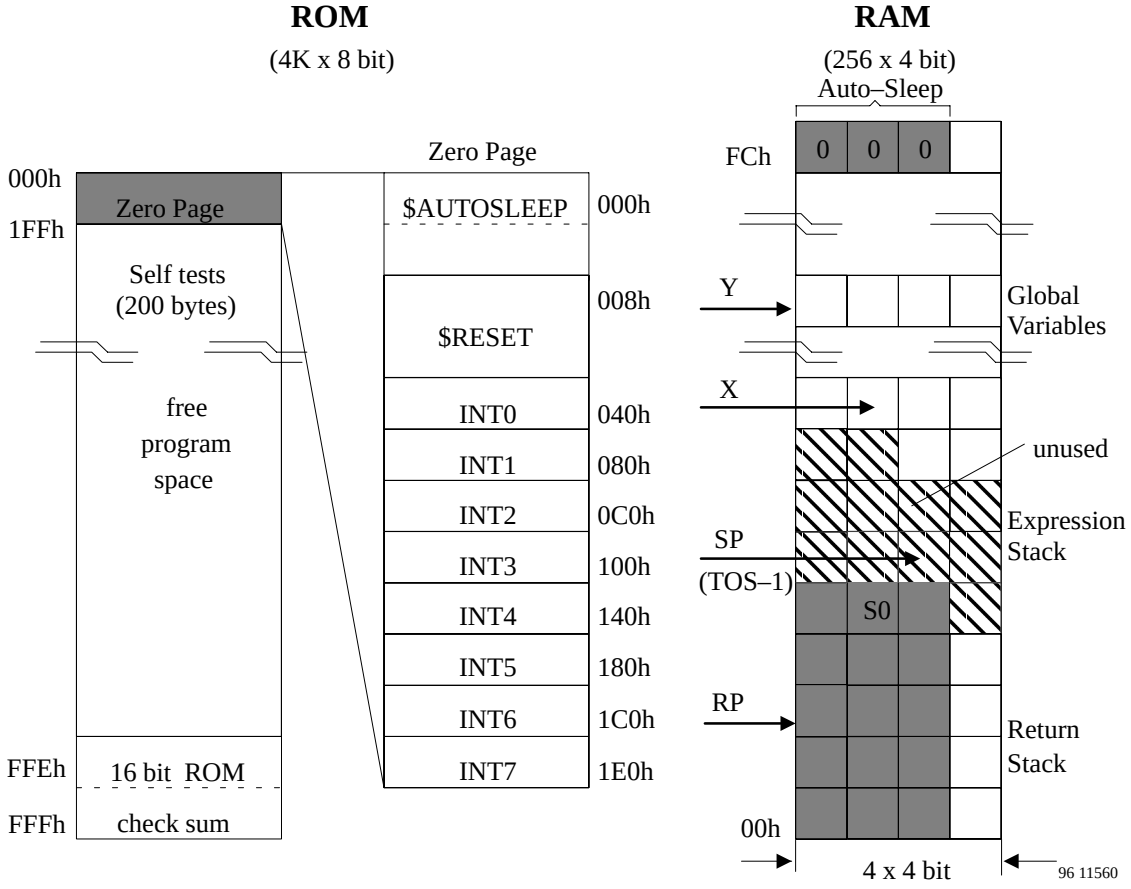


Figure 8. Memory map

1.4 Core Registers

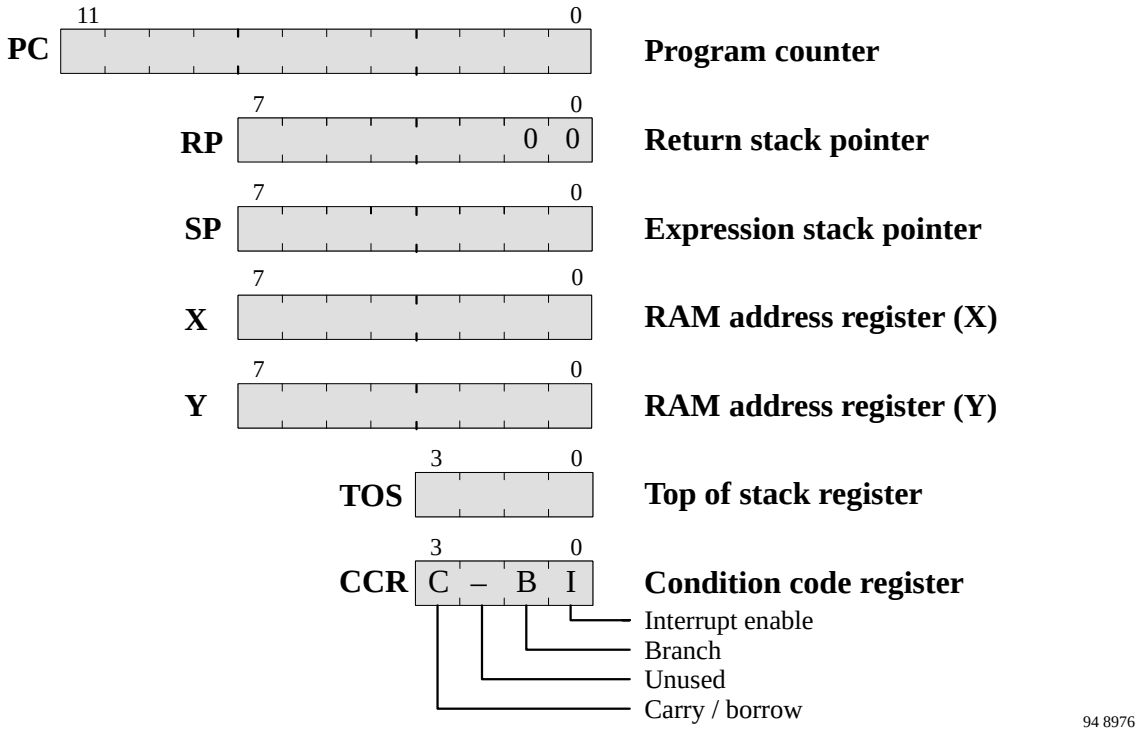


Figure 9. Programming model

As shown in the programming model, the MARC4 core is based on seven registers.

1.4.1 Accumulator (TOS)

Because this microcontroller is a stack based machine with two on-chip stacks located in the internal RAM, all arithmetic, I/O and memory reference operations take their operands from, and return their result to the 4-bit wide expression stack. This stack is also used for passing parameters between subroutines, and as a scratchpad area for temporary storage of data. The top element of the expression stack is immediately accessible through the **TOS** register. The MARC4 can perform most of the operations dealing with the top of stack items (TOS and TOS-1) in a single byte, single cycle instruction.

1.4.2 Expression Stack Pointer (SP)

The 8 bit wide stack pointer **SP** contains the address of the next-to-top 4-bit item (TOS-1) on the expression stack, located in the internal RAM. After power-on reset the stack pointer has to be initialized to the start address of the allocated expression stack area (**S0**).

1.4.3 RAM Address Register (X and Y)

The 8 bit wide registers **X** and **Y** are used to address any 4-bit item in the RAM.

Using either the pre-increment or post-decrement addressing mode it is comfortable to compare, fill or move arrays in the RAM area.

1.4.4 Return Stack Pointer (RP)

The return stack pointer **RP** points to the top element of the return stack.

The 12-bit wide return stack is used for storing subroutine return addresses and keeping loop index counts. The return stack can also be used as a temporary storage area. The MARC4 instruction set supports the exchange of data between the top elements of the expression and return stack. The return stack automatically pre-increments and post-decrements in steps of 4. This means that every time a subroutine return address is stacked, 4-bit RAM locations are left unwritten. These locations are used by the qFORTH compiler to allocate 4-bit variables.

After power-on reset the return stack pointer has to be initialized to FCh.

1.4.5 Program Counter (PC)

The program counter (**PC**) is a 12-bit register that contains the address of the next instruction to be executed by the microcontroller.

1.4.6 Condition Code Register (CCR)

The 4-bit wide condition code register (**CCR**) indicates the results of the instruction just executed as well as the state of the microcontroller. These bits can be individually tested by a program and specified action will take place as a result of their state. Each bit is explained in the following paragraphs.

Carry/Borrow (C)

This flag indicates that a borrow or carry out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during shift and rotate operations and the execution of SET_BCF, CLR_BCF and CCR! instructions.

Zero (Z)

When this bit is set, it indicates that the result of the last arithmetic or logical manipulation was zero.

Branch (B)

A conditional branch takes place when the branch flag was set by one of the previous instructions (e.g. a comparison operation).

Instructions such as SET_BCF, TOG_BF, and CLR_BCF allow the direct manipulation of the branch flag under program control. The flag is affected by all ALU operations except CCR@, DI, SWI, RTI, and OUT.

Interrupt enable (I)

This flag is used to control the interrupt processing on a global basis. Resetting the interrupt enable flag (using the DI instruction) disables all interrupts. The µC does not process further interrupt requests until the interrupt enable flag is set again by either executing an EI, RTI (Return-from-interrupt) instruction or entering the SLEEP mode. After power-on or an external reset the interrupt enable flag is automatically reset. The RTI instruction at the end of the $RESET routine will set the interrupt enable flag and thereby enable all interrupts.

1.4.7 Self-Check

The self test capability of the MARC4 provides the possibility of easily checking the core by executing the RAM and ROM tests after power-on reset. The RAM_TEST and ROM_TEST routines have to be included (either conditionally or unconditionally) in the $RESET routine.

Example: Different methods to implement the self test routines

```
: $RESET    >SP       S0
            >RP       FCh
            Port0     IN  0=
            IF
                      RAM_Test
                      ROM_Test
            THEN
            Reset_LCD
            Init_Vars
;
```

```
: $RESET    DI
            >SP                 S0
            >RP                 FCh
            RAM_Test
            ROM_Test
            ErrorFlag @0 =
            IF
                                Init_Vars
            THEN
;
```

Note: If the self test routines are included unconditionally care should be taken that the pattern written to Port 1 does not interfere with the application hardware. If the stimulus read from Port 0 is different from zero, TEMIC has to be informed (see ordering information).

2 Reset Modes, Interrupts, and Low Power Modes

This chapter describes the reset modes and the different interrupt capabilities of this microcontroller. The low power consumption modes are also discussed.

2.1 Reset Modes

The M43C505 has two reset modes: an active low external reset pin (**NRST**) and a power-on reset function.

2.1.1 External Reset (NRST)

The **NRST** input pin is used to reset the µC to provide an orderly software startup procedure. When using the external reset mode, the **NRST** pin should be low for a minimum of two instruction cycle times.

2.1.2 Power-on Reset

The power-on reset occurs when a positive transition is detected on the power supply input pin. The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage. A power-down reset occurs when a negative transition is detected on the power supply input pin. To improve noise immunity the power-on reset has Schmitt-trigger characteristics as shown in figure 31.

2.1.3 Effects on Internal Circuitry

Both reset modes guarantee a well-defined start condition of the complete microcontroller. During reset all interrupts are disabled, all pending and active interrupts are cleared, all on-chip peripherals are reset and a non-maskable interrupt request is generated. This interrupt has the absolute highest priority, having access to the microcontroller at all times.

The main tasks of the reset service routine ($RESET) are:

- Stack pointer initialization,
- Self test program execution,
- Variable and array initialization, and
- Initialization and setup of the peripherals.

After execution of the $RESET service routine the interrupts are enabled automatically by the RTI or a previously executed EI instruction.

2.2 Interrupts

The M43C505 can handle interrupts of 8 priority levels (table 3). They are generated from on-chip modules (prescaler), external sources (Port 5 and interrupt pads) or synchronously from the core itself (software interrupts). Each interrupt source has a hard-wired interrupt priority and an associated interrupt service routine in the program ROM. The programmer can enable or disable all interrupts by setting or resetting the interrupt enable flag in the CCR using the EI or DI instruction.

When the interrupt enable flag is reset (interrupts disabled), the execution of interrupts is inhibited but not the logging of the interrupt requests in the interrupt pending register. While interrupts are disabled (e.g. for a time critical section of code) and an interrupt is generated the interrupt will not be lost. Its execution will only be delayed until interrupts are enabled again. Interrupts are only lost when the pending register for a particular interrupt priority is still set at the time of a further interrupt transmission of the same level. The pending register is reset either on power-on reset or on completion of the corresponding interrupt service routine by executing the RTI instruction (see figures 10 and 11).

The µC automatically enters the SLEEP mode when the lowest priority interrupt service routine has been completed. This guarantees a maximum use of the power saving capabilities of the µC. Refer to **Low power modes** for more information.

Table 3. Interrupt priority ad address allocation map

Priority	Function	Located in ROM at	Max. Length [ROM bytes]	Interrupt Opcode
INT7	External hardware interrupt, negative edge triggered	1E0h	≥ 24	FCh
INT6	Prescaler interrupt #2	1C0h	32	F8h
INT5	Prescaler interrupt #1	180h	64	F0h
INT4	Port 5, keyboard interrupt	140h	64	E8h
INT3	Software interrupts (SWI3)	100h	64	E0h
INT2	External hardware interrupt, negative edge triggered	0C0h	64	D8h
INT1	Software interrupt (SWI1)	080h	64	D0h
INT0	Software interrupt (SWI0)	040h	64	C8h

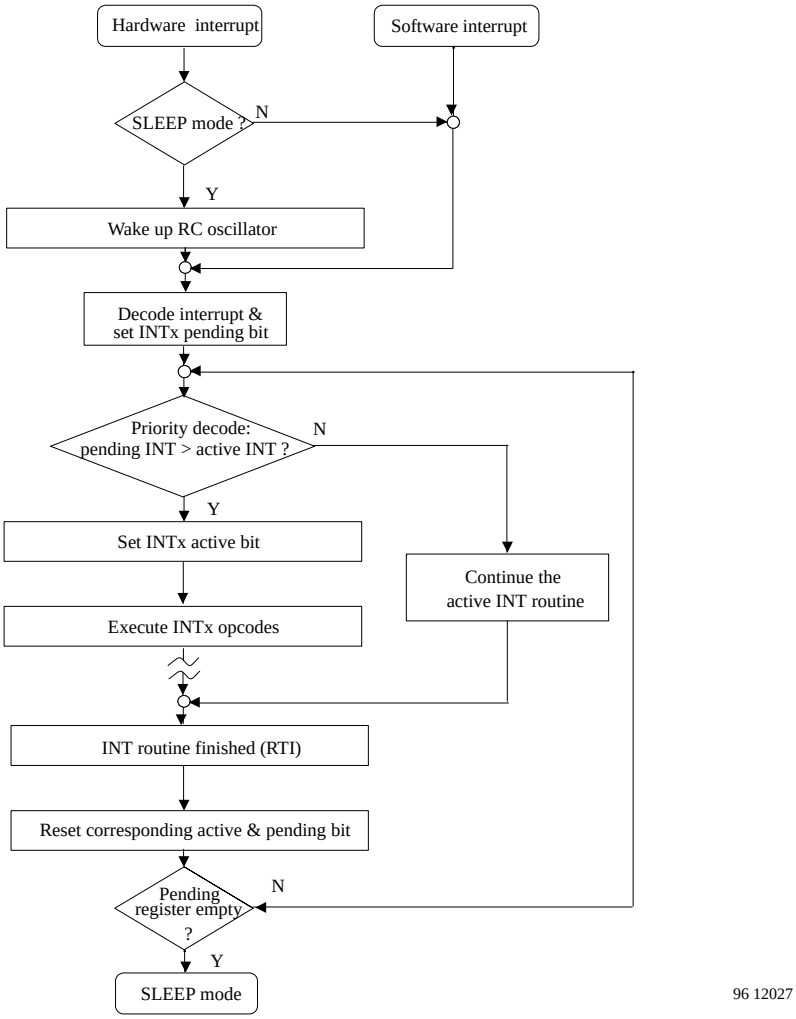


Figure 10. Interrupt flowchart

2.2.1 Interrupt Handling

The integrated interrupt controller samples all interrupt requests and latches these in the interrupt pending register. It also decodes the priority of the interrupt requests, and signals the µC when a higher priority interrupt request is present. If the µC (with interrupts enabled) receives the interrupt controller's signal an interrupt acknowledge cycle will be entered. During this cycle, the µC saves the current PC on the return stack and loads the PC with the start address of the corresponding interrupt service routine. When the µC is in the SLEEP mode it will be activated by any hardware interrupt, by the means of starting the RC oscillator and decoding the interrupt. Using the MARC4 way of interrupt transmission it is possible to transmit more than one interrupt at the same time. The transmitted interrupts are loaded into the interrupt pending register asynchronously. The priority decoder determines the interrupt with the highest priority and activates it as shown in figure 10.

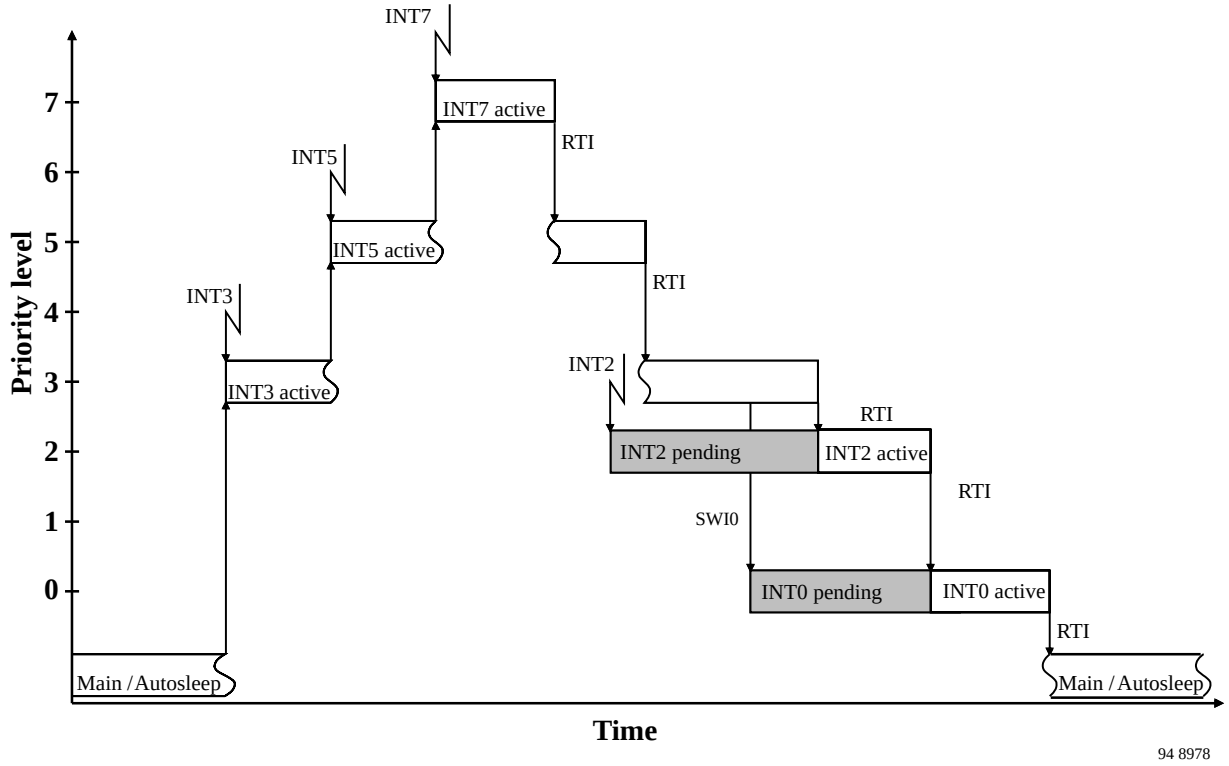


Figure 11. Interrupt processing

The interrupt priority level handling versus time is shown in figure 11.

2.2.2 Interrupt Latency

The interrupt latency is the time from the falling edge of the interrupt to the interrupt service routine being activated. This time is at minimum three and at maximum five instruction cycles depending on the state of the core. The highest interrupt frequency which can be reasonably handled is between 1 and 4 kHz depending on the supply voltage range (i.e. the RC oscillator frequency) and the duty cycle of the application.

2.2.3 Software Interrupts

Software interrupts are executable instructions which are supported by predefined macros named SWI0 through SWI7. The software triggered interrupt operates exactly like any hardware triggered interrupt.

2.3 Hardware Interrupts

Port 5 Interrupts

Port 5 may generate an interrupt of priority level 4 if any of the four input lines of Port 5 is driven low. This function is disabled after power-on reset.

The interrupt is enabled by writing any value to Port 5 and is automatically disabled after a read from Port 5.

External interrupts

The external interrupts **INT2** and **INT7** are negative edge triggered and have Schmitt-trigger characteristics to improve the noise immunity. As shown in figure 12, the following mask programmable options are available on the two external interrupt input pads:

- Integrated pull-up
- Integrated pull-down
- No pull-up or pull-down
- Active pull-up/pull-down (see figure 12b)

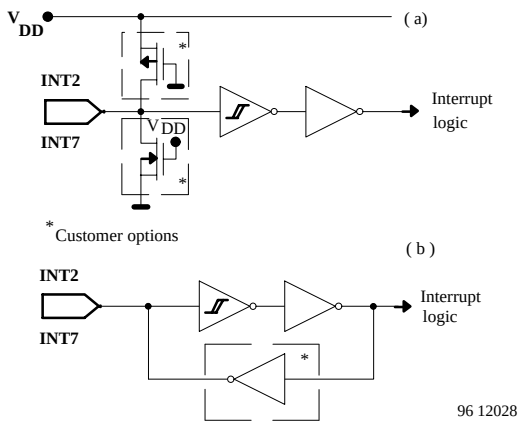


Figure 12. Interrupt option diagram

Active pull-up/pull-down option

When using the active pull-up/pull-down option (figure 12), a low input resistance is ensured without the DC current flow associated with a pull-up or pull-down resistor. The pull-up or pull-down function is selected depending on the current state of the Schmitt-trigger output. When this option is used the input impedance may vary as the internal pull-up or pull-down is switched in.

This option is useful in applications when the external signal is forced to logic 1 or 0 for a longer period of time.

2.3.1 Interrupt Mask Register

The external interrupts **INT2** and **INT7** are maskable. This means **INT2** or **INT7** may be disabled individually while still receiving all other interrupts.

Additionally, if not used as an interrupt input, **INT2** can be utilized as an output. A static output level or an audio frequency square wave is selectable in output mode.

The tone frequency is derived from the crystal oscillator frequency f_C and can be easily calculated by the following formula:

$$f_{BUZ} = \frac{f_C}{2^3} \text{ or } \frac{f_C}{2^4}$$

The frequency is either 4.096 kHz or 2.048 kHz if a standard watch crystal is used. A customer option is available to select one of the two buzzer frequencies. This output mode may also be useful for trimming the crystal oscillator frequency.

All of these actions are selected by writing a control code to Port 6 (table 4).

Table 4. Port 6 control register functions

Control Code	INT7	INT2	I/O	INT2 I/O Function
1111	enabled	enabled	Input	Negative edge triggered interrupt
1011	enabled	masked	Input	Negative edge triggered interrupt
0111	masked	enabled	Input	Negative edge triggered interrupt
0011	masked	masked	Input	Negative edge triggered interrupt
1010	enabled	masked	Output	Output high
1001	enabled	masked	Output	Output low
1000	enabled	masked	Output	Buzzer frequency
0010	masked	masked	Output	Output high
0001	masked	masked	Output	Output low
0000	masked	masked	Output	Buzzer frequency

2.4 Interval Timer/Prescaler Interrupts

The programmable interval timer is usually driven by an external 32.768 kHz watch crystal. Using for example a 38.4 kHz crystal, it is possible to emulate an asynchronous serial interface protocol easily by software.

The prescaler consists of a 15-stage divider chain with two multiplexers. They offer two interrupt sources with priority level 5 and 6. The prescaler module powers up in the reset condition which corresponds to control code Fh. The prescaler interrupt (**INT5**) has 8 programmable taps from 128 Hz down to 1 Hz. They are selectable by writing a value of 7 to 0 into the control register at port address 15. The corresponding interrupt (**INT5**) can only be masked by resetting the complete prescaler.

The second interrupt source (**INT6**) allows the selection of 5 different taps from the divider chain ranging from about 4 kHz down to 16 Hz by writing the corresponding code (Dh to 9) into the control register at port address 15.

Table 5. Selectable interval times for the prescaler (control Port 15)

Control Code	Interrupt Source	Interrupt Frequency	f_C = 32.768 kHz	
			Time Interval	Interrupt Frequency
F	none	Reset & hold complete prescaler		
E	(INT5 only)	**INT6 disabled,** INT5 still active		
D	INT6	$f_c / 2^3$	244.14 µs	4096 Hz
C	INT6	$f_c / 2^5$	976.56 µs	1024 Hz
B	INT6	$f_c / 2^7$	3.906 ms	256 Hz
A	INT6	$f_c / 2^9$	15.625 ms	64 Hz
9	INT6	$f_c / 2^{11}$	62.5 ms	16 Hz
8	INT5	reserved		
7	INT5	$f_c / 2^8$	7.81 ms	128 Hz
6	INT5	$f_c / 2^9$	15.625 ms	64 Hz
5	INT5	$f_c / 2^{10}$	31.25 ms	32 Hz
4	INT5	$f_c / 2^{11}$	62.5 ms	16 Hz
3	INT5	$f_c / 2^{12}$	125 ms	8 Hz
2	INT5	$f_c / 2^{13}$	250 ms	4 Hz
1	INT5	$f_c / 2^{14}$	500 ms	2 Hz
0	INT5	$f_c / 2^{15}$	1 s	1 Hz

The interrupt **INT6** may be disabled selectively using control code Eh without affecting the interval time of the **INT5** tap. The **INT6** multiplexer powers up in the disabled position. The programming of the **INT6** interrupt taps should be done synchronously, if different time base intervals are used temporarily (stop watch application, keyboard debouncing) or an accurate number of interrupts is required. To avoid the transmission of additional unwanted interrupts, the change of the **INT6** tap should be done in a time frame of 200 µs after the reception of a prescaler interrupt.

As illustrated in table 5 only the **INT6** tap can be disabled individually. Therefore special care has to be taken for **INT5**. In the case of programming the **INT6** tap without previously selecting an **INT5** tap (i.e. after power-on reset), an **INT5** frequency of 128 Hz is set by default. Concerning the program development using **INT6**, the following rules should be considered:

- Always program both prescaler interrupt taps,
- If only **INT6** is required, select the 1 Hz tap and define an empty **INT5** routine,
- Otherwise implement a “disable” flag in the **INT5** service routine.

2.4.1 Prescaler during SLEEP Mode

When the microcontroller enters the SLEEP mode, the µC’s internal clocks are halted. While the 32 kHz oscillator, LCD driver, and prescaler remain active, all µC actions are suspended. The microcontroller exits the SLEEP mode when an interrupt is generated by the prescaler (in addition to a logic low on an external interrupt, Port 5 input pin, or an external reset).

2.5 Low Power Modes

Two low power consumption modes of operation are available: SLEEP and STOP mode. These operating modes are initiated by executing the SLEEP instruction.

Note: The SLEEP instruction is not a normal instruction as its function is dependent on the state of the interrupt pending register. SLEEP is therefore available for use within the $AUTOSLEEP and $RESET routine only.

2.5.1 SLEEP Mode

By executing the SLEEP instruction (in the $AUTOSLEEP routine) the microcontroller enters a low power consumption mode. In this SLEEP mode, the programmable prescaler and the LCD driver remain active, while the internal RC oscillator (µC clock) is turned off causing all core processing to be stopped. It can only be kept when none of the interrupt pending or active register bits are set.

During the SLEEP mode, the I bit in the condition code register is set to enable all interrupts. All other registers, memory, and parallel input/output lines remain the same. The 32-kHz crystal oscillator is not switched off, but the prescaler or the LCD driver may be disabled by the application program. This mode will continue until any interrupt or reset is sensed. At this time the event is decoded and the program counter is loaded with the corresponding starting address of the interrupt or reset service routine.

The MARC4's unique **Auto-Sleep** feature allows the µC to enter the SLEEP mode automatically when the lowest priority interrupt service routine has been completed.

The SLEEP mode is a shutdown condition which is used to reduce the average system power consumption in applications where the µC is not fully utilised (figure 13). Using SLEEP and interrupts, the full computational speed of the core is always available. In this way, power is only consumed when needed, allowing the µC to run in high speed bursts from a weak supply (battery, capacitor, or even a solar cell).

Note: When **TST1** is tied to $\mathbf{V_{SS}}$ during power-on reset, the µC activity is observable at the **TCL** pin (using a low capacitance probe).

Calculating the average power consumption

The total power consumption is directly proportional to the active time of the µC. For a rough estimation of the expected average system current consumption, the following formula should be used:

$$I_{SYS} = I_{SLE} + \left(I_{DD} \times \frac{T_{active}}{T_{total}} \right)$$

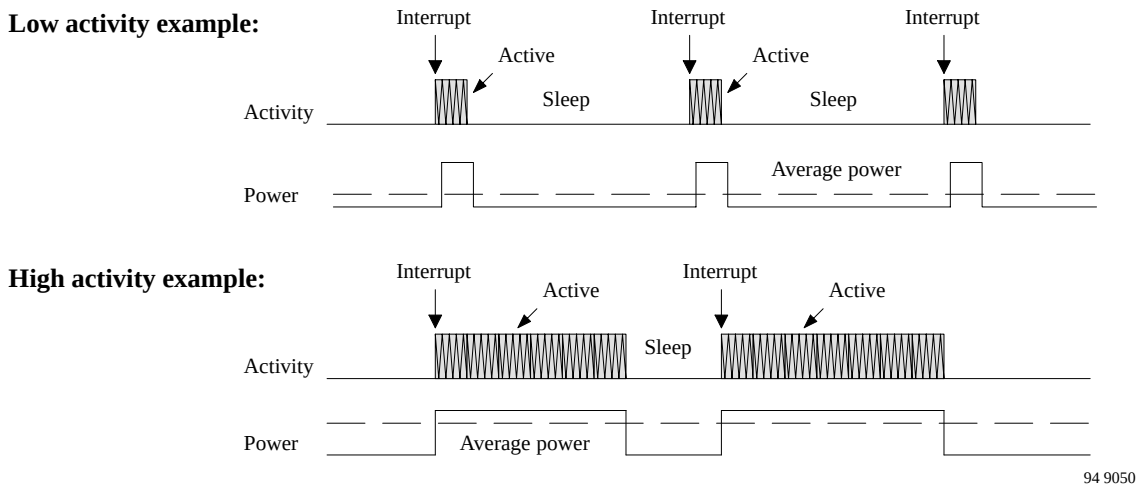


Figure 13. Average system power consumption and duty cycle

2.5.2 STOP Mode

The lowest power consumption mode of the microcontroller is entered with the STOP operation. The current consumption of the µC (without external loads) will be reduced to less than 1 µA at 3 Volts.

The STOP mode can be implemented by switching off the power supply of the crystal oscillator (**AV_{DD}**) with one of the port output lines (refer to figure 14). Before executing the STOP routine, the prescaler should be reset and the LCD driver should be put into the BLANKING mode, because both are turned off when the 32-kHz oscillator is switched off. The internal RC oscillator is stopped by the SLEEP instruction, suspending all further internal processing.

During the STOP mode, the I bit in the CCR is set to enable external interrupts. All other registers, memory, and all I/O lines remain unchanged. This continues until an external interrupt or reset is decoded. The program counter is loaded with the corresponding starting address of the interrupt or reset service routine respectively.

By writing a logic 1 to the corresponding port, the interrupt or reset service routine may turn on the crystal oscillator. The oscillator's start-up time in the range of several seconds (which depends on the operating temperature and supply voltage) must be kept in mind. Therefore the occurrence of the first prescaler interrupts might not be as accurate as usual.

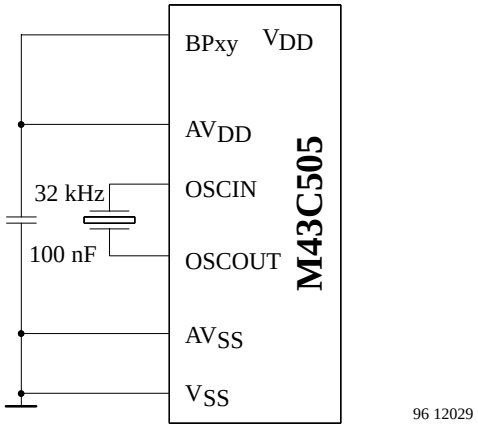


Figure 14. STOP mode application

3 Liquid Crystal Display Driver

This chapter describes the programming of the LCD driver. It also includes

- A discussion of a simple method of setting the LCD power supply voltages
- Information about the relationship between a typical 7-segment numeric display, the segment and back-plane outputs (for 2:1, 3:1, and 4:1 multiplex)
- Waveform examples for the different drive modes.

Figure 15 is a functional block diagram of the LCD driver circuitry. The internal I/O bus is connected to the LCD control register (Port 2) and the LCD data register (Port 3). The LCD driver interface to the programmer comprises these two output ports.

The LCD driver circuitry offers the following features:

- Drives up to 80 display segments
- Supports 5 Volt LCD panels over the full supply voltage range
- Built-in LCD voltage generation with temperature compensation (–8 mV/ ºC)
- Display continues when µC in SLEEP mode
- Programmable multiplex rate:
  Direct drive, 2:1, 3:1, or 4:1 multiplex mode

3.1 Display Data Register

The LCD data register receives the data from the µC and processes it in a 4-bit wide circular 20-stage shift register. The functional block diagram (figure 15) shows the order of the segment information and the way it has to be written into the shift register (starting with the 20-th segment).

A logic 1 in the shift register's bit-map indicates the ON state of the corresponding LCD segment. Similarly a logic 0 indicates the OFF state. There is a one to one correspondence between each stage of the shift register and the segment outputs, and between the individual bits of a register nibble and the backplane outputs. The LSB of each nibble correspond to the 20 segments operated with respect to backplane **COM0**. In multiplexed LCD applications the segment data of the second, third and fourth column of the shift register are time multiplexed with **COM1**, **COM2** and **COM3** respectively. The LCD specific segment decoding is done via qFORTH software routines, thus omitting the need for separate decoding circuitry.

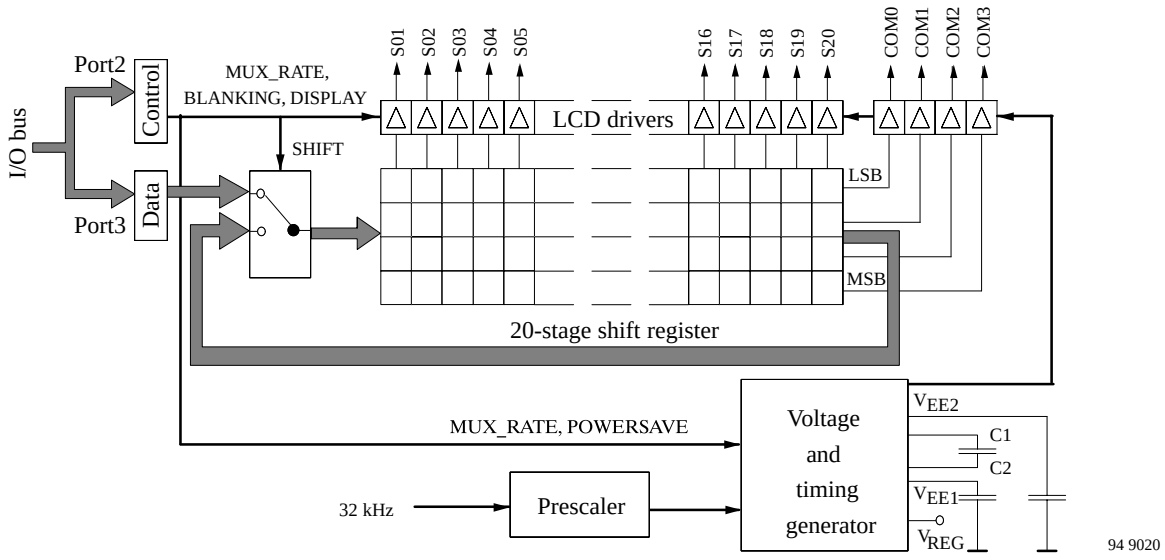


Figure 15. LCD driver – functional block diagram

3.2 LCD Control Register

The LCD control register receives the operation mode data at Port 2 to configure the LCD driver circuitry (refer to table 6).

Table 6. LCD driver – operation modes

Control Code	Operation Mode
0	DIRECT DRIVE
1	2:1 MULTIPLEX
2	3:1 MULTIPLEX
3	DISPLAY
4	CLEAR/INIT (4:1 MULTIPLEX)
5	MASK/SHIFT
6	BLANKING

3.2.1 Initializing the LCD Driver

At power-on reset the LCD driver circuitry is set automatically into BLANKING and 4:1 MULTIPLEX drive mode. After any reset condition, a proper operation of the LCD driver is ensured by writing the following control codes into the LCD control register:

- CLEAR/INIT
- Multiplex drive mode (if not 4:1 MULTIPLEX)

Four terms can be used to set the multiplex rate (refer to table 6). The CLEAR/INIT term initializes the LCD driver, setting it into the 4:1 multiplex drive mode. Therefore no extra control code is needed for 4:1 MULTIPLEX.

After any hardware reset the contents of the LCD display registers are undefined and should be initialized with the following instruction sequence:

- Write BLANKING to the LCD control register
- Write zero 20 times to the LCD data register
- Write DISPLAY to the LCD control register

3.2.2 LCD Driver - Modes of Operation

In normal time keeping applications the DISPLAY command might be given only once at the end of the first complete LCD display update (e.g. “Mo 12:00”). Afterwards a total display change consists only of 20 consecutive nibbles written to the LCD data register.

The BLANKING term causes a blank display and might be necessary before each new data transfer to the display registers. This is especially true when the µC is heavily loaded by a number of interrupt sources and the LCD update is handled as a base task. The BLANKING will be removed at the end of the data transfer by writing DISPLAY. If the DISPLAY command is not given, the BLANKING remains which allows the easy implementation of a blinking display.

When using the MASK/SHIFT term, only nibbles requiring an update need to be software decoded and written to the LCD data register. The data to be retained is simply shifted back to its original position, whilst new data nibbles are inserted in the appropriate position (refer to figure 15).

As an example for the effective use of the MASK/SHIFT term, the implementation of a 6 digit (3:1 multiplex) LCD panel test is described.

- Setup the LCD driver for 3:1 MULTIPLEX.
- Switch on all segments of the leading 7 segment digit (including the attenuator, see figure 21) with a complete LCD display update.
- After (half of) a second, write MASK/SHIFT to the LCD control register.
  Write three dummy values to the LCD data register to support the shift clock pulses. This operation will scroll the digit one position to the right.
- After a total of five operations, the digit appears in the right-most position and the (BLANKING or) DISPLAY term should be given to the control register to overwrite the MASK/SHIFT multiplexer configuration.

3.3 LCD Voltage and Timing Generator

The LCD voltage generator circuitry boosts the regulated liquid crystal display voltage ($\mathbf{V_{REG}}$) to the doubled and tripled voltage components ($\mathbf{V_{EE1}}$, $\mathbf{V_{EE2}}$) required by multiplexed liquid crystal displays. These voltage levels are applied to the driver circuitry (see figure 15).

Most 5 Volt LCD panels have a temperature coefficient of –8 mV/ºC. The temperature compensated reference for the LCD voltage booster circuitry ($\mathbf{V_{REG}}$), has the task of meeting this requirement directly, so the user gets the best LCD contrast over the full operating temperature and supply voltage range.

The external components for the LCD voltage generation (one pump and two storage capacitors) should be connected to the µC as shown in figure 16 .

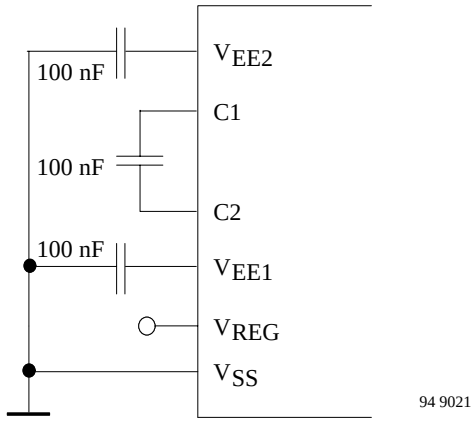


Figure 16. External components

For very small LCD panels the capacitor values may be reduced from 100 nF to 47 nF. The user has to connect the µC and the LCD as it will be in the final product in order to select the capacitor value. To examine the LCD driver waveforms an oscilloscope with a low capacitance probe should be used.

3.3.1 Maximum LCD Drive Capability

As a design guideline for large LCD panels, use the following basic formula to describe the flatening of the LCD segment and backplane driver outputs:

$$\tau = R \times C$$

Assuming the 1/4 duty, 1/3 bias LCD drive method up to 80 segments on the LCD panel is descibed in figure 26. The frame frequency at 1/4 duty is given as 64 Hz (16 ms) and each backplane will be active for 4 ms.

The decrease of the rise and fall time at the output waveform signals to be seen at higher LCD segment loads is given to 100 µs.

Any higher capacitive load will increase the average DC offset voltage. Please check this important parameter with your LCD supplier too. To improve the drive capabilty of the LCD driver the storage capacitors at V_{EE1} and V_{EE2} has to be increased to 220 nF.

Drive Capability of Each Backplane (COM0...3)

$R_{BPOmax} = 3\ k\Omega$

$$C_{BPmax} = \frac{100\ \mu s}{3\ k\Omega} = 33\ nF$$

for 20 segments per backplane driver. Therefore the maximum capacitive load per segment is around 1.6 nF.

Drive Capability of Segment Outputs (S01...S20)

$R_{SEGOmax} = 6\ k\Omega$

$$C_{SEGmax} = \frac{100\ \mu s}{6\ k\Omega} = 16.5\ nF$$

for 4 segments per segment driver. The maximum capacitive load per segment driver could be up to 4 nF.

Example:

Based on a total height of 30 mm, a normal segment may have the dimensions of 15 mm x 4 mm = 60 mm^2. Therefore the capacitance/mm^2 of the selected LCD panel has to be 1.65 nF/60 $mm^2 \leq 27$ pf/mm^2.

3.4 Direct Drive Mode

The static LCD drive mode is used when a single backplane is provided at the LCD.

The LSB of each stage of the display shift register directly maps to the corresponding segment driver.

Sample backplane and segment drive waveforms for this mode are shown in figure 17.

The following formulas are valid in the DIRECT DRIVE mode at any instant (t):

$V_{state1}(t) = V_{S01}(t) - V_{COM0}(t)$

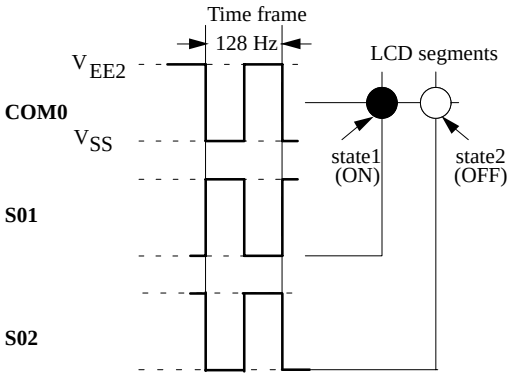
$V_{state2}(t) = V_{S02}(t) - V_{COM0}(t)$

$V_{on(rms)} = V_{EE2}$

$$V_{off(rms)} = \frac{V_{EE2}}{3} = V_{REG}$$

==> Contrast ratio = 3.0

(a) Waveform at driver



(b) Resultant waveforms at LCD segment

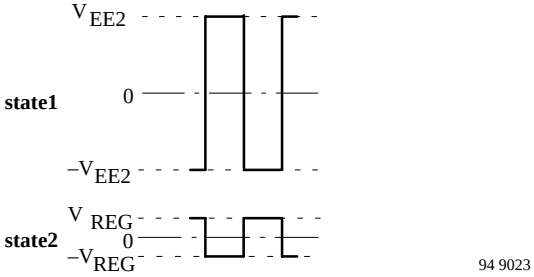


Figure 17. Direct drive mode waveforms

3.5 2:1 Multiplex Drive Mode

Figure 18 shows the connection of a 2:1 multiplex 5 digit LCD panel having the numeric display pattern shown in figure 19, the segment outputs (**S01**-**S20**), and the backplane outputs (**COM0**, **COM1**).

In the example “456.78” is displayed on the LCD panel and the corresponding contents of the display data register is shown.

Backplane and segment drive waveforms for this mode are shown in figure 20.

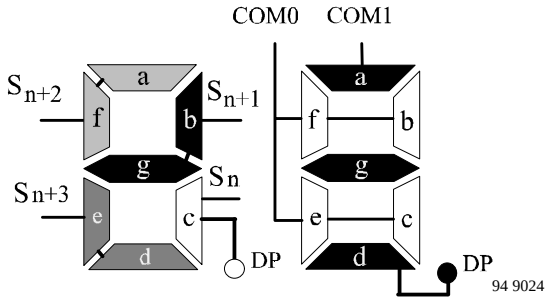


Figure 18. 2:1 Multiplex 7 segment digit

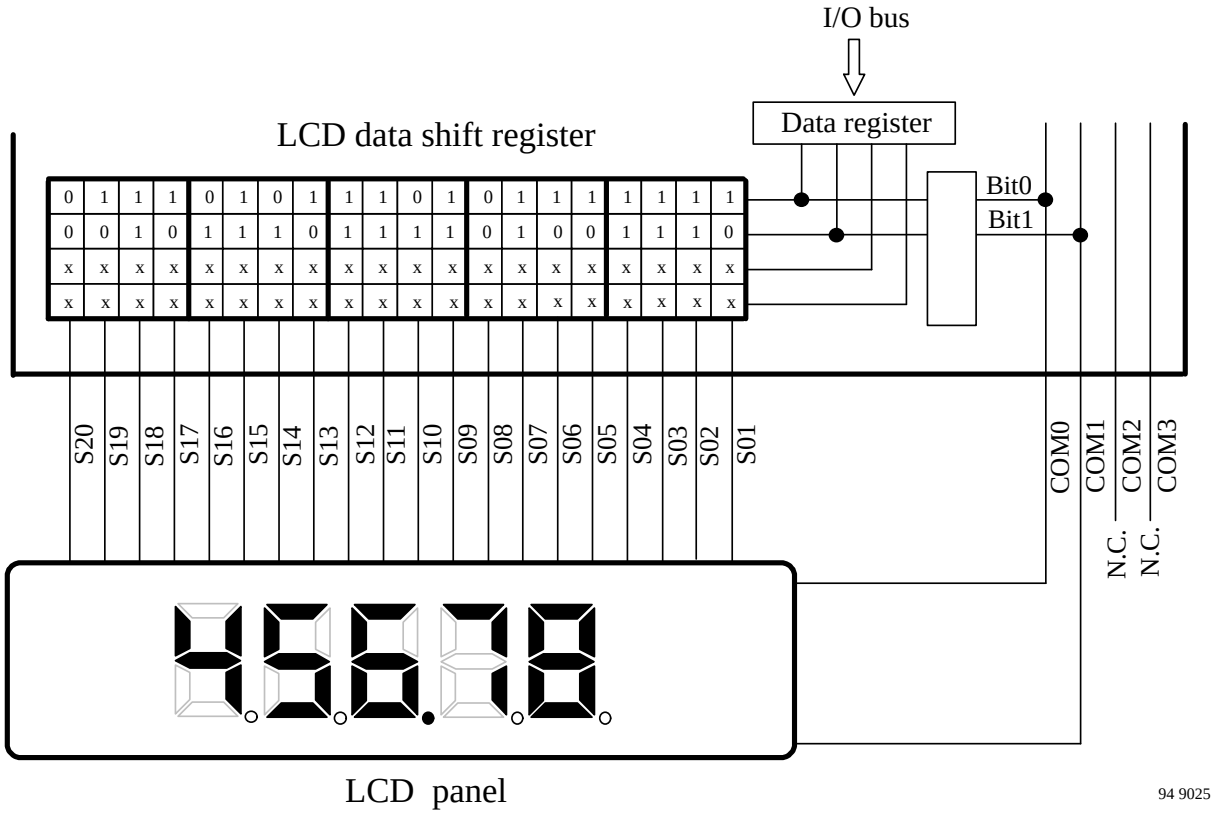
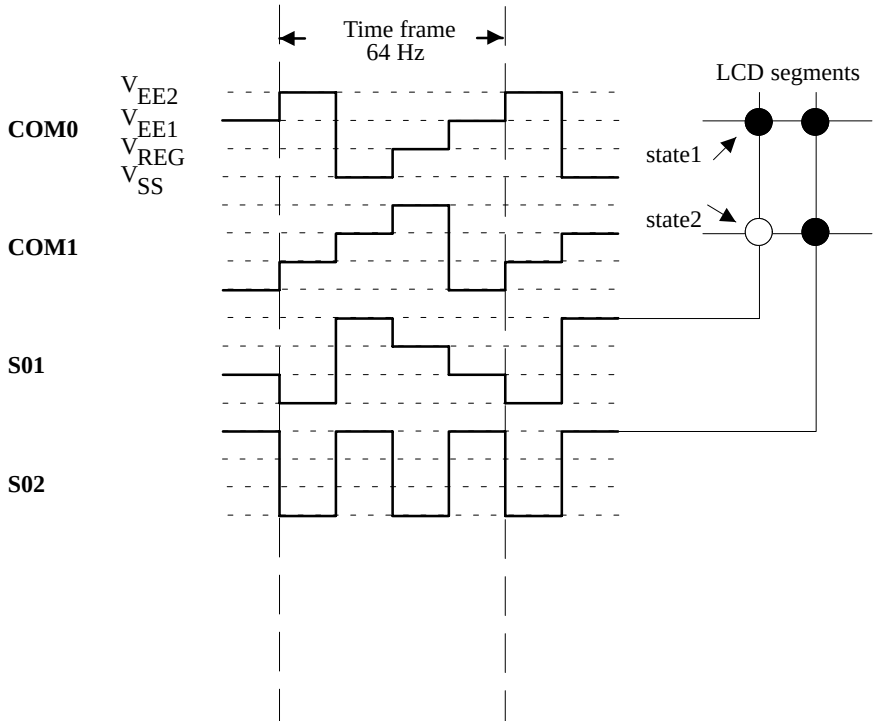


Figure 19. 2:1 Multiplexer LCD panel connection

(a) Waveforms at driver



(b) Resultant waveforms at LCD segment

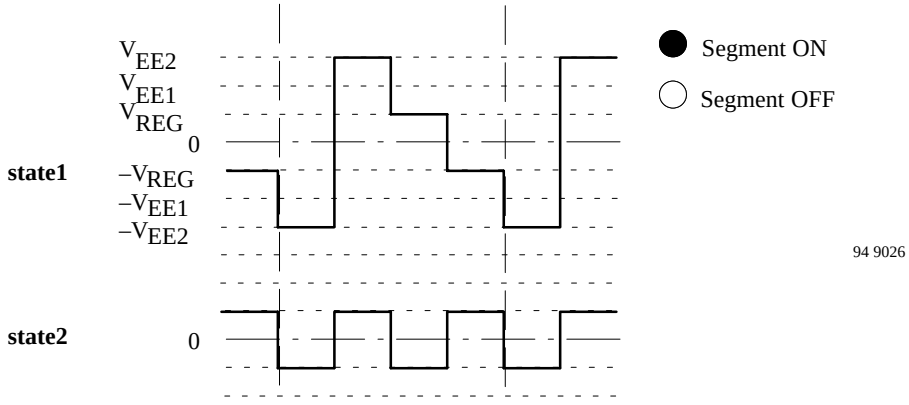


Figure 20. Waveforms for 2:1 multiplex drive mode

The following formulas are valid in the 2:1 multiplex drive mode at any instant (t):

$V_{state1}(t) = V_{S01}(t) - V_{COM0}(t)$ and
$V_{state2}(t) = V_{S01}(t) - V_{COM1}(t)$

$$V_{on(rms)} = \frac{V_{EE2}}{3}\sqrt{5} = 0.745\ V_{EE2} \text{ and } V_{off(rms)} = \frac{V_{EE2}}{3}$$

Contrast ratio = $V_{on(rms)} / V_{off(rms)} = 2.23$

3.6 3:1 Multiplex Drive Mode

Figure 21 shows the connection of a 3:1 multiplex 6 3/4 digit LCD panel having the numeric display pattern shown in figure 22, the segment outputs (**S01**-**S20**), and the backplane outputs (**COM0**-**COM2**).

In the example, “123456.7” is displayed (with a max. displayable value of “3999999”) and the corresponding contents of the LCD display data register is shown.

Backplane and segment drive waveforms for this mode are shown in figure 23.

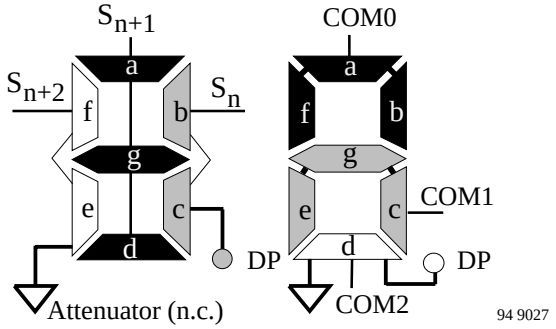


Figure 21. 3:1 multiplex 7 segment digit

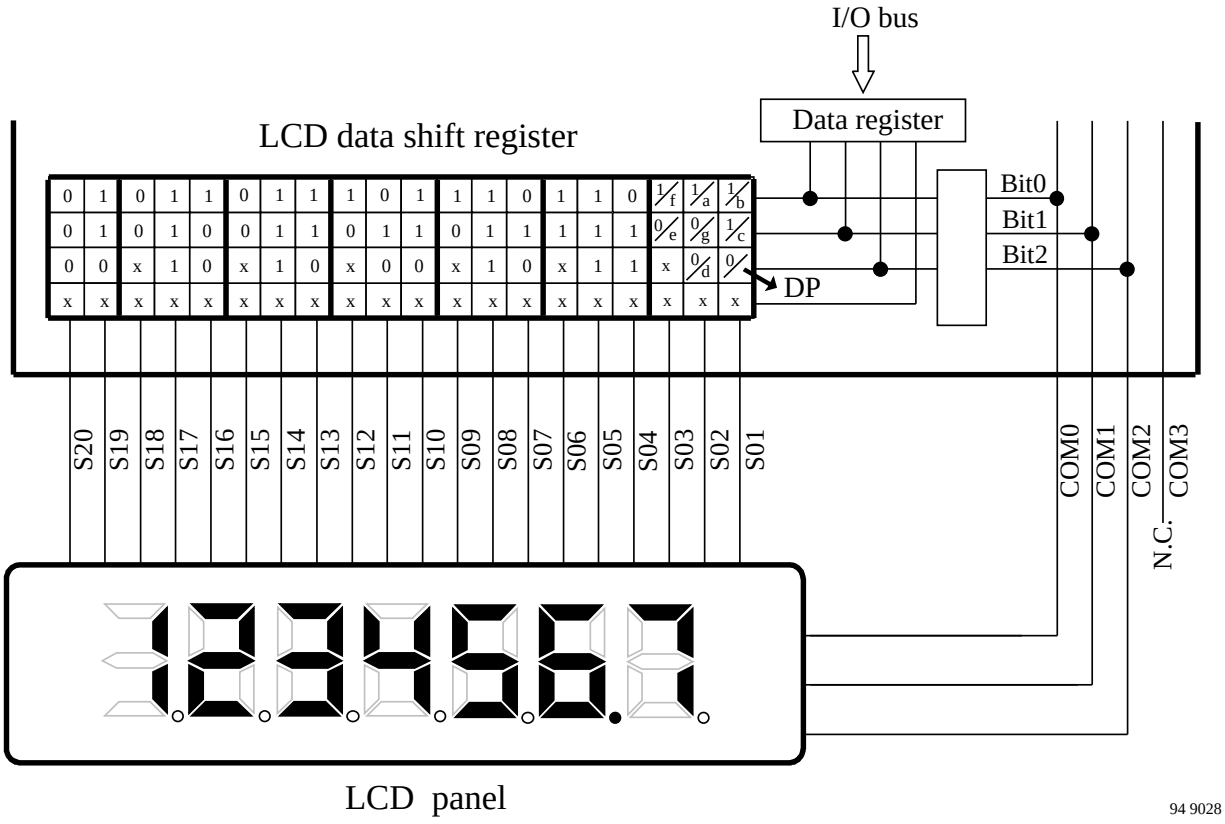


Figure 22. 3:1 Multiplexer LCD panel connection

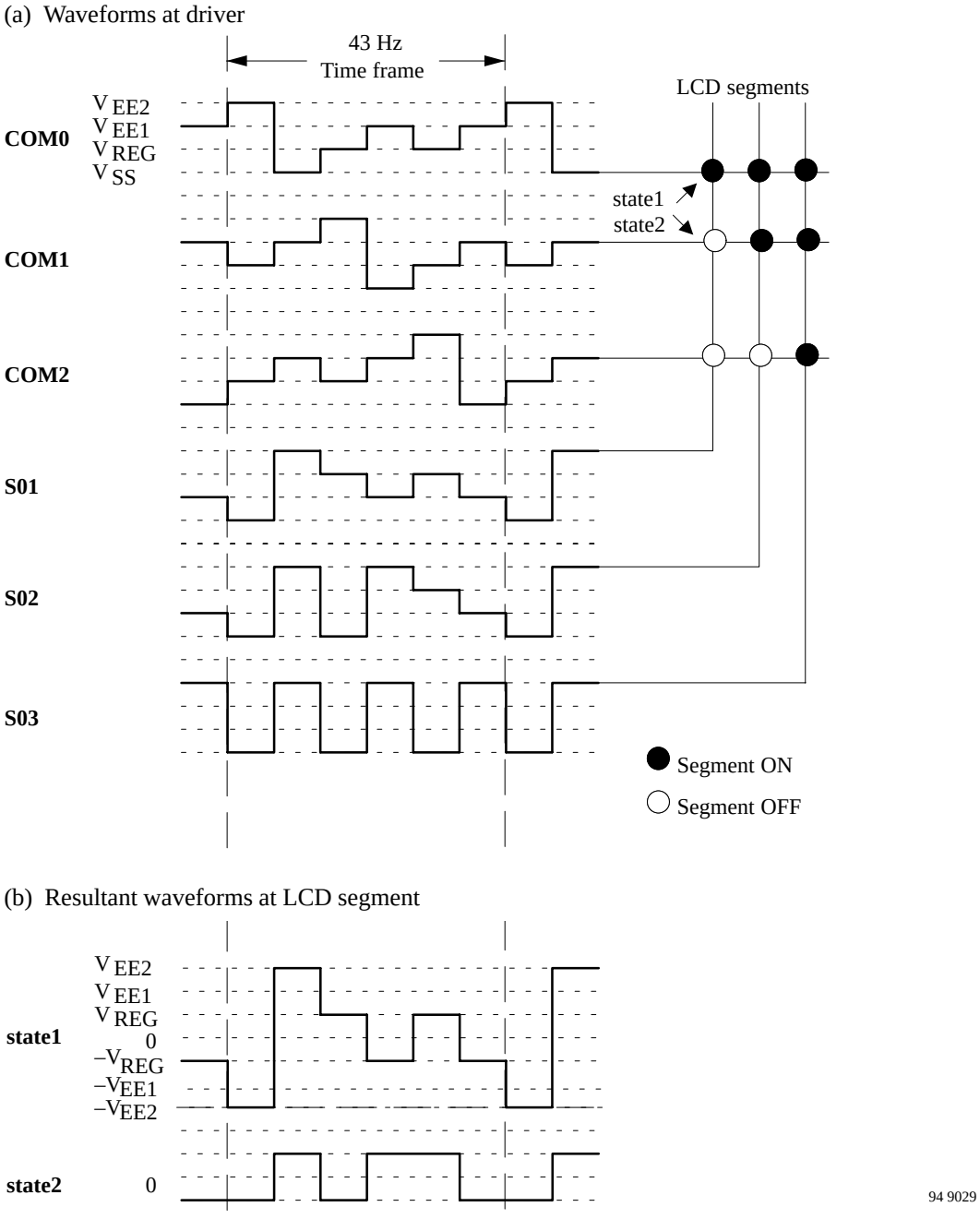


Figure 23. Waveforms for 3:1 multiplex drive mode

The following formulas are valid in the 3:1 multiplex drive mode at any instant (t):

$V_{state1}(t) = V_{S01}(t) - V_{COM0}(t)$ and
$V_{state2}(t) = V_{S01}(t) - V_{COM1}(t)$

$$V_{on(rms)} = \frac{V_{EE2}}{9}\sqrt{33} = 0.638\ V_{EE2} \text{ and } V_{off(rms)} = \frac{V_{EE2}}{3}$$

Contrast ratio = $V_{on(rms)} / V_{off(rms)} = 1.915$

3.7 4:1 Multiplex Drive Mode

Figure 24 shows the connection of a 4:1 multiplex 10 digit LCD panel having the numeric display pattern shown in figure 25, the segment outputs (**S01**-**S20**), and the backplane outputs (**COM0**-**COM3**).

In the example, “123456.7890” is displayed and the corresponding contents of the LCD display data register is shown.

Backplane and segment drive waveforms for this mode are shown in figure 26.

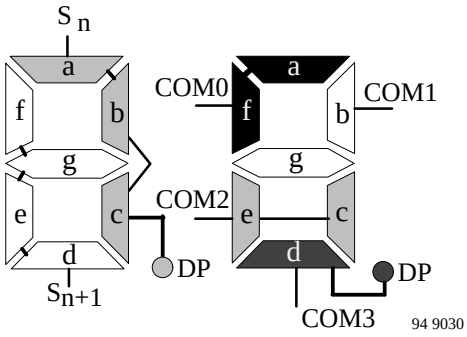


Figure 24. 4:1 Multiplex 7 segment digit

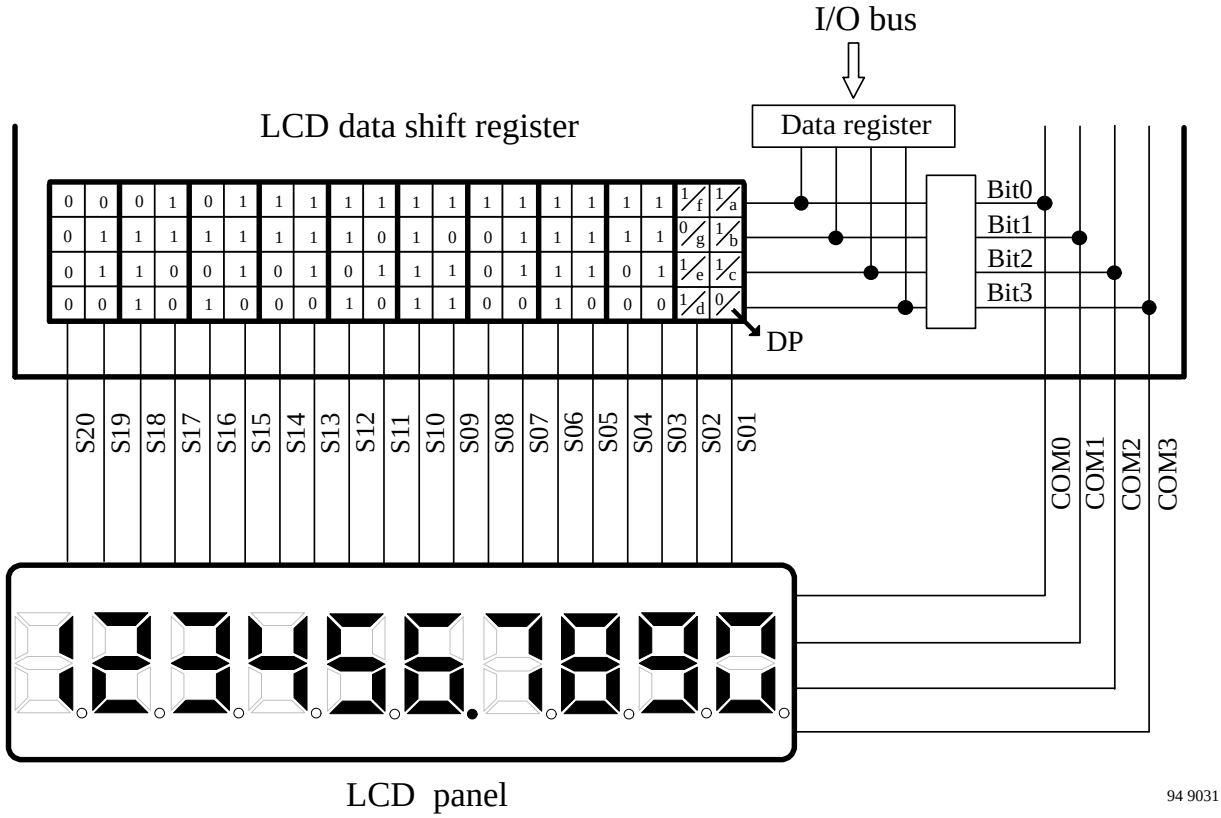
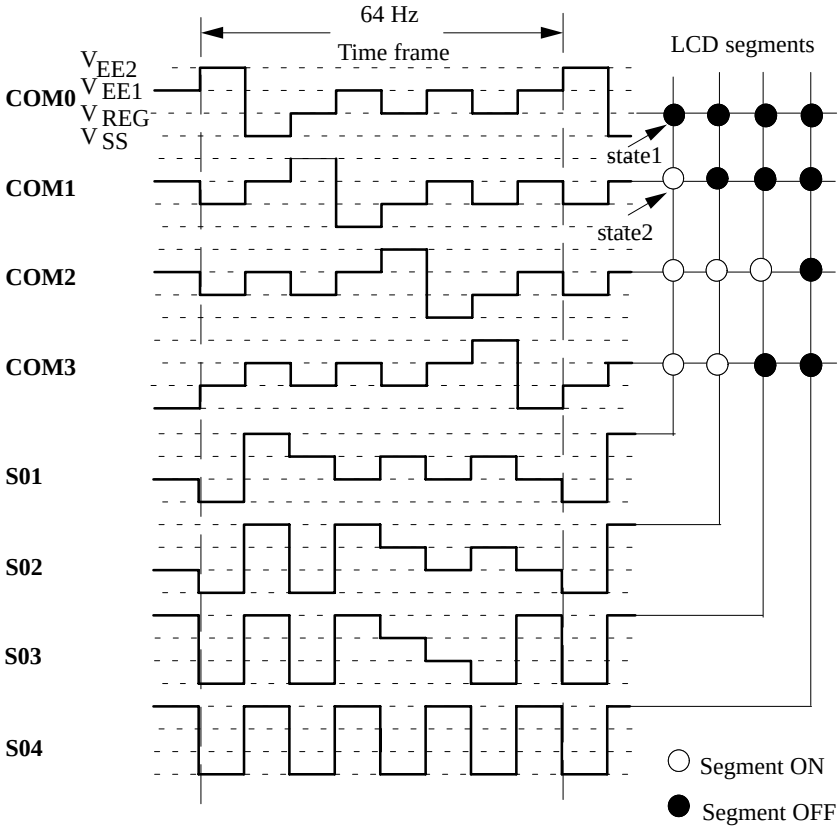
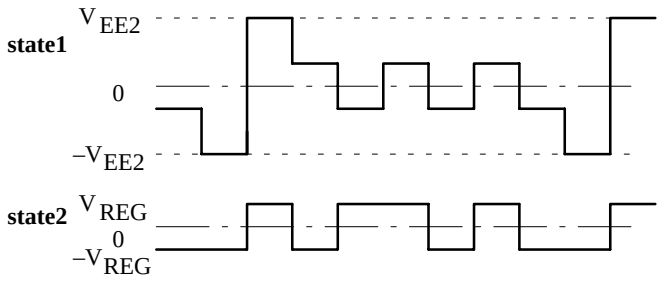


Figure 25. 4:1 Multiplexer LCD panel connection

(a) Waveforms at driver



(b) Resultant waveforms at LCD segment



94 9032

Figure 26. Waveforms for 4:1 multiplex drive mode

The following formulas are valid in the 4:1 multiplex drive mode at any instant (t):

$V_{state1}(t) = V_{S01}(t) - V_{COM0}(t)$ and
$V_{state2}(t) = V_{S01}(t) - V_{COM1}(t)$

$$V_{on(rms)} = \frac{V_{EE2}}{3}\sqrt{3} = 0.577\ V_{EE2} \text{ and } V_{off(rms)} = \frac{V_{EE2}}{3}$$

Contrast ratio = $V_{on(rms)} / V_{off(rms)} = 1.732$

4 Electrical Specification

4.1 Absolute Maximum Ratings

All voltages are given relative to V_{SS}. The circuit is protected against supply voltage reversal for typically 5 minutes.

Parameters	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Input voltage (on any pin)	V_{IN}	V_{SS}–0.3 ≤ V_{IN} ≤ V_{DD}+0.3	V
Output short circuit duration	t_{short}	indefinite	sec
Operating temperature range	T_{amb}	–20 to +80	°C
Storage temperature range	T_{stg}	–40 to +125	°C
Thermal resistance (PLCC)	θ_{JA}	70	°C/W
Maximum solder temperature	T_{sld}	260 (t ≤ 10 sec)	°C

Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operational section of these specification is not implied. Exposure to absolute maximum rating condition for an extended period may affect device reliability. All inputs and outputs are protected against high electrostatic voltages or electric fields. However, precautions to minimize built-up of electrostatic charges during handling are recommended. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g., V_{DD}).

4.2 DC Operating Characteristics, V_{DD} = 3 V

Supply voltage $\mathbf{V_{DD} = 3.0\ V, V_{SS} = 0\ V, T_{amb} = +25°C}$ unless otherwise specified. All voltage levels are measured with reference to $\mathbf{V_{SS}}$ and current flowing into the device is positive. Typical parameters represent the statistical mean values.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage		V_{DD}	2.4	3.0	3.6	V
Active current	Note 1	I_{DD}		1.4	2.5	mA
Sleep current	Note 2	I_{SLE}	2.0	3.0	5.0	µA
Supply current quotient	Note 3	$\frac{\lvert I_{DD}\rvert}{SYSCL}$	0.7	0.8	0.9	$\frac{mA}{MHz}$
RC oscillator frequency (system clock)	Note 5, 8 (see figure 29)	SYSCL	0.9	1.75	2.8	MHz
	V_{DD} = 2.4 V		0.5	0.75		MHz
Internal power-on reset						
POR voltage	Note 4, 8 (see figure 31)	V_{POR}		1.8	2.2	V
POR voltage hysteresis	Note 8	ΔV_{POR}		–100		mV
Output pads						
Hi–Z leakage current	Open drain	I_{OZ}		±20	±100	nA
Output capacitance	Note 8	C_{OUT}		5	10	pF
Input pads (except NRST and OSCIN under test conditions)						
Input voltage high		V_{IH}	0.8*V_{DD}		V_{DD}	V
Input voltage low		V_{IL}	V_{SS}		0.2*V_{DD}	V
Input current low	V_{IN} = V_{SS}; no pull up	I_{ILO}		±20	±100	nA
Input current high	V_{IN} = V_{DD}	I_{IH}		±20	±100	nA
Input capacitance	Note 8	C_{IN}		5	10	pF

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
NRST and OSCIN input pads under test conditions						
Input voltage high		V_{IH}	V_{DD}		V_{DD}	V
Input voltage low		V_{IL}	V_{SS}		V_{SS}	V
Bidirectional Ports 0, 1, 4, outputs NST, OD and buzzer						
Input current low **)	$V_{IN} = V_{SS}$	I_{IL}	–0.8	–1.6	–3	µA
Output current high	V_{OH} = 2.4 V	I_{OH}	0.8	–1.3		mA
Output current low	V_{OL} = 0.6 V	I_{OL}	1.5	2.4		mA
Input Port 5						
Input current low **)	$V_{IN} = V_{SS}$	I_{IL}	–6	–13	–20	µA
NRST input						
Input current low	$V_{IN} = V_{SS}$	I_{IL}		–8	–16	µA
Interrupt Schmitt-trigger input INT2, INT7						
Input current low **)	$V_{IN} = V_{SS}$	I_{IL}	–6	– 11	–20	µA
Negative going threshold voltage	Note 8	VT–		1.1		V

) **I_{IL} values are only valid if the pull-up resistor is optioned in.

4.3 DC Operating Characteristics, V_{DD} = 5 V

Supply voltage **V_{DD} = 5.0 V, V_{SS} = 0 V, T_{amb} = +25°C** unless otherwise specified. All voltage levels are measured with reference to **V_{SS}** and current flowing into the device is positive. Typical parameters represent the statistical mean values.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage		V_{DD}	2.4	5	5.5	V
Active current	Note 1	I_{DD}		7	15	mA
Sleep current	Note 2	I_{SLE}	3	7	10	µA
Supply current quotient	Note 3, 8	$\frac{\lvert I_{DD}\rvert}{SYSCL}$		2	2.1	$\frac{mA}{MHz}$
RC oscillator frequency	Note 5, 8	SYSCL	2	3.5		MHz
Internal power-on reset						
Power–on reset voltage	Note 4, 8 (see figure 31)	V_{POR}		1.8	2.2	V
POR voltage hysteresis	Note 8	ΔV_{POR}		–100		mV
Output pads						
Hi–Z leakage current	Open drain	I_{OZ}		±20	±300	nA
Output capacitance	Note 8	C_{OUT}		5	10	pF
Input pads (except OSCIN and NRST under test conditions)						
Input voltage high		V_{IH}	0.8*V_{DD}		V_{DD}	V
Input voltage low		V_{IL}	V_{SS}		0.2*V_{DD}	V
Input current low	$V_{IN} = V_{SS}$; no pull up	I_{ILO}		±20	±300	nA
Input current high	$V_{IN} = V_{DD}$	I_{IH}		±20	±300	nA
Input capacitance	Note 8	C_{IN}		5	10	pF
NRST and OSCIN input pads under test conditions						
Input voltage high		V_{IH}	V_{DD}		V_{DD}	V
Input voltage low		V_{IL}	V_{SS}		V_{SS}	V

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Bidirectional Ports 0, 1, 4, outputs NST, OD and buzzer						
Input current low **)	$V_{IN} = V_{SS}$	I_{IL}	–3	–5.5	–8	µA
Output current high	V_{OH} = 4 V	I_{OH}	–1.2	–2		mA
Output current low	V_{OL} = 1 V	I_{OL}	2.5	3.5		mA
Input port 5						
Input current low **)	$V_{IN} = V_{SS}$	I_{IL}	–25	–45	–60	µA
NRST input						
Input current low	$V_{IN} = V_{SS}$	I_{IL}		–25	–50	µA
Interrupt Schmitt-trigger input INT2, INT7						
Input current low **)	$V_{IN} = V_{SS}$	I_{IL}	–20	–37.5	–60	µA
Negative going threshold voltage	Note 8	VT–		1.6		V

) **I_{IL} values are only valid if the pull-up resistor is optioned in.

4.4 DC Operating Characteristics, V_{DD} = 2.4 to 5.5 V, T_{amb} = +25°C

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
LCD driver **[5V LCD panel]**	**Segment outputs: S01 ... S20** **Backplane outputs: COM0 ... COM3**					
Regulated voltage	Note 6	V_{REG}	1500	1650	1800	mV
Doubler voltage	V_{REG} = 1650 mV	V_{EE1}	3000	3300	3600	mV
Tripler voltage	V_{REG} = 1650 mV	V_{EE2}	4500	4850	5400	mV
Temperature compensation relative to $V_{REG;}$	Note 8	T_{REG}	–7	–8	–9	mV/°C
Backplane frequency	4:1 multiplex 3:1 multiplex 2:1 multiplex Direct drive	f_{BP}		64 43 64 128		Hz Hz Hz Hz
Segment output resistance	ΔV_{SEG} = 100 mV; Note 8	R_{SO}	3.5	4.5	6	kΩ
Backplane output resistance	ΔV_{BP} = 100 mV; Note 8	R_{BO}	1.7	2.25	3	kΩ
Average DC offset	Note 8	V_{DC}		50	100	mV
Quartz oscillator						
Frequency	C_L = 10 pF	f_C		32,768		Hz
Integrated input capacitance	Note 8	C_{IN}		20		pF
Integrated output capacitance	Note 8	C_{OUT}		23.5		pF
Stability	AV_{DD} = 100 mV; Note 8	Δf/f		0.1	1	ppm
Start-up time	AV_{DD} = 3.0 V	t_{SQ}		2	4	sec

4.5 DC Electrical Characteristics, V_{DD} = 3 V

V_{DD} = 3 V±10%, V_{SS} = 0 V, T_{amb} = –10°C to +75°C, unless otherwise specified.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Active current	Note 1	I_{DD}		1.5	3	mA
Sleep current	Note 2	I_{SLE}		4	7	µA
Supply current quotient	Note 3	$\frac{\lvert I_{DD}\rvert}{SYSCL}$		0.8	0.9	$\frac{mA}{MHz}$
RC oscillator frequency (system clock)	Note 5	SYSCL	0.8	1.6		MHz
	V_{DD} = 2.4 V		0.4	0.75		MHz
Internal power-on reset						
POR voltage	Note 4	V_{POR}	1.2	1.8	2.4	V
Bidirectional Ports 0, 1, 4 outputs NST, OD and buzzer						
Input current low **)	$V_{IN} = V_{SS}$	I_{IL}	–0.6	–1.6	– 3.2	µA
Output current high	V_{OH} = 2.4 V	I_{OH}	–0.7	–1.4	– 2.1	mA
Output current low	V_{OL} = 0.6 V	I_{OL}	1.5	2.5	3.5	mA
Input Port 5						
Input current low **)	$V_{IN} = V_{SS}$	I_{IL}	–5	–15	– 25	µA
NRST input						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–3	–8	– 15	µA
Interrupt Schmitt-trigger input INT2, INT7						
Input current low **)	$V_{IN} = V_{SS}$	I_{IL}	–5	–12	– 20	µA

**) I_{IL} values are only valid if the pull-up resistor is optioned in.

Notes:

- All values shown reflect average measurements.
- Typical values at midpoint of voltage range, +25°C only.
- Data is for design guidance only and is not tested for, or guaranteed by TEMIC.

4.6 DC Electrical Characteristics, V_{DD} = 5 V

V_{DD} = 5 V±10%, V_{SS} = 0 V, T_{amb} = –10°C to +75°C, unless otherwise specified.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Active current	Note 1	I_{DD}		8	15	mA
Sleep current	Note 2	I_{SLE}		7	11	µA
Supply current quotient	Note 3	$\frac{\lvert I_{DD}\rvert}{SYSCL}$		2	2.5	$\frac{mA}{MHz}$
RC-oscillator frequency	Note 5	SYSCL	1.5	3.5	8	MHz
Internal power-on reset						
POR voltage	Note 4	V_{POR}	1.2	1.8	2.4	V
Bidirectional Ports 0, 1, 4, outputs NST, OD and buzzer						
Input current low **)	$V_{IN} = V_{SS}$	I_{IL}	–2.5	– 5.5	–9.0	µA
Output current high	V_{OH} = 4 V	I_{OH}	–1.0	–2.2	–4.0	mA
Output current low	V_{OL} = 1 V	I_{OL}	2.0	3.7	6.0	mA

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Input Port 5						
Input current low **)	$V_{IN} = V_{SS}$	I_{IL}	–15	–45	–70	µA
NRST input						
Input current low	$V_{IN} = V_{SS}$	I_{IL}	–10	–25	–70	µA
Interrupt Schmitt-trigger input INT2, INT7						
Input current low **)	$V_{IN} = V_{SS}$	I_{IL}	–15	–40	–70	µA

**) I_{IL} values are only valid if the pull-up resistor is optioned in.

Notes:

- All values shown reflect average measurements.
- Typical values at midpoint of voltage range, +25°C only.
- Data is for design guidance only and is not tested for, or guaranteed by TEMIC.

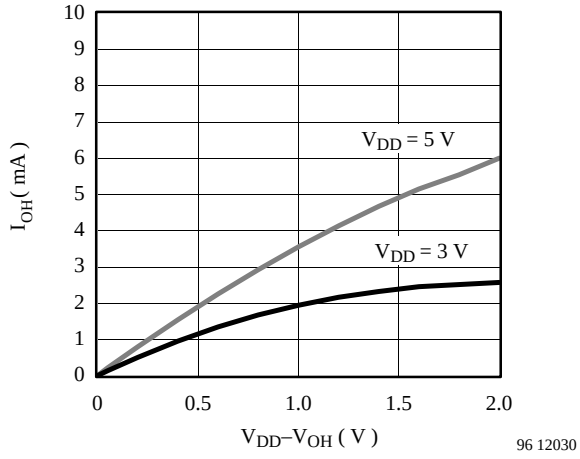


Figure 27. Typical I_{OH} vs. V_{DD}–V_{OH} for all ports

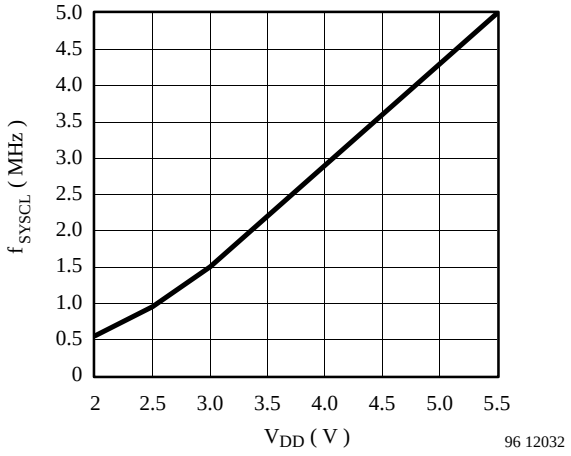


Figure 29. Typical system clock frequency SYSCL vs. supply voltage (internal RC oscillator)

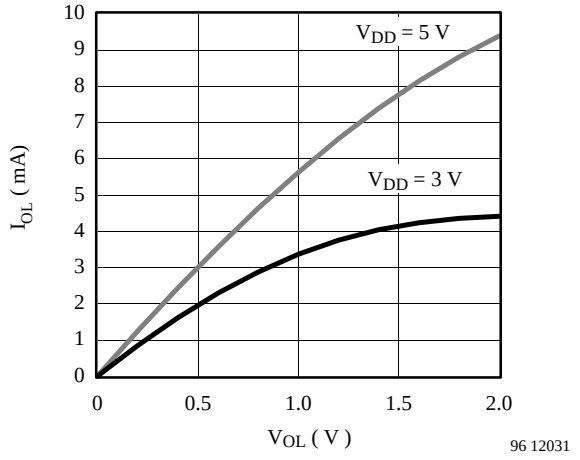


Figure 28. Typical I_{OL} vs. V_{OL} for all ports

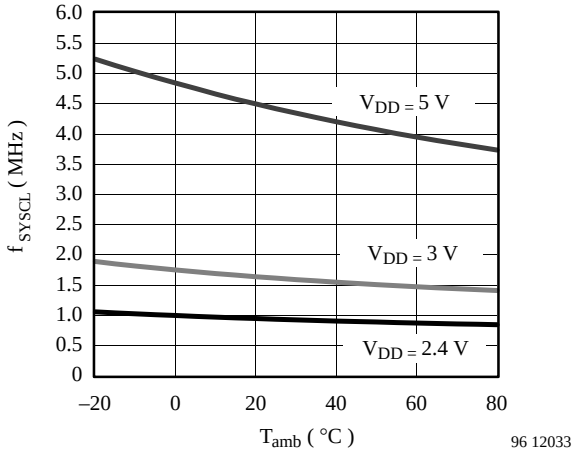


Figure 30. Typical SYSCL frequency vs. temperature

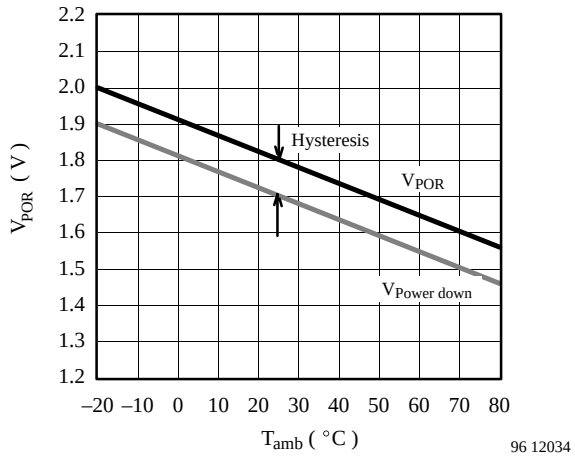


Figure 31. Power-on reset voltage vs. temperature

Note 1: Maximum active current (I_{DD})

This is the current observed at the V_{SS} pin with the crystal oscillator, the LCD driver and µC core permanently active. No output loads, all input ports and interrupt inputs connected to V_{DD} and the prescaler is reset. This mode can be achieved by connecting the **NRST** pin to V_{SS}.

The average system current of an application can be estimated with the formula:

$$I_{SYS} = I_{SLE} + \frac{\text{Duty cycle}}{100\%} \text{ x } I_{DD}$$

whereby

$$\text{Duty cycle} = \frac{\text{Active time x } 100\%}{(\text{Sleep time} + \text{Active time})}$$

I_{DD} = 1.4 mA ; I_{SLE} = 4 µA at 3 Volts.

In 'time keeping mode' the duty cycle is less than 1%, which gives a current consumption of about 18 µA at 3 V.

Note 2: Sleep current (I_{SLE})

This is the current taken with the crystal oscillator and the LCD driver active, the prescaler reset, the µC core in SLEEP mode and all input ports, bidirectional ports (if in input mode) and interrupts connected to V_{DD}. This state can, unless catered for in the application program, only be permanently achieved under production test conditions.

Note 3: Supply current quotient

Normalized active current relative to the core's operation frequency SYSCL.

The frequency of the integrated RC oscillator depends on the supply voltage as well as on the process parameters (i.e. sum of threshold voltages).

Note 4: Power-on reset voltage (V_{POR})

This is the supply voltage, which must be exceeded for the internal power on reset circuit to be released. The switching function can be observed on the **NRST** pin.

Note 5: Core oscillator frequency (f_{SYSCL})

The RC oscillator provides the central clocking of the core and the frequency varies with supply voltage and temperature to track the optimum performance of the µC. This frequency can be measured on the **TCL** pin by connecting the **NRST** and **TST1** pins to V_{SS}.

Note 6: LCD voltages are measured with

– 100 nF capacitor between **C1** and **C2**

– 100 nF capacitor between V_{EE1} and V_{SS}

– 100 nF capacitor between V_{EE2} and V_{SS}.

A load capacitance of 200 pF is connected between each backplane and V_{SS}.

The regulated and temperature compensated LCD voltage V_{REG} can also be supplied from an external voltage source through the V_{REG} pin, as long as the externally supplied voltage is larger than the internally generated voltage. It is also possible to supply all three LCD voltage levels through the pads V_{REG}, V_{EE1} and V_{EE2} as it is done under production test conditions.

Note 8: Measurement not subject to production test.

5 Mechanical Data

This chapter contains the pad layout and pad coordinates. The pin assignments for the 64 pin plastic QFP is shown in figure 2, page 2. The 64 pin ceramic DIL package used for emulation and prototyping purposes is also included.

5.1 Emulation Package

The pin-out of the emulation and prototype devices are compatible to the piggyback device M40C505

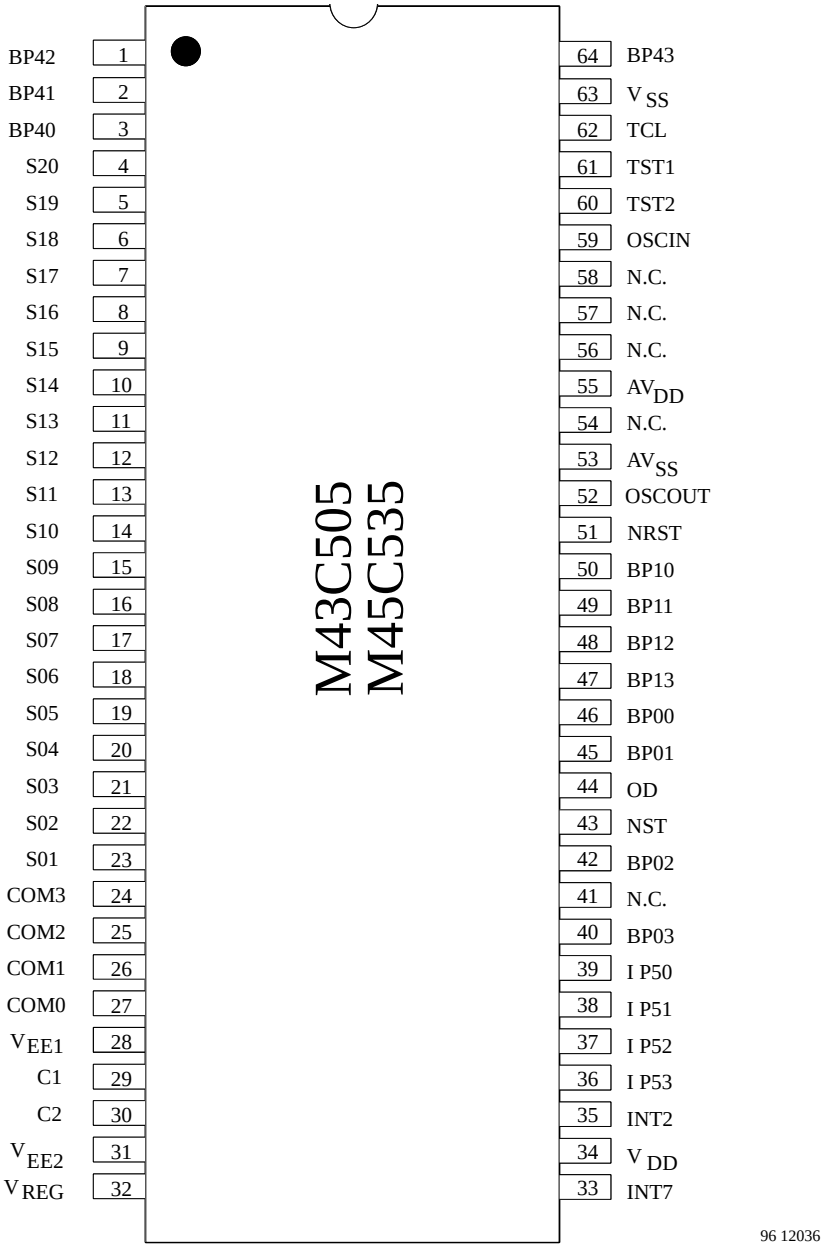


Figure 32. M43C505 / M45C535 in 64 pin ceramic DIL

5.2 Pad Layout

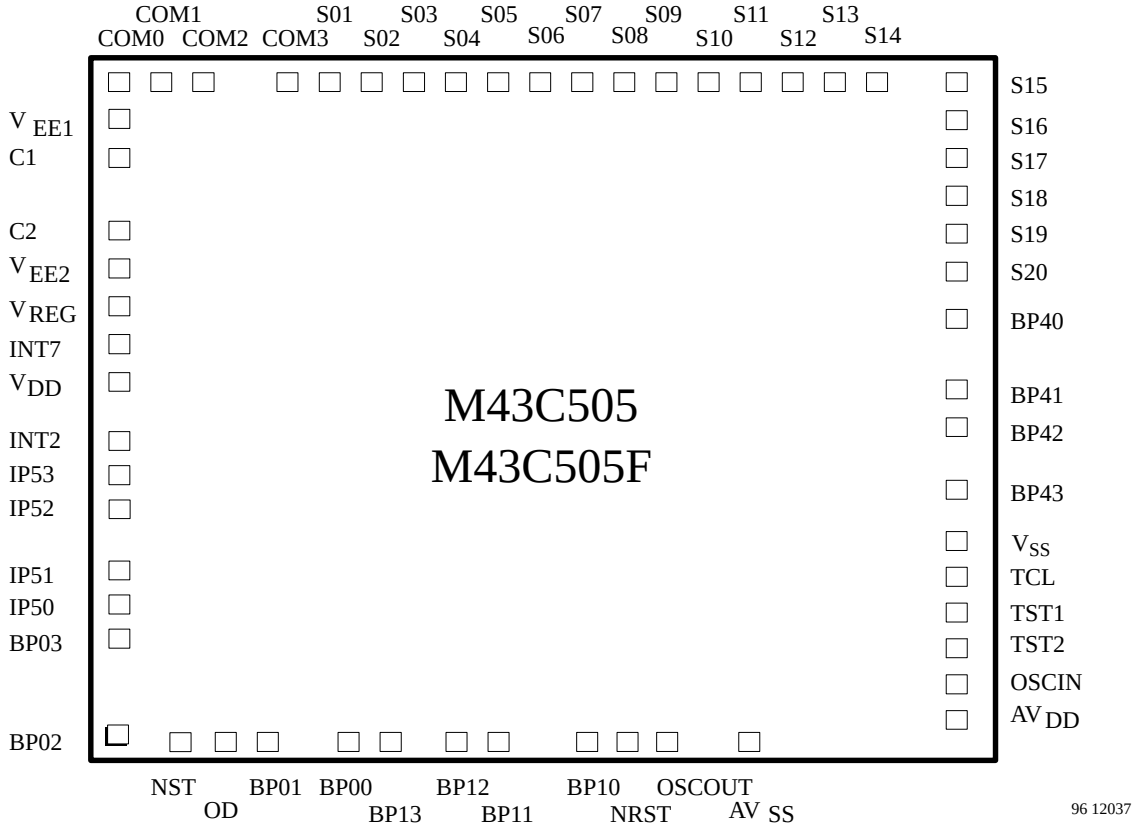


Figure 33. M43C505 pad layout

5.3 Pad Coordinates

M43C505:

The M43C505 is available in die form for COB mounting. Therefore the substrate, i.e. the backside of the die, should be connected to $\mathbf{V_{SS}}$.

Die size: 3.84×3.59 mm = 13.8 mm^2 (incl. scribe)
Pad size: 100×100 µm
Thickness: 480 ± 25 µm (= 19 ± 1 mil)

M43C505F:

The M43C505D is available in bar die form for COB mounting only. Therefore the substrate, i.e. the backside of the die, should be connected to $\mathbf{V_{SS}}$.

Die size: 3.84×3.57 mm = 13.7 mm^2 (incl. scribe)
Pad size: 100×100 µm
Thickness: 480 ± 20 µm

Table 7. Pad coordinates **M43C505**

No.	Name	X Point	Y Point	No.	Name	X Point	Y Point
1	**BP02**	0	0	31	**S12**	2728.0	3036.8
2	**NST**	202.0	0	32	**S11**	2562.0	3036.8
3	**OD**	380.8	0	33	**S10**	2386.0	3036.8
4	**BP01**	556.8	0	34	**S09**	2220.0	3036.8
5	**BP00**	889.6	0	35	**S08**	2044.0	3036.8
6	**BP13**	1065.6	0	36	**S07**	1878.0	3036.8
7	**BP12**	1364.4	0	37	**S06**	1702.0	3036.8
8	**BP11**	1540.4	0	38	**S05**	1536.0	3036.8
9	**BP10**	1847.2	0	39	**S04**	1360.0	3036.8
10	**NRST**	2023.2	0	40	**S03**	1194.0	3036.8
11	**OSCOUT**	2189.2	0	41	**S02**	1018.0	3036.8
12	**AV_{SS}**	2467.2	0	42	**S01**	852.0	3036.8
13	**AV_{DD}**	3333.6	0	43	**COM3**	676.0	3036.8
14	**OSCIN**	3340.0	184.4	44	**COM2**	342.0	3036.8
15	**TST2**	3340.0	360.4	45	**COM1**	166.0	3036.8
16	**TST1**	3340.0	526.4	46	**COM0**	0	3036.8
17	**TCL**	3340.0	702.4	47	**V_{EE1}**	0	2829.0
18	**V_{SS}**	3340.0	868.4	48	**C1**	0	2653.0
19	**BP43**	3340.0	1189.2	49	**C2**	0	2274.2
20	**BP42**	3340.0	1488.0	50	**V_{EE2}**	0	2098.2
21	**BP41**	3340.0	1664.0	51	**V_{REG}**	0	1932.2
22	**BP40**	3340.0	1962.8	52	**INT7**	0	1756.2
23	**S20**	3340.0	2188.0	53	**V_{DD}**	0	1590.2
24	**S19**	3340.0	2354.0	54	**INT2**	0	1424.2
25	**S18**	3340.0	2530.0	55	**IP53**	0	1248.2
26	**S17**	3340.0	2696.0	56	**IP52**	0	1034.2
27	**S16**	3340.0	2872.0	57	**IP51**	0	738.8
28	**S15**	3340.0	3038.0	58	**IP50**	0	524.8
29	**S14**	3070.0	3036.8	59	**BP03**	0	332.8
30	**S13**	2904.0	3036.8	60			

Table 8. Pad coordinates **M43C505F**

No.	Name	X Point	Y Point	No.	Name	X Point	Y Point
1	**BP02**	0	0	31	**S12**	**2788.4**	3036.8
2	**NST**	**194.0**	0	32	**S11**	**2622.4**	3036.8
3	**OD**	380.8	0	33	**S10**	**2446.4**	3036.8
4	**BP01**	556.8	0	34	**S09**	**2280.4**	3036.8
5	**BP00**	889.6	0	35	**S08**	**2104.4**	3036.8
6	**BP13**	1065.6	0	36	**S07**	**1938.4**	3036.8
7	**BP12**	1364.4	0	37	**S06**	**1762.4**	3036.8
8	**BP11**	1540.4	0	38	**S05**	**1596.4**	3036.8
9	**BP10**	1847.2	0	39	**S04**	**1420.4**	3036.8
10	**NRST**	2023.2	0	40	**S03**	**1254.4**	3036.8
11	**OSCOUT**	2189.2	0	41	**S02**	**1078.4**	3036.8
12	**AV_{SS}**	2467.2	0	42	**S01**	**912.4**	3036.8
13	**AV_{DD}**	3333.6	0	43	**COM3**	**736.4**	3036.8
14	**OSCIN**	3340.0	184.4	44	**COM2**	342.0	3036.8
15	**TST2**	3340.0	360.4	45	**COM1**	166.0	3036.8
16	**TST1**	3340.0	526.4	46	**COM0**	0	3036.8
17	**TCL**	3340.0	702.4	47	**V_{EE1}**	0	2829.0
18	**V_{SS}**	3340.0	868.4	48	**C1**	0	2653.0
19	**BP43**	3340.0	1189.2	49	**C2**	0	2274.2
20	**BP42**	3340.0	1488.0	50	**V_{EE2}**	0	2098.2
21	**BP41**	3340.0	1664.0	51	**V_{REG}**	0	1932.2
22	**BP40**	3340.0	1962.8	52	**INT7**	0	1756.2
23	**S20**	3340.0	2188.0	53	**V_{DD}**	0	1590.2
24	**S19**	3340.0	2354.0	54	**INT2**	0	1424.2
25	**S18**	3340.0	2530.0	55	**IP53**	0	1248.2
26	**S17**	3340.0	2696.0	56	**IP52**	0	1034.2
27	**S16**	3340.0	2872.0	57	**IP51**	0	738.8
28	**S15**	3340.0	3038.0	58	**IP50**	0	524.8
29	**S14**	**3130.4**	3036.8	59	**BP03**	0	332.8
30	**S13**	**2964.4**	3036.8	60			

Note: Pad coordinates printed as **bold numbers** identify modified pad positions compared to the e3505 and M43C505 design.

6 Appendix M45C535

The M45C535 is especially designed for low volumes, prototyping of M43C505 with fast turn-around times of less than one month.

The M45C535 is functionally and electrically compatible to the high volume standard M43C505.

The M45C535 (e3535) is available either as a packaged part (QFP64) or in bare die form for COB mounting. In the latter case, the substrate, i.e. the backside of the die, should be connected to $\mathbf{V_{SS}}$.

Die size: 3.84×4.41 mm = 16.9 mm^2 (incl. scribe)

Pad size: 100×100 µm

Thickness: 480 ± 25 µm (= 19 ± 1 mil)

6.1 Pad Layout

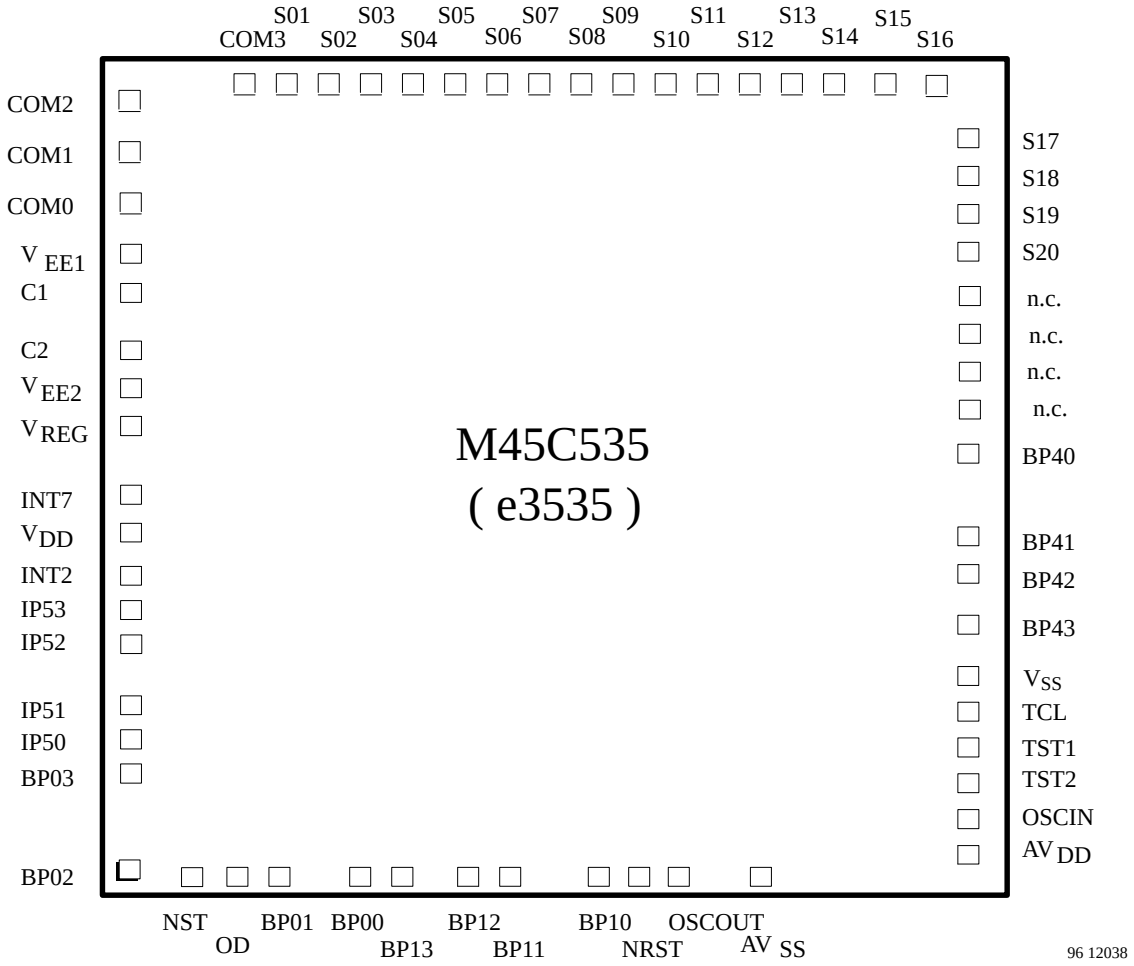


Figure 34. M45C535 pad layout

6.2 Pad Coordinates

Table 9. Pad coordinates **M45C535**

No.	Name	X Point	Y Point	No.	Name	X Point	Y Point
1	**BP02**	0	0	31	**S12**	2386.0	3852.0
2	**NST**	202.0	0	32	**S11**	2220.0	3852.0
3	**OD**	380.8	0	33	**S10**	2044.0	3852.0
4	**BP01**	556.8	0	34	**S09**	1878.0	3852.0
5	**BP00**	889.6	0	35	**S08**	1702.0	3852.0
6	**BP13**	1065.6	0	36	**S07**	1536.0	3852.0
7	**BP12**	1364.4	0	37	**S06**	1360.0	3852.0
8	**BP11**	1540.4	0	38	**S05**	1194.0	3852.0
9	**BP10**	1847.2	0	39	**S04**	1018.0	3852.0
10	**NRST**	2023.2	0	40	**S03**	852.0	3852.0
11	**OSCOUT**	2189.2	0	41	**S02**	676.0	3852.0
12	**AV_{SS}**	2467.2	0	42	**S01**	510.0	3852.0
13	**AV_{DD}**	3333.6	0	43	**COM3**	334.0	3852.0
14	**OSCIN**	3340.0	184.4	44	**COM2**	0	3852.0
15	**TST2**	3340.0	360.4	45	**COM1**	0	3644.0
16	**TST1**	3340.0	526.4	46	**COM0**	0	3468.0
17	**TCL**	3340.0	702.4	47	**V_{EE1}**	0	3302.0
18	**V_{SS}**	3340.0	868.4	48	**C1**	0	3126.0
19	**BP43**	3340.0	1242.8	49	**C2**	0	2648.0
20	**BP42**	3340.0	1520.4	50	**V_{EE2}**	0	2472.8
21	**BP41**	3340.0	1696.4	51	**V_{REG}**	0	2306.8
22	**BP40**	3340.0	1974.0	52	**INT7**	0	1756.2
23	**S20**	3340.0	3051.6	53	**V_{DD}**	0	1590.2
24	**S19**	3340.0	3227.6	54	**INT2**	0	1424.2
25	**S18**	3340.0	3393.6	55	**IP53**	0	1248.2
26	**S17**	3340.0	3569.6	56	**IP52**	0	1034.2
27	**S16**	3070.0	3852.0	57	**IP51**	0	738.8
28	**S15**	2904.0	3852.0	58	**IP50**	0	524.8
29	**S14**	2728.0	3852.0	59	**BP03**	0	332.8
30	**S13**	2562.0	3852.0	60			

7 Ordering Information

Please insert ROM CRC and select the option setting from the list below.

BP40
- ❑ CMOS
- ❑ Open drain
- ❑ Pull-up
- ❑ No pull-up

BP41
- ❑ CMOS
- ❑ Open drain
- ❑ Pull-up
- ❑ No pull-up

BP42
- ❑ CMOS
- ❑ Open drain
- ❑ Pull-up
- ❑ No pull-up

BP43
- ❑ CMOS
- ❑ Open drain
- ❑ Pull-up
- ❑ No pull-up

IP50
- ❑ Pull-up
- ❑ No pull-up

IP51
- ❑ Pull-up
- ❑ No pull-up

IP52
- ❑ Pull-up
- ❑ No pull-up

IP53
- ❑ Pull-up
- ❑ No pull-up

INT2
- ❑ Pull-up
- ❑ No pull-up
- ❑ Pull-down
- ❑ Active pull-up/pull-down

INT7
- ❑ Pull-up
- ❑ No pull-up
- ❑ Pull-down
- ❑ Active pull-up/pull-down

OSCIN
- ❑ Internal CAP
- ❑ No CAP

OSCOUT
- ❑ Internal CAP
- ❑ No CAP

Buzzer
- ❑ 2.048 kHz (default)
- ❑ 4.096 kHz

Package
- ❑ DIT
- ❑ 64 pin QFP

ROM
- ❑ File: _____.HEX
- ❑ CRC type: 16-bit/Short
- ❑ CRC: _____ hex

Selftest
- ❑ Stimulus at Port 0: _____

Approval : Date: __.__.__ Signature: _____

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