PTH12040W — 12-V Input

50-A, 8 –14-V Input, Non-Isolated Wide-Output Adjust Power Module

SLTS237 DECEMBER 2004

NOMINAL SIZE = 2.05 in x 1.05 in (52 mm x 26,7 mm)

Features

- 50 A Output Current
- 8 to 14-V Input Voltage
- Wide-Output Voltage Adjust (0.8 V to 5.5 V)
- Efficiencies up to 96 %
- On/Off Inhibit
- Differential Output Sense
- Output Over-Current Protection (Non-Latching, Auto-Reset)
- Over-Temperature Protection
- Auto-Track™ Sequencing
- Start Up Into Output Prebias
- Margin Up/Down Controls
- Operating Temp: –40 to +85 °C
- Multi-Phase Switch-Mode Topology
- Programmable Under-Voltage Lockout (UVLO)
- Safety Agency Approvals: UL/cUL 60950, EN60950 VDE (Pending)

Description

The PTH12040W is a high-performance 50-A rated, non-isolated, power module, which uses the latest multi-phase switched-mode topology. This provides a small, ready-to-use module, that can power the most densly populated multi-processor systems.

Operating from an input voltage range of 8 to 14 V, the PTH12040W requires a single resistor to set the output voltage to any value over the range, 0.8 V to 5.5 V. The wide input voltage range makes the PTH12040W particularly suitable for advanced computing and server applications that utilize a loosely regulated 12-V intermediate distribution bus.

The modules incorporate a comprehensive list of features. They include on/off inhibit and margin up/down controls. A differential remote output voltage sense ensures tight load regulation, and an output overcurrent and overtemperature shutdown protect against most load faults. The programmable under-voltage lockout allows the turn-on and turn-off voltage thresholds to be customized.

The PTH12040W incorporates Auto-Track™. Auto-Track is a popular feature of the PTH family that allows the outputs of multiple modules to track a common voltage during power up and power down transitions. This greatly simplifies power up and power down supply-voltage sequencing in a power supply system.

The modules use double-sided surface mount construction to provide a low profile and compact footprint. Package options inlude both through-hole and surface mount configurations.

Pin Configuration

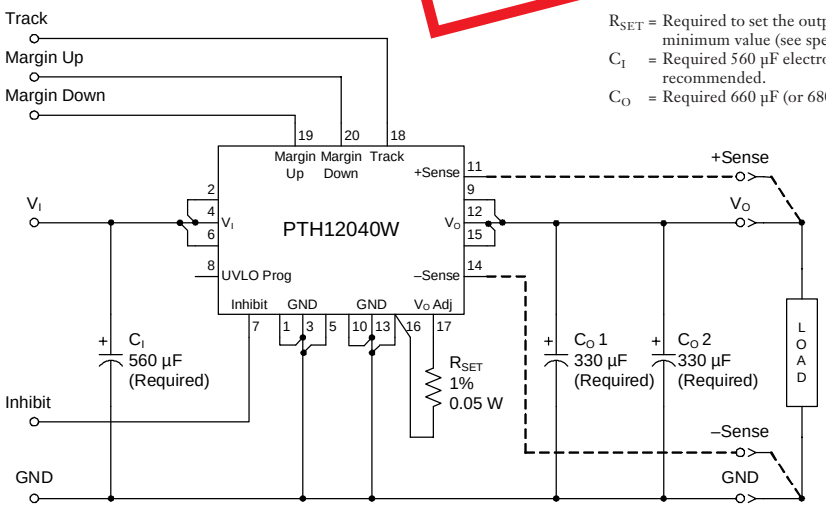
Pin	Function
1	GND
2	V_I
3	GND
4	V_I
5	GND
6	V_I
7	Inhibit *
8	UVLO Prog
9	V_O
10	GND
11	+Sense
12	V_O
13	GND
14	–Sense
15	V_O
16	GND
17	V_O Adjust
18	Track
19	Margin Up *
20	Margin Down *

* *Denotes negative logic:*
Open = Normal operation
Ground = Function active

Standard Application

Auto-Track™ Sequencing

R_{SET} = Required to set the output voltage higher than the minimum value (see spec. table for values).
C_I = Required 560 µF electrolytic capacitor. 1,000 µF recommended.
C_O = Required 660 µF (or 680 µF) electrolytic capacitor.



Ordering Information

Output Voltage (PTH12040❒xx)

Code	Voltage
W	0.8 V – 5.5 V (Adjust)

Package Options (PTH12040x❒❒) (1)

Code	Description	Pkg Ref. (2)
AH	Horiz. T/H	(EVF)
AS	SMD, Standard (3)	(EVG)

Notes: *(1) Add "T" to end of part number for tape and reel on SMD packages only.*
(2) Reference the applicable package reference drawing for the dimensions and PC board layout
(3) "Standard" option specifies 63/37, Sn/Pb pin solder material.

Pin Descriptions

GND: This is the common ground connection for the V_I and *Vout* power connections. It is also the 0 VDC reference for the control inputs.

V_I: The positive input voltage power node to the module, which is referenced to common *GND*.

V_O: The regulated positive power output with respect to the *GND* node.

Inhibit: The Inhibit pin is an open-collector/drain negative logic input that is referenced to *GND*. Applying a low-level ground signal to this input disables the module's output and turns off the output voltage. When the *Inhibit* control is active, the input current drawn by the regulator is significantly reduced. If the *Inhibit* pin is left open-circuit, the module will produce an output whenever a valid input source is applied.

V_O Adjust: A 1%, 0.05-W resistor must be connected between this pin and GND to set the output voltage higher than the minimum value. The set-point range for the output voltage is from 0.8 V to 5.5 V. The resistor required for a given output voltage may be calculated from the following formula. If left open circuit, the module output will default to its lowest output voltage value. For further information on the adjustment and/or trimming of the output voltage, consult the related Application Information.

$$R_{SET} = 10\text{ k} \cdot \frac{0.8\text{ V}}{V_O - 0.8\text{ V}} - 1.696\text{ k}$$

The specification table gives the preferred resistor values for a number of standard output voltages.

+Sense: The sense inputs allow the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy *+Sense* should be connected to V_O. If it is left open, a low-value internal resistor ensures that the output remains in regulation.

–Sense: For optimal voltage accuracy *–Sense* should be connected to the ground return at the load. If it is left open, a low-value internal resistor ensures that the output remains in regulation.

UVLO Prog: Connecting a resistor from this pin to signal ground allows the 'on' threshold of the input under-voltage lockout (UVLO) to be adjusted higher than the default value. The hysterisis can also be independenly reduced by connecting a second resistor from this pin to V_I. For further information consult the Application Information.

Track: This is an analog control input that allows the output voltage to follow another voltage during power-up and power-down sequences. The pin is active from 0 V, up to the nominal set-point voltage. Within this range the module's output will follow the voltage at the *Track* pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its nominal output voltage. If unused this input should be connected to V_I for a faster power-up. For further information consult the related Application Information.

Margin Down: When this input is asserted to *GND*, the output voltage is decreased by 5% from the nominal. The input requires an open-collector (open-drain) interface. It is not TTL compatible. A lower percent change can be accommodated with a series resistor. For further information, consult the Application Information.

Margin Up: When this input is asserted to *GND*, the output voltage is increased by 5%. The input requires an open-collector (open-drain) interface. It is not TTL compatible. The percent change can be reduced with a series resistor. For further information, consult the related Application Information.

Environmental & Absolute Maximum Ratings (Voltages are with respect to GND)

Characteristics	Symbols	Conditions	Min	Typ	Max	Units
Signal Input Voltages		Track control (pin 18)	–0.3	—	V_I + 0.3	V
Operating Temperature Range	T_A	Over V_I Range	–40	—	85	°C
Solder Reflow Temperature	T_{reflow}	Surface temperature of module body or pins			235 (i)	°C
Storage Temperature	T_S	—	–40	—	125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ Sine, mounted	—	TBD (ii)	—	G's
Mechanical Vibration		Mil-STD-883D, Method 2007.2 20-2000 Hz	—	TBD (ii)	—	G's
Weight	—		—	17	—	grams
Flammability	—	Meets UL 94V-O				

Notes: *(i) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.*
(ii) Qualification limits.

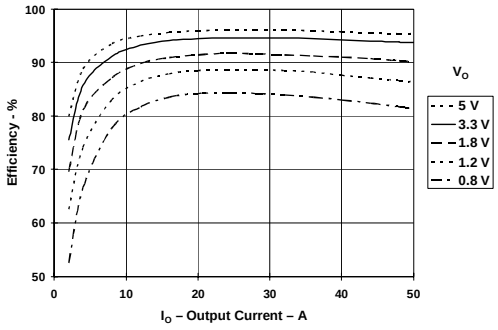
Specifications (Unless otherwise stated, T_A =25 °C, V_I =12 V, V_O =3.3 V, C_I =1,000 µF, C_O =660 µF, and I_O =I_O max)

			PTH12040W			
Characteristics	Symbols	Conditions	Min	Typ	Max	Units
Output Current	I_O	60 °C, 200 LFM airflow	0	—	50 (1)	A
Input Voltage Range	V_I	Over I_O range	8 (2)	—	14	V
Set-Point Voltage Tolerance	V_O tol		—	—	±2 (2)	%V_O
Temperature Variation	ΔReg_{temp}	–40 °C <T_A < +85 °C	—	±0.5	—	%V_O
Line Regulation	ΔReg_{line}	Over V_I range	—	±5	—	mV
Load Regulation	ΔReg_{load}	Over I_o range	—	±5	—	mV
Total Output Variation	ΔReg_{tot}	Includes set-point, line, load, –40 °C ≤ T_A ≤ +85 °C	—	—	±3 (2)	%V_O
Output Adjust Range	ΔV adj		0.8	—	5.5 (3)	V
Efficiency	η	I_O =35 A R_{SET} = 205 Ω V_O = 5.0 V	—	96	—	%
		R_{SET} = 1.5 kΩ V_O = 3.3 V	—	95	—	
		R_{SET} = 3.01 kΩ V_O = 2.5 V	—	93	—	
		R_{SET} = 4.99 kΩ V_O = 2.0 V	—	92	—	
		R_{SET} = 6.34 kΩ V_O = 1.8 V	—	91	—	
		R_{SET} = 9.76 kΩ V_O = 1.5 V	—	90	—	
		R_{SET} = 18.2 kΩ V_O = 1.2 V	—	88	—	
		R_{SET} = 38.3 kΩ V_O = 1.0 V	—	86	—	
		R_{SET} = open cct. V_O = 0.8 V	—	82	—	
V_o Ripple (pk-pk)	V_R	20 MHz bandwidth All voltages	—	15	—	mVpp
Over-Current Threshold	I_O trip	Reset, followed by auto-recovery	—	95	—	A
Transient Response		1 A/µs load step, 50 to 100% $I_O$max, C_O =660 µF				
	t_{tr}	Recovery Time	—	70	—	µSec
	ΔV_{tr}	V_O over/undershoot	—	150	—	mV
Margin Up Down Adjust	V_O adj	With V_O Adjust control	—	± 5	—	%
Margin Input Current	I_{IL} margin	Pin to GND	—	– 8 (4)	—	µA
Track Input Current (pin 18)	I_{IL} track	Pin to GND	—	—	–0.13 (4)	mA
Track Slew Rate Capability	dV_{track}/dt	$\lvert V_{TRACK} - V_O \rvert \le 50$ mV and $V_{TRACK} < V_O$(nom)	—	—	1	V/ms
Under-Voltage Lockout	UVLO	Pin 8 open on-threshold	—	7.5 (5)	—	V
		hysterisis	—	1 (5)	—	
Inhibit Control (pin7)		Referenced to GND				
Input High Voltage	V_{IH}		2.5	—	Open (6)	V
Input Low Voltage	V_{IL}		–0.2	—	0.5	
Input Low Current	I_{IL} inhibit	Pin to GND	—	–0.5	—	mA
Input Standby Current	I_I inh	Inhibit (pin 7) to GND	—	35	—	mA
Switching Frequency	f_S	Over V_I and I_O ranges	0.9	1.05	1.2	MHz
External Input Capacitance	C_I		560 (7)	1,000	—	µF
External Output Capacitance	C_O	capacitance value non-ceramic	660 (8)	—	14,000 (9)	µF
		ceramic	—	—	400	µF
		Equiv. series resistance (non-ceramic)	2 (10)	—	—	mΩ
Reliability	MTBF	Per Bellcore TR-332 50 % stress, T_A =40 °C, ground benign	2.5	—	—	10^6 Hrs

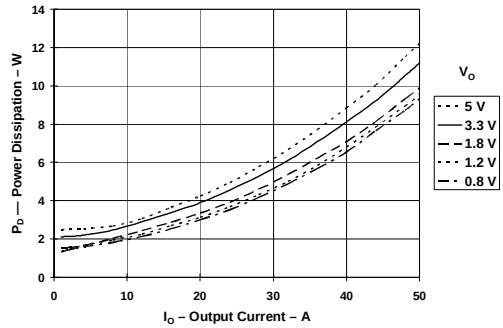
Notes: *(1) See SOA curves or consult factory for appropriate derating.*
(2) The set-point voltage tolerance is affected by the tolerance of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with 100 ppm/°C or better temperature stability.
(3) When the set-point voltage is adjusted higher than 3.6 V, a 10-V minimum input voltage is recommended.
(4) A small low-leakage (<100 nA) MOSFET is recommended to control this pin. The open-circuit voltage is less than 1 Vdc.
(5) These are the default voltages. The y may be adjusted using the 'UVLO Prog' control input. Consult the Application Information for further guidance.
(6) This control pin has an internal pull-up to 5 V nominal. If it is left open-circuit the module will operate when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended for control. For further information, consult the related application note.
(7) A minimum capacitance of 560-µF is required at the input for proper operation. For best results, 1,000 µF is recommended. The capacitance must be rated for a minimum of 300 mArms of ripple current.
(8) A minimum value of output capacitance is required for proper operation. Adding additional capacitance at the load will further improve transient response.
(9) This is the calculated maximum. The minimum ESR requirement will often result in a lower value. Consult the Application Information for further guidance.
(10) This is the typcial ESR for all the electrolytic (non-ceramic) output capacitance. Use 4 mΩ as the minimum when using max-ESR values to calculate.

Characteristic Data; V_I =12 V *(See Note A)*

Efficiency vs Load Current

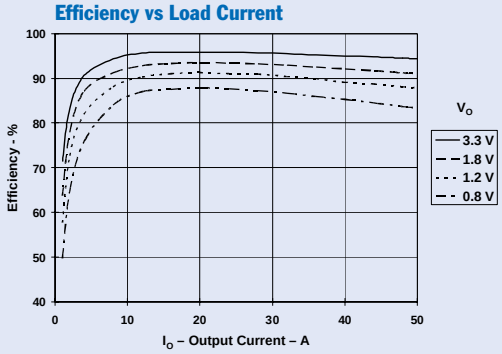


Power Dissipation vs Load Current

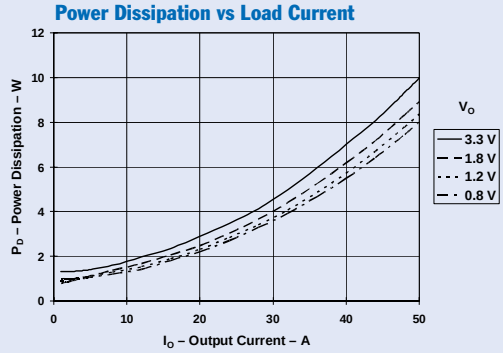


Characteristic Data; V_I =8 V *(See Note A)*

Efficiency vs Load Current

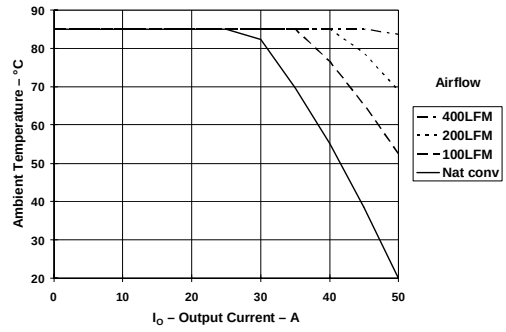


Power Dissipation vs Load Current

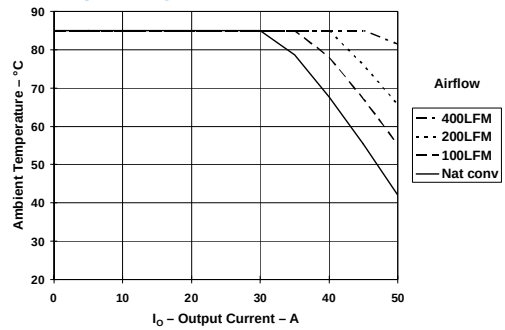


Safe Operating Area; V_I =12 V *(See Note B)*

Output Voltage =3.3 V



Output Voltage =1.2 V



Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.*
Note B: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.*

Capacitor Recommendations for the PTH12040W Power Module

The PTH12040W is a state-of-the-art multi-phase power converter topology that uses three parallel switching and filter inductor paths between the common input and output filter capacitors. The three paths share the load current, operate at the same frequency, and are evenly displaced in phase.

With multiple switching paths the transient output current capability is significantly increased. This reduces the amount of external output capacitance required to support a load transient. As a further benefit, the ripple current, as seen by the input and output capacitors, is reduced in magnitude and effectively tripled in frequency.

Input Capacitor

The improved transient response of a multi-phase converter places a bigger burden on the transient capability of the input source. The size and value of the input capacitor is therefore determined by this converter's transient performance capability. The minimum amount of input capacitance required is 560 µF, [3] with an RMS ripple current rating of 300 mA. This minimum value assumes that the converter is supplied with a responsive, low-inductance input source. This source should have ample capacitive decoupling and be distributed to the converter via PCB power and ground planes. For high-performance applications, or wherever the transient performance of the input source is limited, 1,000 µF of input capacitance is recommended.

Ripple current, less than 100 mΩ of equivalent series resistance (ESR), and temperature are the main considerations when selecting input capacitors. The ripple current reflected from the input of the PTH12040W module is moderate to low. Therefore any good quality, computer-grade electrolytic capacitor, of either value suggested, will have adequate ripple current rating.

Regular tantalum capacitors are not recommended for the input bus. These capacitors require a recommended minimum voltage rating of 2 × (max. DC voltage + AC ripple). This is standard practice to ensure reliability. No tantalum capacitors were found with a sufficient voltage rating to meet this requirement. [1] When the operating temperature is below 0 °C, the ESR of aluminum electrolytic capacitors increases. For these applications Os-Con, poly-aluminum, and polymer-tantalum types should be considered. Adding one or two ceramic capacitors to the input will reduce high-frequency reflected ripple current. [4]

Output Capacitors

The PTH12040W requires a minimum output capacitance of 680 µF (or 2 × 330 µF), with an ESR of 15 mΩ to 40 mΩ. This is necessary for the stable operation of the regulator. Additional capacitance can be added to improve the module's performance to load transients. High quality, computer-grade electrolytic capacitors are recommended. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0 °C. For operation below 0 °C, tantalum, ceramic, or Os-Con type capacitors will be necessary.

When using a combination of one or more non-ceramic capacitors, the calculated equivalent ESR should be no lower than 2 mΩ (4 mΩ when calculating using the manufacturer's maximum ESR values). A list of preferred low-ESR type capacitors are identified in Table 1-1.

Ceramic Capacitors

Above 150 kHz the performance of aluminum electrolytic capacitors is less effective. Multilayer ceramic capacitors have very low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output. When used on the output their combined ESR is not critical as long as the total value of ceramic capacitors, with values between 10µf and 100µF, does not exceed 400 µF. Also, to prevent the formation of local resonances, do not place more than five identical ceramic capacitors in parallel with values of 10 µF or greater.

Tantalum Capacitors

Tantalum type capacitors can only be used on the output bus, and are recommended for applications where the ambient operating temperature can be less than 0 °C. The AVX TPS, Sprague 593D/594/595 and Kemet T495/T510 capacitor series are suggested over many other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution many general purpose tantalum capacitors have considerably higher ESR, reduced power dissipation and lower ripple current capability. These capacitors are also less reliable due to their reduced power dissipation and surge current ratings. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

When specifying Os-con and polymer tantalum capacitors for the output, the minimum ESR limit will be encountered well before the maximum capacitance value is reached.

Capacitor Table

Table 1-1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100 kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

Designing for Very Fast Load Transients

The transient response of the DC/DC converter has been characterized using a load transient with a di/dt of 1 A/µs. The typical voltage deviation for this load transient is given in the data sheet specification table using the mnimum required value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any DC/DC converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases special attention must be paid to the type, value and ESR of the capacitors selected.

Table 1-1: Input/Output Capacitors

Capacitor Vendor, Type Series (Style)	Capacitor Characteristics					Quantity		
	Working Voltage	Value (µF)	Max. ESR at 100 kHz	Max Ripple Current at 85 °C (Irms)	Physical Size(mm)	Input Bus	Output Bus	Vendor Part Number
Panasonic FC (Radial) FK (SMD)	25 V 25 V 16 V 35 V	1000 560 680 1000	0.043 Ω 0.065 Ω 0.080 Ω 0.060 Ω	>1690 mA 1205 mA >850 mA 1100 mA	16 × 15 12.5×15 10 × 10.2 12.5×13.5	1 1 1 1	1 2 1 1	EEUFC1E102S EEUFC1E561S EEVFK1C681P EEVFK1V102Q
United Chemi-Con MVZ(SMD) LXZ, Aluminum (Radial) PS, Poly-Aluminum(Radial) PXA, Poly-Aluminum (SMD)	16 V 16 V 25 V 16 V 16 V	470 470 680 330 330	0.090 Ω 0.090 Ω 0.068 Ω 0.014 Ω 0.014 Ω	670 mA 760 mA 1050 mA 5060 mA 5050 m A	10×10 10×12.5 10×16 10×12.5 10×12.2	2 2 1 2 2	2 2 1 ≤4 ≤4	MVZ25VC471MJ10TP LXZ16VB471M10X12LL LXZ16VB681M10X16LL 16PS330MJ12 PXA16VC331MJ12TP
Nichicon, Aluminum HD (Radial) PM (Radial)	25 V 25 V 35 V	560 680 560	0.060 Ω 0.038 Ω 0.048 Ω	1060 mA 1430 mA 1360 mA	12.5×15 10×16 16×15	1 1 1	2 1 2	UPM1E561MHH6 UHD1C681MHR UPM1V561MHH6
Panasonic, Poly-Aluminum: WA (SMD)	16 V	330	0.022 Ω	4100 mA	10×10.2	2	≤5	EEFWA1C331P
Sanyo TPE, Poscap (SMD) SP, Os-Con (Radial) SVP, Os-Con (SMD)	10 V 16 V 16 V	330 270 330	0.025 Ω 0.018 Ω 0.016 Ω	3000 mA >3500 mA 4700 mA	7.3L ×5.7W 10×10.5 11×12	N/R [1] 3 [3] 2	≤5 ≤4 ≤4	10TPE330M 16SP270M 16SVP330M
AVX, Tantalum, Series III TPS (SMD)	10 V 10 V	470 330	0.045 Ω 0.045 Ω	>1723 mA >1723 mA	7.3L ×5.7W ×4.1H	N/R [1] N/R [1]	≤5 [2] ≤5 [2]	TPSE477M010R0045 **(V_o≤5.1V)** TPSE337M010R0045 **(V_o≤5.1V)**
Kemet, Poly-Tantalum T520 (SMD) T530 (SMD)	10 V 10 V 6.3 V	330 330 470	0.040 Ω 0.015 Ω 0.012 Ω	1800 mA >3800 mA 4200 mA	4.3W ×7.3L ×4.0H	N/R [1] N/R [1] N/R [1]	2 ≤4 ≤3 [2]	T520X337M010AS T530X337M010AS T530X477M006AS **(V_o≤5.1V)**
Vishay-Sprague 595D, Tantalum (SMD) 94SA, Os-con (Radial)	10 V 16 V	470 1,000	0.100 Ω 0.015 Ω	1440 mA 9740 mA	7.2L×6W ×4.1H 16×25	N/R [1] 1	2 [2] ≤4	595D477X0010R2T **(V_o≤5.1V** 94SA108X0016HBP
Kemet, Ceramic X5R (SMD)	16 V 6.3 V	10 47	0.002 Ω 0.002 Ω	—	3225	1 [4] N/R [1]	≤8 ≤8	C1210C106M4PAC C1210C476K9PAC
Murata, Ceramic X5R (SMD)	6.3 V 6.3 V 16 V 16 V 16 V	100 47 47 22 10	0.002 Ω	—	3225	N/R [1] N/R [1] 1 [4] 1 [4] 1 [4]	≤4 ≤8 ≤8 ≤8 ≤8	GRM32ER60J107M GRM32ER60J476M GRM32ER61C476K GRM32ER61C226K GRM32DR61C106K
TDK, Ceramic X5R (SMD)	6.3 V 6.3 V 16 V 16 V	100 47 22 10	—	—	3225	N/R [1] N/R [1] 1 [4] 1 [4]	≤4 ≤8 ≤8 ≤8	C3225X5R0J107MT C3225X5R0J476MT C3225X5R1C226MT C3225X5R1C106MT

[1] N/R –Not recommended. The voltage rating does not meet the minimum operating limits.
[2] The voltage rating of this capacitor only allows it to be used for output voltages that are equal to or less than 5.1 V.
[3] Total capacitance of 540 µF is acceptable based on the combined ripple current rating.
[4] Small ceramic capacitors may used to complement electrolytic types at the input to further reduce high-frequency ripple current.

Adjusting the Output Voltage of the PTH12040W Wide-Output Adjust Power Module

The *V_O Adjust* control (pin 17) sets the output voltage of the PTH12040W product. The adjustment range is from 0.8 V to 5.5 V. The adjustment method requires the addition of a single external resistor, R_{SET}, that must be connected directly between the *V_o Adjust* and *GND* pins [1]. Table 2-1 gives the preferred value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides. Figure 2-1 shows the placement of the required resistor.

Table 2-1; Standard Values of R_{SET} for Common Output Voltages

	PTH12040W	
V_O (Req'd)	**R_{SET}**	**V_O (Actual)**
5 V	205 Ω	5.008 V
3.3 V	1.5 kΩ	3.303 V
2.5 V	3.01 kΩ	2.500 V
2 V	4.99 kΩ	1.997 V
1.8 V	6.34 kΩ	1.796 V
1.5 V	9.76 kΩ	1.498 V
1.2 V	18.2 kΩ	1.202 V
1.0 V	38.3 kΩ	1.000 V
0.8 V	Open	0.800 V

For other output voltages the value of the required resistor can either be calculated, or simply selected from the range of values given in Table 2-2. The following formula can be used to calculate the adjust resistor value.

$$R_{SET} = 10\,k\Omega \cdot \frac{0.8\,V}{V_o - 0.8} - 1.696\ k\Omega$$

Notes:

1. A 0.05-W rated resistor may be used. The tolerance should be 1%, and the temperature stability, 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pin 17 and nearest GND pin (pin 16) using dedicated PCB traces.
2. Never connect capacitors from *V_o Adjust* to either *GND* or *V_O*. Any capacitance added to the *V_o Adjust* pin will affect the stability of the regulator.

Figure 2-1; V_o Adjust Resistor Placement

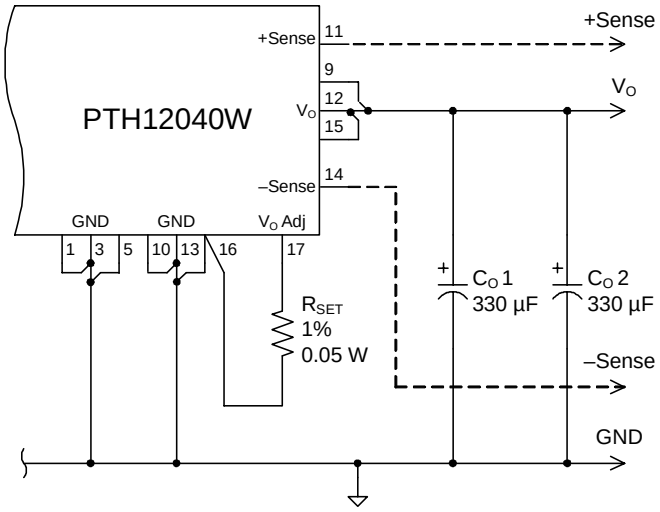


Table 2-2; Output Voltage Set-Point Resistor Values

V_O	R_{SET}	V_O	R_{SET}	V_O	R_{SET}
0.800	Open	1.60	8.3 kΩ	3.10	1.78 kΩ
0.825	318.0 kΩ	1.65	7.72 kΩ	3.15	1.71 kΩ
0.850	158.0 kΩ	1.70	7.19 kΩ	3.20	1.64 kΩ
0.875	105.0 kΩ	1.75	6.73 Ω	3.25	1.57 kΩ
0.900	78.31 kΩ	1.80	6.3 Ω	3.30	1.5 kΩ
0.925	62.3 kΩ	1.85	5.92 kΩ	3.35	1.44 kΩ
0.950	51.6 kΩ	1.90	5.58 kΩ	3.40	1.38 kΩ
0.975	44.0 kΩ	1.95	5.26 kΩ	3.50	1.27 kΩ
1.000	38.3 kΩ	2.00	4.97 kΩ	3.60	1.16 kΩ
1.025	33.9 kΩ	2.05	4.7 kΩ	3.70	1.06 kΩ
1.050	30.3 kΩ	2.10	4.46 kΩ	3.80	971 Ω
1.075	27.4 kΩ	2.15	4.23 kΩ	3.90	885 Ω
1.100	25.0 kΩ	2.20	4.02 kΩ	4.00	804 Ω
1.125	22.9 kΩ	2.25	3.82 kΩ	4.10	728 Ω
1.150	21.2 kΩ	2.30	3.64 kΩ	4.20	657 Ω
1.175	19.6 kΩ	2.35	3.47 kΩ	4.30	590 Ω
1.200	18.3 kΩ	2.40	3.3 kΩ	4.40	526 Ω
1.225	17.1 kΩ	2.45	3.15 kΩ	4.50	466 Ω
1.250	16.1 kΩ	2.50	3.01 kΩ	4.60	409 Ω
1.275	15.1 kΩ	2.55	2.88 kΩ	4.70	355 Ω
1.300	14.3 kΩ	2.60	2.75 kΩ	4.80	304 Ω
1.325	13.5 kΩ	2.65	2.63 kΩ	4.90	255 Ω
1.350	12.8 kΩ	2.70	2.51 kΩ	5.00	209 Ω
1.375	12.2 kΩ	2.75	2.41 kΩ	5.10	164 Ω
1.400	11.6 kΩ	2.80	2.3 kΩ	5.20	122 Ω
1.425	11.1 kΩ	2.85	2.21 kΩ	5.30	82 Ω
1.450	10.6 kΩ	2.90	2.11 kΩ	5.40	43 Ω
1.475	10.2 kΩ	2.95	2.02 kΩ	5.50	0 Ω
1.50	9.73 kΩ	3.00	1.94 kΩ		
1.55	8.97 kΩ	3.05	1.86 kΩ		

Adjusting the Under-Voltage Lockout (UVLO) of the PTH12040W Power Modules

The PTH12040W power modules incorporate an input under-voltage lockout (UVLO). The UVLO feature prevents the operation of the module until there is sufficient input voltage to produce a valid output voltage. This enables the module to provide a clean, monotonic powerup for the load circuit, and also limits the magnitude of current drawn from the regulator's input source during the power-up sequence.

The UVLO characteristic is defined by the on-threshold (V_{THD}) and hysterisis (V_{HYS}) voltages. Below the 'on' threshold, the *Inhibit* control is overriden, and the module will not produce an output. The hysterisis voltage is the difference between the 'on' and 'off' threshold voltages. It ensures a clean power-up, even when the input voltage is rising slowly. The hysterisis prevents start-up oscillations, which can occur if the input voltage droops slightly when the module begins drawing current from the input source.

UVLO Adjustment

The UVLO feature of the PTH12040W module allows for limited adjustment of both the on-threshold and hysterisis voltages. The adjustment is made via the '*UVLO Prog*' control pin. When the *UVLO Prog* pin is left open circuit the on-threshold and hysterisis voltages are internally set to their default values. The 'on' threshold has a nominal voltage of 7.5 V, and the hysterisis 1 V. This ensures that the module will produce a regulated output when the minimum input voltage is applied (see specifications). The combination correlates to an 'off' threshold of approximately 6.5 V. The adjustments are limited. The on-threshold can only be adjusted higher, and the hysterisis voltage can only be reduced in magnitude.

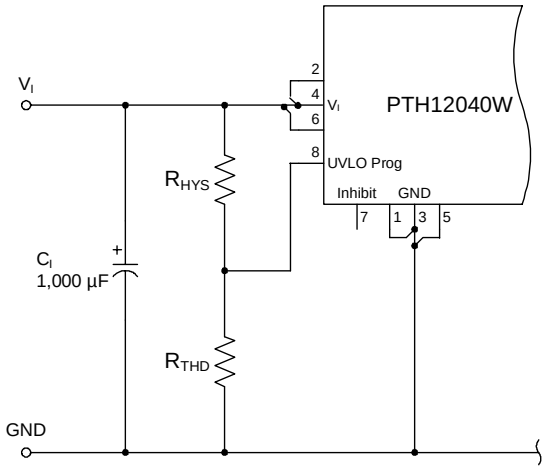
The 'on' threshold might need to be raised if the module is powered from a tightly regulated 12-V bus. This would prevent it from operating if the input bus failed to completely rise to its specified regulation voltage. The hysterisis shouldn't be changed unless absolutely necessary. A generous amount of hysterisis ensures that the module exhibits a clean startup. Therefore adjustment of the hysterisis should only be considered if there is a system requirement to specifically set the off-threshold voltage (in addition to the on-threshold). Depending on the load regulation of the input source, the hysterisis should not be adjusted below 0.5 V without careful consideration.

Adjustment Method

The resistors R_{THD}, and R_{HYS} (see Figure 2-2), provide the adjustment of the on-threshold and hysterisis voltages. R_{THD} connects between the *UVLO Prog* control pin and *GND*, and R_{HYS} is connected between the *UVLO Prog* and V_I. R_{THD} alone can be used to adjust the on-threshold voltage higher. However, to adjust the hysterisis to a lower value requires both the R_{HYS} and R_{THD} resistors to be placed in the circuit.

The recommended adjustment method requires that any change to the hysterisis be determined first. If the hysterisis is changed, then a value for R_{THD} must also be calculated. This is irrespective of whether a change is required to the value of V_{THD}. If there is no change to V_{HYS}, then a resistor should not be placed in the R_{HYS} location. R_{HYS} should then be assigned an infinite value for calculating the value of R_{THD}.

Figure 2–2; UVLO Program Resistor Placement



Hysterisis Adjust

The hysterisis voltage, V_{HYS}, is the difference between the 'on' and 'off' threshold values. The default value is 1 V and it can only be adjusted to a lower value.

! *Caution should be used when changing the hysterisis voltage to a lower value, as it could induce start-up oscillations.*

Any change in the hysterisis voltage will require both R_{HYS} and R_{THD} resistors be in place. Adding R_{HYS} alone will not have the desired effect. The value for R_{HYS} must first be calculated using equation, Eq. 2-1. The value identified for R_{HYS} must then be used to determine a value for R_{THD}, using equation, Eq. 2–2.

$$R_{HYS} = \frac{26.1 \cdot V_{HYS}}{0.365 \cdot (1 - V_{HYS})} \quad k\Omega \qquad \text{Eq. 2–1}$$

Threshold Adjust

The following equation, Eq. 2-2, determines the value of R_{THD} required to adjust V_{THD} to a new value. The default value is 7.5 V, and it may only be adjusted to a higher value. If the hysterisis value has been adjusted, then a value for R_{THD} must also be calculated. (This is irrespective of whether V_{THD} is being adjusted.) If there has been no adjustment for the hystersis voltage, the term '$1/R_{HYS}$' in equation Eq. 2-2, may be assigned the value, '0'.

Eq. 2–2:

$$R_{THD} = \frac{39.2\ k\Omega}{39.2\ [(1/R_{HYS} + 0.014)(V_{THD}/2.5 - 1) - 0.0027] - 1}$$

Calculated Values

Table 2-3 (below) shows a matrix of standard resistor values for R_{HYS} and R_{THD}, for different options of the on-threshold (V_{THD}) and hysterisis (V_{HYS}) voltages. For most applications, only the on-threshold voltage should need to be adjusted. In this case select only a value for R_{THD} from far right-hand column.

The hysterisis should only be adjusted if there is a specific requirement to independently adjust the off-threshold, separately from the on-threshold voltage. In this case, a value for both R_{HYS} and R_{THD} must be selected from the table. This is irrespective of whether the on-threshold voltage is being adjusted.

Table 2-3; Calculated Values of R_{HYS} and R_{THD}, for Various Values of V_{HYS} and V_{THD}

	V_{HYS}	0.5 V	0.6 V	0.7 V	0.8 V	0.9 V	1 V (default)
V_{THD}	R_{HYS}	71.5 kΩ	107 kΩ	165 kΩ	287 kΩ	649 kΩ	N/A
8.0 V		30.1 kΩ	43.2 kΩ	63.4 kΩ	97.6 kΩ	169 kΩ	402 kΩ
8.5 V		25.5 kΩ	36.5 kΩ	51.1 kΩ	73.2 kΩ	110 kΩ	187 kΩ
9.0 V		23.2 kΩ	30.9 kΩ	42.2 kΩ	57.6 kΩ	82.5 kΩ	124 kΩ
9.5 V		20 kΩ	27.4 kΩ	36.5 kΩ	48.7 kΩ	64.9 kΩ	90.9 kΩ
10 V	R_{THD}	18.2 kΩ	24.3 kΩ	31.6 kΩ	41.2 kΩ	54.9 kΩ	73.2 kΩ
10.5 V		16.2 kΩ	21.5 kΩ	28 kΩ	36.5 kΩ	46.4 kΩ	60.4 kΩ
11 V		15 kΩ	19.6 kΩ	25.5 kΩ	32.4 kΩ	41.2 kΩ	52.3 kΩ
11.5 V		14 kΩ	18.2 kΩ	23.2 kΩ	28 kΩ	36.5 kΩ	45.3 kΩ
12 V		12.7 kΩ	16.5 kΩ	21 kΩ	26.1 kΩ	32.4 kΩ	40.2 kΩ

Features of the PTH Family of Non-Isolated Wide Output Adjust Power Modules

POLA™ Compatibility

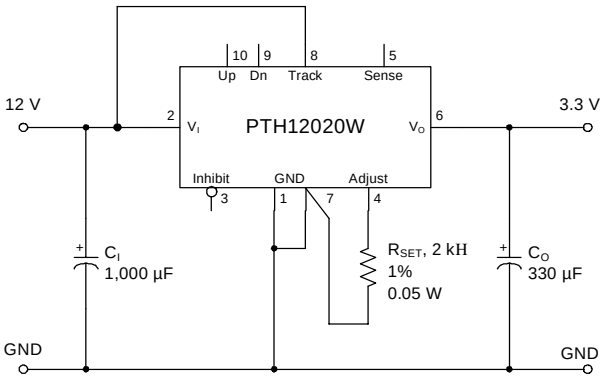
The PTH/PTV family of non-isolated, wide-output adjustable power modules from Texas Instruments are optimized for applications that require a flexible, high performance module that is small in size. Each of these products are POLA™ compatible. POLA-compatible products are produced by a number of manufacturers, and offer customers advanced, non-isolated modules with the same footprint and form factor. POLA parts are also assured to be interoperable, thereby providing customers with true second-source availability.

All POLA products include Auto-Track™. This feature was specifically designed to simplify the task of sequencing the supply voltages in a power system. This and other features are described in the following sections.

Soft-Start Power Up

The Auto-Track feature allows the power-up of multiple PTH modules to be directly controlled from the *Track* pin. However in a stand-alone configuration, or when the Auto-Track feature is not being used, the *Track* pin should be directly connected to the input voltage, V_I (see Figure 3-1).

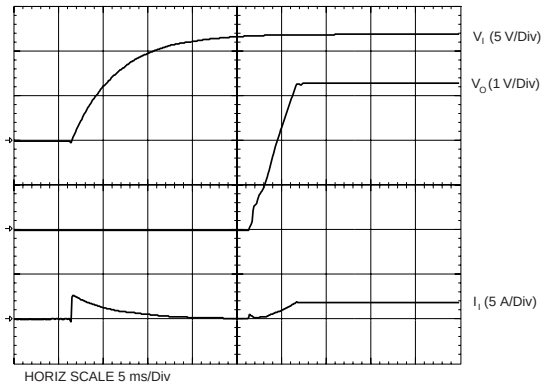
Figure 3–1



When the *Track* pin is connected to the input voltage the Auto-Track function is permanently disengaged. This allows the module to power up entirely under the control of its internal soft-start circuitry. When power up is under soft-start control, the output voltage rises to the set-point at a quicker and more linear rate.

From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically 8 ms-15 ms) before allowing the output voltage to rise.

Figure 3–2



The output then progressively rises to the module's set-point voltage. Figure 3-2 shows the soft-start power-up characteristic of the 18-A output product (PTH12020W), operating from a 12-V input bus and configured for a 3.3-V output. The waveforms were measured with a 5-A resistive load and the Auto-Track feature disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power-up is complete within 25 ms.

Over-Current Protection

For protection against load faults, all modules incorporate output over-current protection. Applying a load that exceeds the regulator's over-current threshold will cause the regulated output to shut down. Following shutdown a module will periodically attempt to recover by initiating a soft-start power-up. This is described as a "hiccup" mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

Over-Temperature Protection (OTP)

The PTH12020, PTH12030, and PTH12040 products have over-temperature protection. These products have an on-board temperature sensor that protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module's *Inhibit* control is internally pulled low. This

turns the output off. The output voltage will drop as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the the sensed temperature decreases by about 10 °C below the trip point.

Note: The over-temperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and will reduce the long-term reliability of the module. Always operate the regulator within the specified Safe Operating Area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

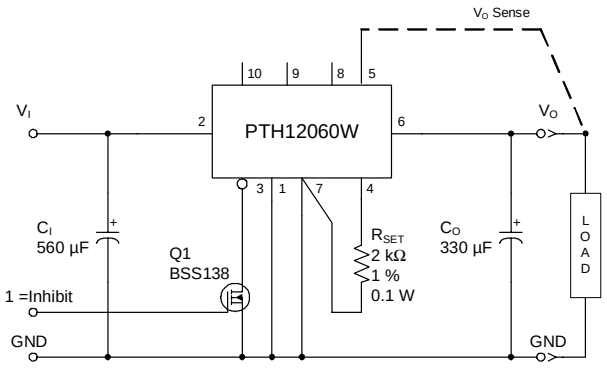
Output On/Off Inhibit

For applications requiring output voltage on/off control, each series of the PTH family incorporates an output *Inhibit* control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power modules function normally when the *Inhibit* pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_I with respect to *GND*.

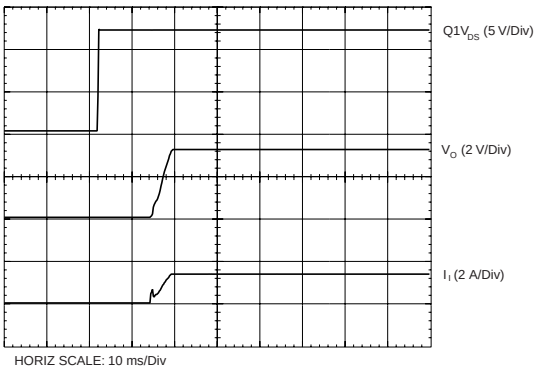
Figure 3-3 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The *Inhibit* input has its own internal pull-up to a potential of 5 V to 13.2 V (see footnotes to specification table). The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

Figure 3–3



Turning Q1 on applies a low voltage to the *Inhibit* control pin and disables the output of the module. If Q1 is then turned off, the module will execute a soft-start power-up sequence. A regulated output voltage is produced within 25 msec. Figure 3-4 shows the typical rise in both the output voltage and input current, following the turn-off of Q1. The turn off of Q1 corresponds to the rise in the waveform, Q1 V_{DS}. The waveforms were measured with a 5-A constant current load.

Figure 3–4



Remote Sense

Products with this feature incorporate an output voltage sense pin, V_O *Sense*. A remote sense improves the load regulation performance of the module by allowing it to compensate for any 'IR' voltage drop between its output and the load. An IR drop is caused by the high output current flowing through the small amount of pin and trace resistance.

To use this feature simply connect the V_O *Sense* pin to the V_O node, close to the load circuit (see data sheet standard application). If a sense pin is left open-circuit, an internal low-value resistor (15-Ω or less) connected between the pin and and the output node, ensures the output remains in regulation.

With the sense pin connected, the difference between the voltage measured directly between the V_O and *GND* pins, and that measured from V_O *Sense* to *GND*, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

Note: The remote sense feature is not designed to compensate for the forward drop of non-linear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

Auto-Track™ Function

The Auto-Track function is unique to the PTH/PTV family, and is available with all POLA products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications, that use dual-voltage VLSI ICs such as DSPs, micro-processors, and ASICs.

How Auto-Track Works

Auto-Track works by forcing the module's output voltage to follow a voltage presented at the *Track* control pin. This control range is limited to between 0 V and the module's set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module's output remains at its set-point [1]. As an example, if the Track pin of a 2.5-V regulator is at 1 V, the regulated output will be 1 V. But if the voltage at the Track pin rises to 3 V, the regulated output will not go higher than 2.5 V.

When under track control, the regulated output from the module follows the voltage at its Track pin on a volt-for-volt basis. By connecting the Track pin of a number of these modules together, the output voltages will follow a common signal during power-up and power-down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit [3]. For convenience the Track control incorporates an internal RC charge circuit. This operates off the module's input voltage to produce a suitable rising waveform at power up.

Typical Application

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant modules. Connecting the Track control pins of two or more modules forces the Track control of all modules to follow the same collective RC ramp waveform, and allows them to be controlled through a single transistor or switch; Q1 in Figure 3-5.

To initiate a power-up sequence, it is recommended that the Track control be first pulled to ground potential. This should be done at or before input power is applied to the modules, and then held for at least 10 ms thereafter. This brief period gives the modules time to complete their internal soft-start initialization. Applying a logic-level high signal to the on/off control in Figure 3-5 turns Q1 on, and applies a ground signal to the track control. After completing their internal soft-start intialization, the output of all modules will remain at zero volts while Q1 is on.

10 ms after a valid input voltage has been applied to the modules, Q1 may be turned off. This allows the track control voltage to automatically rise toward to the modules' input voltage. During this period the output voltage of each module will rise in unison with other modules, to its respective set-point voltage.

Figure 3-6 shows the output voltage waveforms from the circuit of Figure 3-5 after the on/off control is set from a high to a low-level voltage. The waveforms, V_O1 and V_O2 represent the output voltages from the two power modules, U1 (3.3 V) and U2 (2 V) respectively. V_O1 and V_O2 are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. Power down is the reverse of power up, and is accomplished by lowering the track control voltage back to zero volts. The important constraint is that a valid input voltage must be maintained until the power down is complete. It also requires that Q1 be turned off relatively slowly. This is so that the Track control voltage does not fall faster than Auto-Track's slew rate capability, which is 1 V/ms. The components R1 and C1 in Figure 3-5 limit the rate at which Q1 can pull down the Track control voltage. The values of 100 k-ohm and 0.1 µF correlate to a decay rate of about 0.17 V/ms.

The power-down sequence is initiated with a low-to-high transition at the on/off control input to the circuit. Figure 3-7 shows the power-down waveforms. As the Track control voltage falls below the nominal set-point voltage of each power module, then its output voltage decays with all the other modules under Auto-Track control.

Notes on Use of Auto-Track™

1. The Track pin voltage must be allowed to rise above the module's set-point voltage before the module can regulate at its adjusted set-point voltage.
2. The Auto-Track function will track almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absloute maximum voltage that may be applied to the Track pin is the input voltage V_I.
4. The module will not follow a voltage at its Track control input until it has completed its soft-start initialization. This takes about 10 ms from the time that the module has sensed that a valid voltage has been applied its input. During this period, it is recommended that the Track pin be held at ground potential.
5. The module is capable of both sinking and sourcing current when following a voltage at its Track pin. Therefore startup into an output prebias cannot be supported when a module is under Auto-Track control. *Note: A pre-bias holdoff is not necessary when all supply voltages rise simultaneously under the control of Auto-Track.*
6. The Auto-Track function can be disabled by connecting the *Track* pin to the input voltage (V_I). When Auto-Track is disabled, the output voltage will rise at a quicker and more linear rate after input power is applied.

Figure 3–5; Sequenced Power Up & Power Down Using Auto-Track

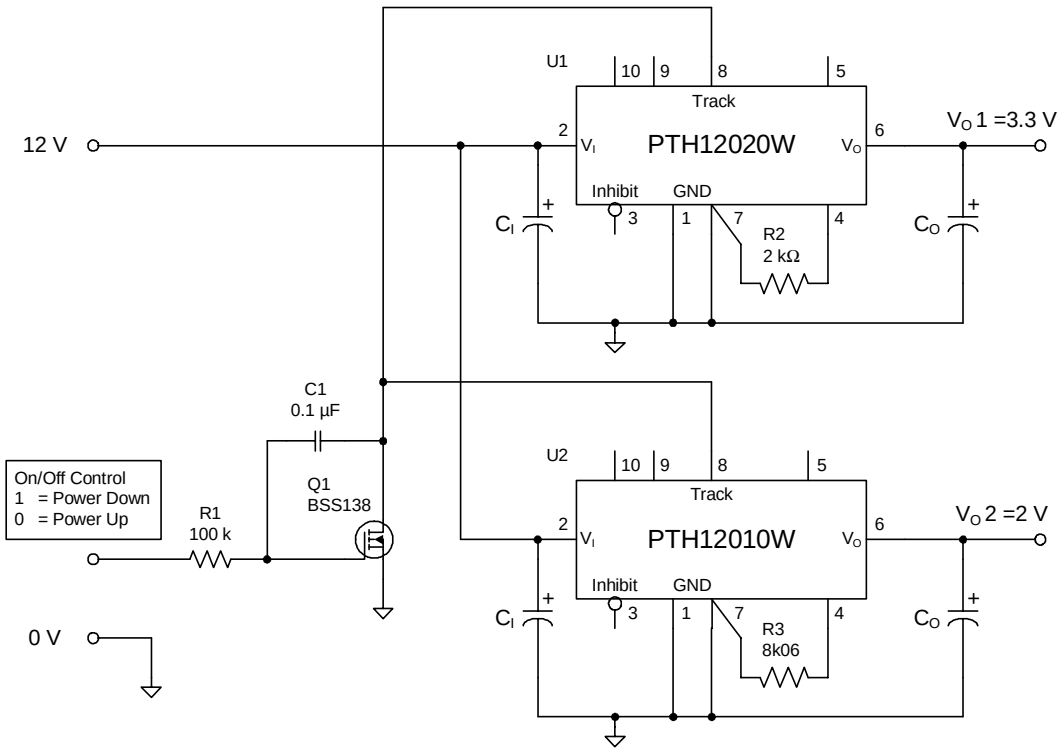


Figure 3–6; Simultaneous Power Up with Auto-Track Control

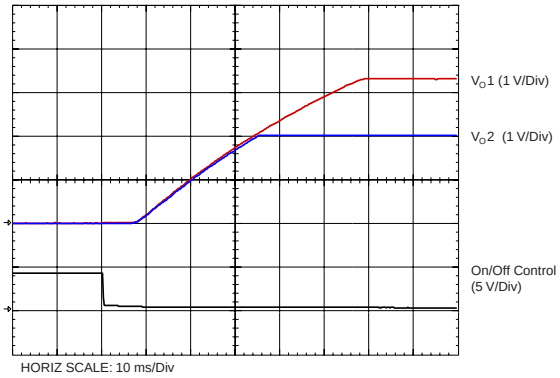
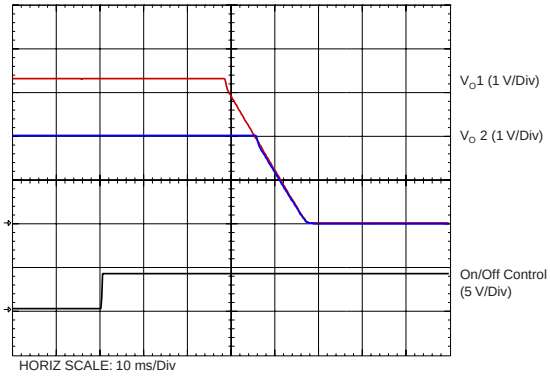


Figure 3–7; Simultaneous Power Down with Auto-Track Control



Margin Up/Down Controls

The PTH12060, PTH12010, PTH12020, PTH12030, and PTH12040 products incorporate *Margin Up* and *Margin Down* control inputs. These controls allow the output voltage to be momentarily adjusted,[1] either up or down, by a nominal 5%. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. The ±5% change is applied to the adjusted output voltage, as set by the external resistor, R_{SET} at the *V_O Adjust* pin.

The 5 % adjustment is made by pulling the appropriate margin control input directly to the *GND* terminal [2]. A low-leakage open-drain device, such as an n-channel MOSFET or p-channel JFET is recommended for this purpose [3]. Adjustments of less than 5 % can also be accommodated by adding series resistors to the control inputs. The value of the resistor can be selected from Table 3-2, or calculated using the following formula.

Up/Down Adjust Resistance Calculation

To reduce the margin adjustment to a value less than 5%, series resistors are required (See R_D and R_U in Figure 3-8). For the same amount of adjustment, the resistor value calculated for R_U and R_D will be the same. The formula is as follows.

$$R_U \text{ or } R_D = \frac{499}{\Delta\%} - 99.8 \quad k\Omega$$

Where $\Delta\%$ = The desired amount of margin adjust in percent.

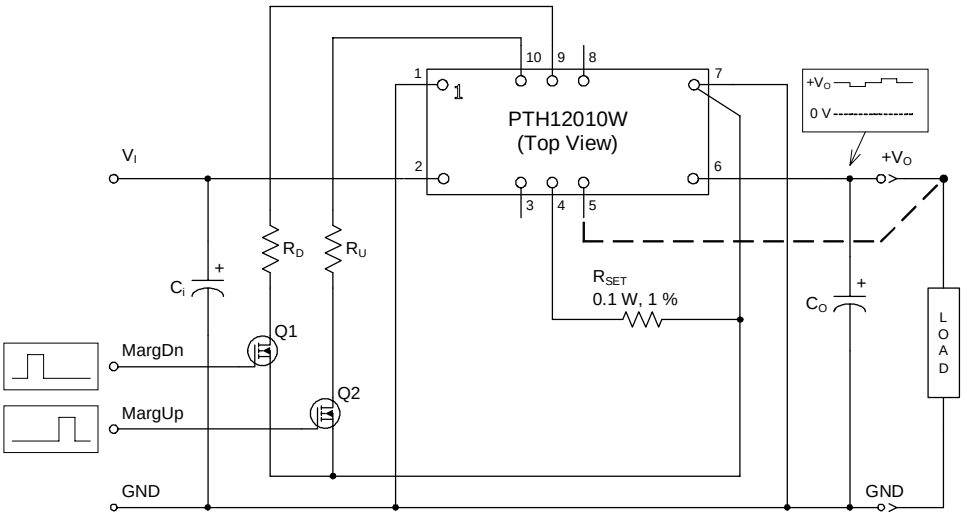
Notes:

1. The *Margin Up** and *Margin Dn** controls were not intended to be activated simultaneously. If they are their affects on the output voltage may not completely cancel, resulting in the possibility of a slightly higher error in the output voltage set point.
2. The ground reference should be a direct connection to the module's signal *GND* (the GND connection recommended for R_{SET}). This will produce a more accurate adjustment at the load circuit terminals. The transistors Q1 and Q2 should be located close to the regulator.
3. The Margin Up and Margin Dn control inputs are not compatible with devices that source voltage. This includes TTL logic. These are analog inputs and should only be controlled with a true open-drain device (preferably a discrete MOSFET transistor). The device selected should have low off-state leakage current. Each input sources 8 µA when grounded, and has an open-circuit voltage of 0.8 V.

Table 3-2; Margin Up/Down Resistor Values

% Adjust	R_U / R_D
5	0.0 kΩ
4	24.9 kΩ
3	66.5 kΩ
2	150.0 kΩ
1	397.0 kΩ

Figure 3–8; Margin Up/Down Application Schematic



Pre-Bias Startup Capability

The capability to start up into an output pre-bias condition is available to all the 12-V input series of PTH/PTV power modules.

A pre-bias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes, sometimes used as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, such modules can sink as well as source output current. The 12-V input PTH modules all incorporate synchronous rectifiers, but will not sink current during startup, or whenever the *Inhibit* pin is held low. Startup includes an initial delay (approx. 8 - 15 ms), followed by the rise of the output voltage under the control of the module's internal soft-start mechanism; see Figure 3-9.

Conditions for Pre-Bias Holdoff

In order for the module to allow an output pre-bias voltage to exist (and not sink current), certain conditions must be maintained. The module holds off a pre-bias voltage when the *Inhibit* pin is held low, and whenver the output is allowed to rise under soft-start control. Power up under soft-start control occurs upon the removal of the ground signal to the *Inhibit* pin (with input voltage applied), or when input power is applied with Auto-Track disabled [1]. To further ensure that the regulator doesn't sink output current, (even with a ground signal applied to its *Inhibit*), the input voltage must always be greater than the applied pre-bias source. This condition must exist throughout the power-up sequence.

The soft-start period is complete when the output begins rising above the pre-bias voltage. Once it is complete the module functions as normal, and will sink current if a voltage higher than the nominal regulation value is applied to its output.

Note: If a pre-bias condition is not present, the soft-start period will be complete when the output voltage has risen to either the set-point voltage, or the voltage applied at the module's Track control pin, whichever is lowest.

Demonstration Circuit

Figure 3-10 shows the startup waveforms for the demonstration circuit shown in Figure 3-11. The initial rise in V_O2 is the pre-bias voltage, which is passed from the VCCIO to the VCORE voltage rail through the ASIC. Note that the output current from the PTH12010L module (I_O2) is negligible until its output voltage rises above the applied pre-bias.

Figure 3-9; PTH12020W Startup

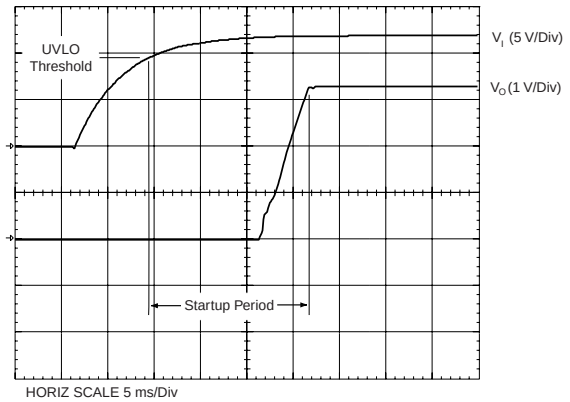
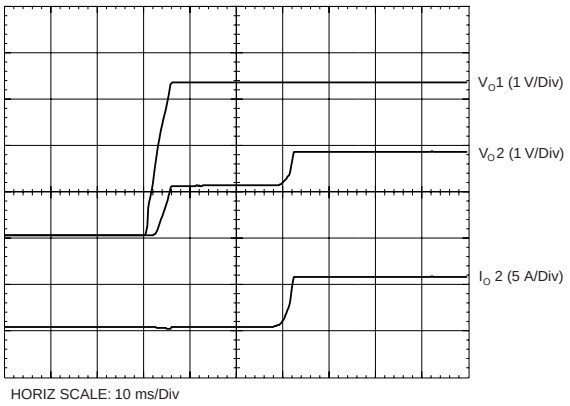


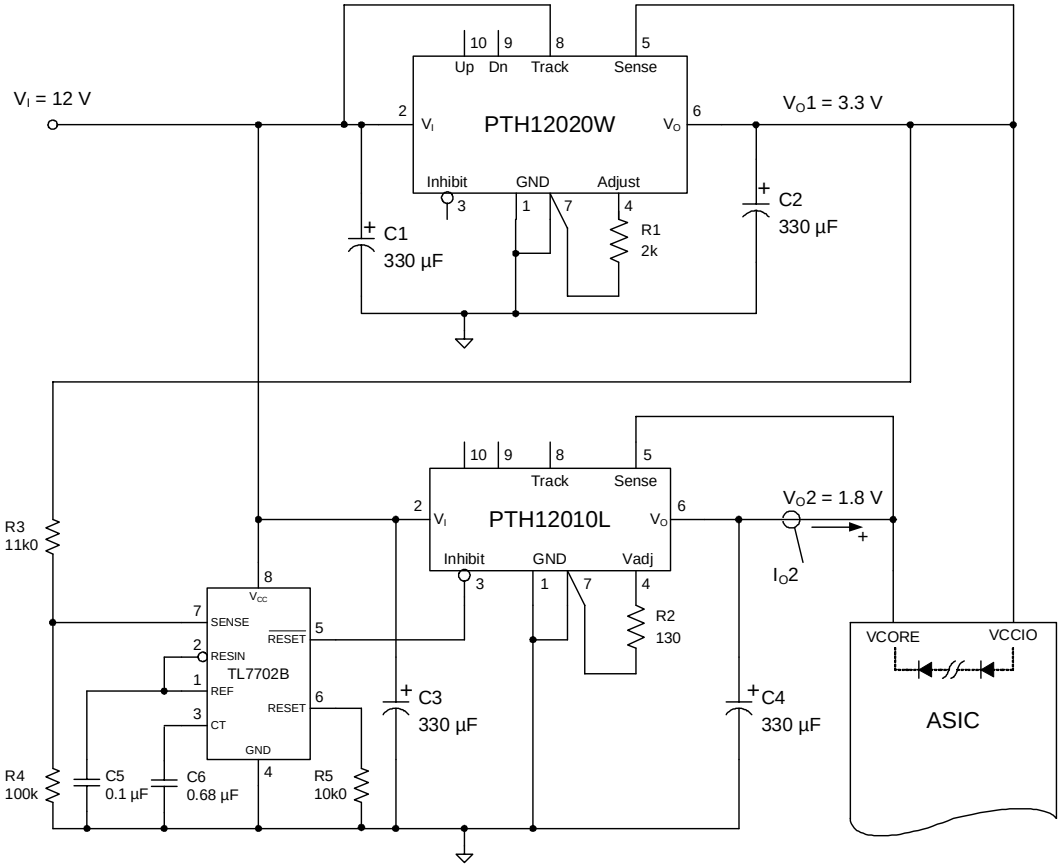
Figure 3–10; Pre-Bias Startup Waveforms



Notes

1. The pre-bias start-up feature is not compatible with Auto-Track. If the rise in the output is limited by the voltage applied to the *Track* control pin, the output will sink current during the period that the track control voltage is below that of the back-feeding source. For this reason, it is recommended that Auto-Track be disabled when not being used. This is accomplished by connecting the *Track* pin to the input voltage, V_I. This raises the *Track* pin voltage well above the set-point voltage prior to the module's start up, thereby defeating the Auto-Track feature.

Figure 3–11; Application Circuit Demonstrating Pre-Bias Startup



PACKAGING INFORMATION

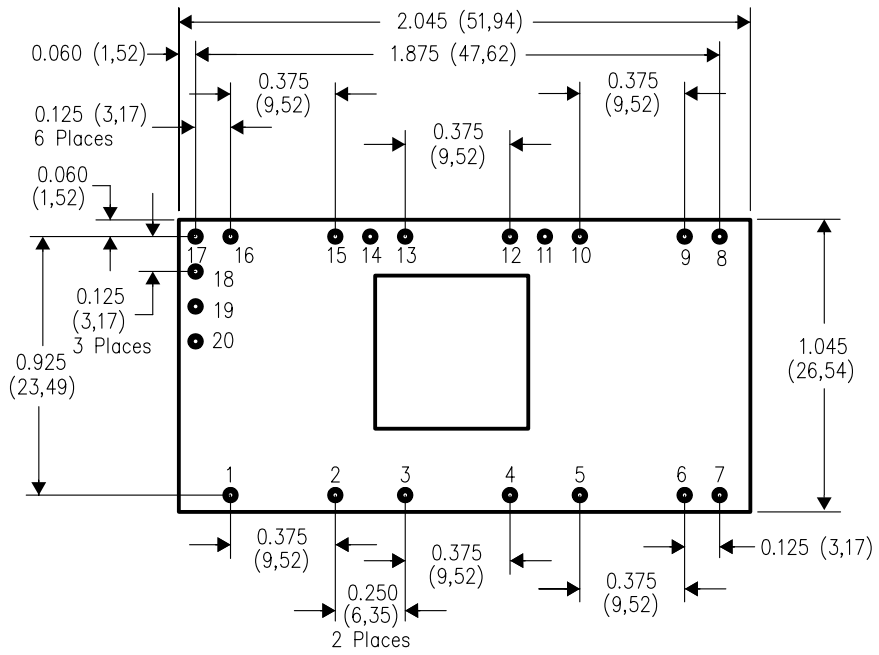
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
PTH12040WAH	ACTIVE	DIP MODULE	EVF	20	12	TBD	Call TI	Level-1-235C-UNLIM
PTH12040WAS	ACTIVE	DIP MODULE	EVG	20	12	TBD	Call TI	Level-1-235C-UNLIM

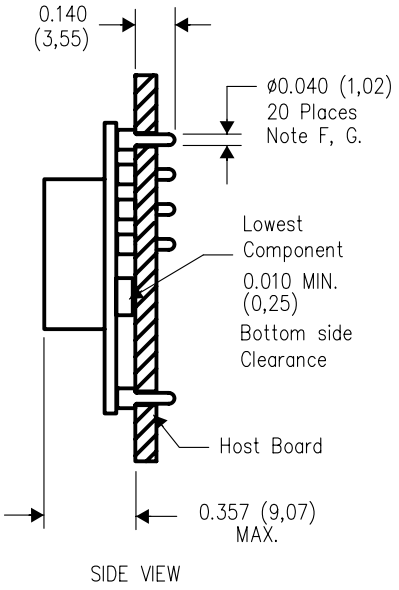
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

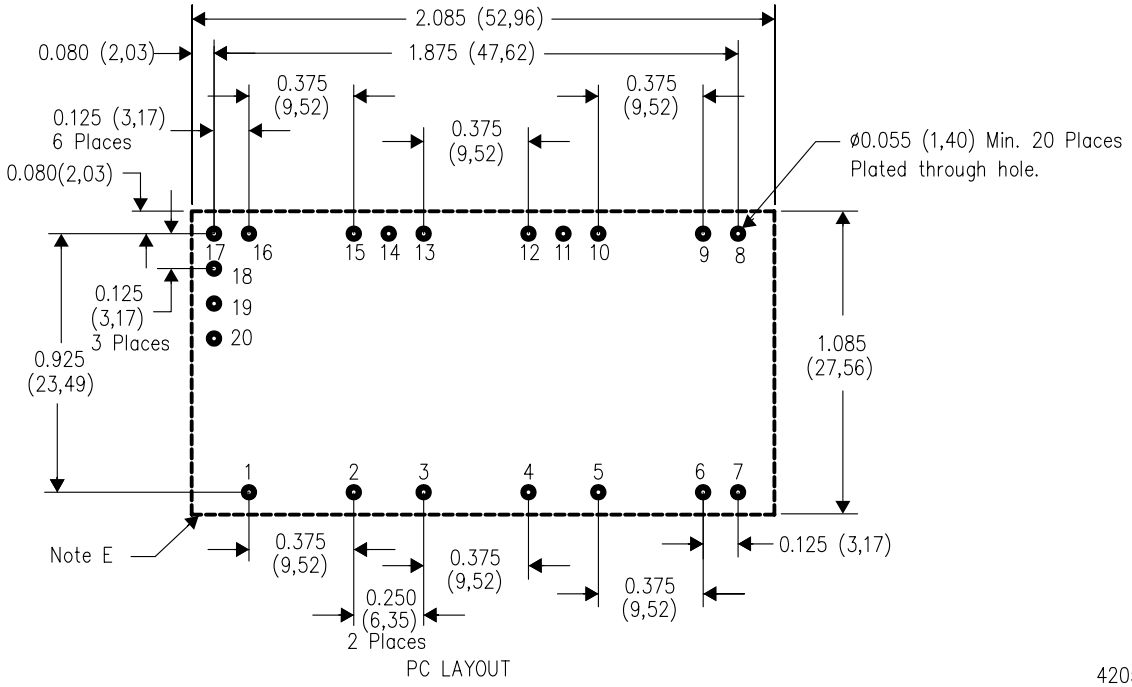
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

EVF (R–PDSS–T20) DOUBLE SIDED MODULE



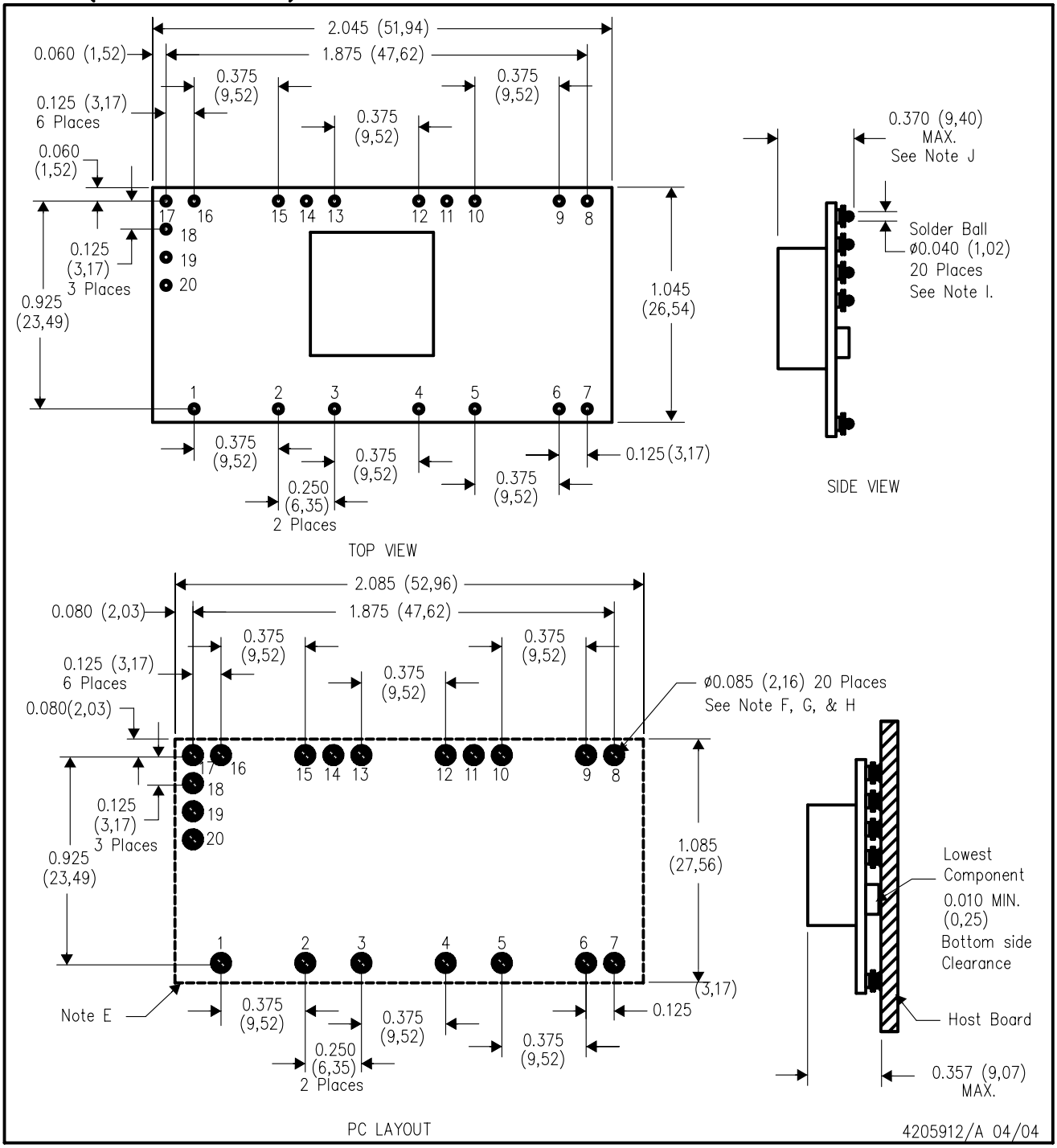




4205911/A 04/04

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

EVG (R–PDSS–T20) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265