SIEMENS

2M × 72-Bit EDO-DRAM Module (ECC - Module)

HYM 72V2005GS-50/-60

168 pin buffered DIMM Module

- 168 pin JEDEC Standard, Buffered 8 Byte Dual In-Line Memory Module for PC main memory applications
- 1 bank 2 M x 72 organisation
- Optimized for ECC applications
- Extended Data Out (EDO)
- Performance:

		-50	-60	
t_{RAC}	$\overline{RAS}$ access time	50	60	ns
t_{CAC}	$\overline{CAS}$ access time	18	20	ns
t_{AA}	Access time from address	30	35	ns
t_{RC}	Read/Write cycle time	84	104	ns
t_{HPC}	Fast page mode cycle time	20	25	ns

- Single + 3.3V ± 0.3 V supply
- $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs and clock fully LVTTL & LVCMOS compatible
- 4 Byte interleave enabled, Dual Address inputs (A0/B0)
- Buffered inputs excepts $\overline{RAS}$ and DQ
- Parallel Presence Detects
- Utilizes nine 2M × 8 -DRAMs and BiCMOS buffers/line drivers
- 2048 refresh cycles / 32 ms with 11 / 10 addressing
- Gold contact pad
- Double sided module with 25.35 mm (1000 mil) height

The HYM 72V2005GS-50/-60 is a 16 MByte DRAM module organized as 2 097 152 words by 72-bit in a 168-pin, dual read-out, single-in-line package comprising nine HYB3117805BSJ 2M × 8 EDO DRAMs in 400 mil wide SOJ-28 - packages mounted together with ceramic decoupling capacitors on a PC board. All inputs except $\overline{RAS}$ and DQ are buffered by using BiCMOS buffers/ line drivers.

Each HYB3117805BSJ is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The density and speed of the module can be detected by the use of presence detect pins.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYM 72V2005GS-50		L-DIM-168-22	DRAM module (access time 50 ns)
HYM 72V2005GS-60		L-DIM-168-22	DRAM module (access time 60 ns)

Pin Names

A0-A11,B0	Row Address Inputs
A0-A10,B0	Column Address Inputs
DQ0 - DQ71	Data Input/Output
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS2}$	Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$	Read / Write Input
$\overline{OE0}$, $\overline{OE2}$	Output Enable
Vcc	Power (+3.3 Volt)
Vss	Ground
PD1 - PD8	Presence Detect Pins
$\overline{PDE}$	Presence Detect Enable
ID0 , ID1	ID indentification bit
N.C.	No Connection

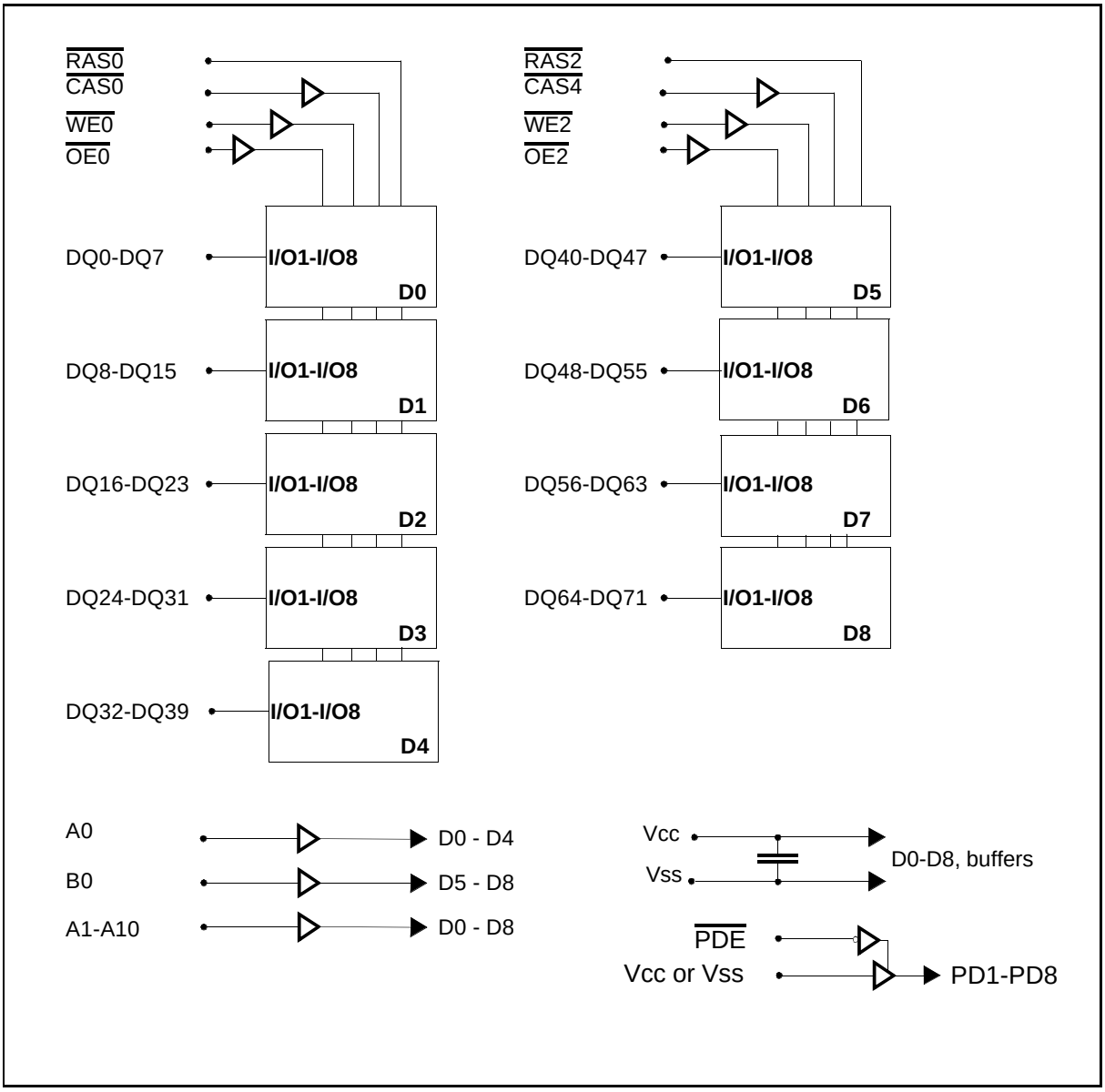
Presence-Detect and ID-pin Truth Table:

Module	ID0	ID1	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8
HYM 72V2005GS-50	Vss	Vss	1	0	0	1	1	0	0	0
HYM 72V2005GS-60	Vss	Vss	1	0	0	1	1	1	1	0

Note: 1 = High Level (Driver Output) , 0 = Low Level (Driver Output) for $\overline{PDE}$ active (ground) . For $\overline{PDE}$ at a high level all PD terminal are in tri-state.

Pin Configuration

PIN #	Symbol	PIN #	Symbol		PIN #	Symbol	PIN #	Symbol
1	VSS	43	VSS		85	VSS	127	VSS
2	DQ0	44	OE2		86	DQ36	128	NC
3	DQ1	45	RAS2		87	DQ37	129	NC
4	DQ2	46	CAS4		88	DQ38	130	NC
5	DQ3	47	NC		89	DQ39	131	NC
6	VCC	48	WE2		90	VCC	132	PDE
7	DQ4	49	VCC		91	DQ40	133	VCC
8	DQ5	50	NC		92	DQ41	134	NC
9	DQ6	51	NC		93	DQ42	135	NC
10	DQ7	52	DQ18		94	DQ43	136	DQ54
11	DQ8	53	DQ19		95	DQ44	137	DQ55
12	VSS	54	VSS		96	VSS	138	VSS
13	DQ9	55	DQ20		97	DQ45	139	DQ56
14	DQ10	56	DQ21		98	DQ46	140	DQ57
15	DQ11	57	DQ22		99	DQ47	141	DQ58
16	DQ12	58	DQ23		100	DQ48	142	DQ59
17	DQ13	59	VCC		101	DQ49	143	VCC
18	VCC	60	DQ24		102	VCC	144	DQ60
19	DQ14	61	NC		103	DQ50	145	NC
20	DQ15	62	NC		104	DQ51	146	NC
21	DQ16	63	NC		105	DQ52	147	NC
22	DQ17	64	NC		106	DQ53	148	NC
23	VSS	65	DQ25		107	VSS	149	DQ61
24	NC	66	DQ26		108	NC	150	DQ62
25	NC	67	DQ27		109	NC	151	DQ63
26	VCC	68	VSS		110	VCC	152	VSS
27	WE0	69	DQ28		111	NC	153	DQ64
28	CAS0	70	DQ29		112	NC	154	DQ65
29	NC	71	DQ30		113	NC	155	DQ66
30	RAS0	72	DQ31		114	NC	156	DQ67
31	OE0	73	VCC		115	NC	157	VCC
32	VSS	74	DQ32		116	VSS	158	DQ68
33	A0	75	DQ33		117	A1	159	DQ69
34	A2	76	DQ34		118	A3	160	DQ70
35	A4	77	DQ35		119	A5	161	DQ71
36	A6	78	VSS		120	A7	162	VSS
37	A8	79	PD1		121	A9	163	PD2
38	A10	80	PD3		122	NC	164	PD4
39	NC	81	PD5		123	NC	165	PD6
40	VCC	82	PD7		124	VCC	166	PD8
41	NC	83	ID0 (VSS)		125	NC	167	ID1 (VSS)
42	NC	84	VCC		126	B0	168	VCC



Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 ℃
Storage temperature range..... – 55 to + 125 ℃
Input/output voltage ..... -0.5 to min (Vcc+0.5, 4.6) V
Power supply voltage..... – 0.5V to 4.6 V
Power dissipation..... 5,8 W
Data out current (short circuit) ..... 50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics
T_A = 0 to 70 ℃; V_{CC} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.0	Vcc + 0.3	V	1)
Input low voltage	V_{IL}	– 0.3	0.8	V	1)
Output high voltage (LVTTL) Output „H“level voltage (I_{OUT} = – 2 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (LVTTL) Output „L“level voltage (I_{OUT} = + 2 mA)	V_{OL}	–	0.4	V	1)
Output high voltage (LVCMOS) Output „H“level voltage (I_{OUT} = – 100 µA)	V_{OH}	Vcc-0.2	–	V	1)
Output low voltage (LVCMOS) Output „L“level voltage (I_{OUT} = + 100 µA)	V_{OL}	–	0.2	V	1)
Input leakage current (0 V < V_{IN} < Vcc, all other pins = 0 V)	$I_{I(L)}$	– 20	20	µA	1)
Output leakage current (DO is disabled, 0 V < V_{OUT} < Vcc)	$I_{O(L)}$	– 20	20	µA	1)
Average V_{CC} supply current: -50 version -60 version ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)	I_{CC1}	 – –	 1080 990	 mA mA	2) 3) 4)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = *2.4V*, one address change within 15,6 µs trc)	I_{CC2}	–	50	mA	–

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles:	I_{CC3}				2) 4)
-50 version		–	1080	mA	
-60 version		–	990	mA	
($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					
Average V_{CC} supply current during hyper page mode (EDO):	I_{CC4}				2) 3) 4)
-50 version		–	630	mA	
-60 version		–	495	mA	
		–			
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V, one address change within 15,6 µs trc)	I_{CC5}	–	30	mA	–
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode:	I_{CC6}				2) 4)
-50 version		–	1080	mA	
-60 version		–	990	mA	
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					

Capacitance

T_A = 0 to 70 °C; V_{CC} = 3.3 V ± 0.3 V; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11,B0)	C_{I1}	–	10	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	–	50	pF
Input capacitance ($\overline{CAS0}$, $\overline{CAS4}$)	C_{I3}	–	15	pF
Input capacitance ($\overline{WE0}$,$\overline{WE2}$,$\overline{OE0}$,$\overline{OE2}$)	C_{I4}	–	15	pF
I/O capacitance (DQ0-DQ71)	C_{IO1}	–	15	pF

AC Characteristics (note: 5,6,7,8)
T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3 V

Parameter	Symbol	-50		-60		Unit	Note
		min.	max.	min.	max.		
common parameters							
Random read or write cycle time	t_{RC}	84	–	104	–	ns	
RAS precharge time	t_{RP}	30	–	40	–	ns	
RAS pulse width	t_{RAS}	50	100k	60	100k	ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10k	10	10k	ns	
Row address setup time	t_{ASR}	5	–	5	–	ns	9
Row address hold time	t_{RAH}	6	–	8	–	ns	10
Column address setup time	t_{ASC}	2	–	2	–	ns	11
Column address hold time	t_{CAH}	13	–	15	–	ns	9
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	10	32	12	40		12
$\overline{RAS}$ to column address delay time	t_{RAD}	8	20	10	25	ns	12
$\overline{RAS}$ hold time	t_{RSH}	18	–	20	–	ns	9
$\overline{CAS}$ hold time	t_{CSH}	38	–	48	–	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	9
Transition time (rise and fall)	t_T	1	30	1	30	ns	7
Refresh period	t_{REF}	–	64	–	64	ms	
Read Cycle							
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	ns	13,14
Access time from $\overline{CAS}$	t_{CAC}	–	18	–	20	ns	9,13,14
Access time from column address	t_{AA}	–	30	–	35	ns	9,13, 15
$\overline{OE}$ access time	t_{OEA}	–	18	–	20	ns	9,13
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns	9
Read command setup time	t_{RCS}	2	–	2	–	ns	11
Read command hold time	t_{RCH}	2	–	2	–	ns	11,16
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	16
$\overline{CAS}$ to output in low-Z	t_{CLZ}	2	–	2	–	ns	11,13
Output buffer turn-off delay	t_{OFF}	–	18	–	20	ns	9,17

AC Characteristics (cont'd) (note: 5,6,7,8)
T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3 V

Parameter	Symbol	-50		-60		Unit	Note
		min.	max.	min.	max.		
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	–	18	–	20	ns	9,17
$\overline{CAS}$ delay time from Din	t_{DZC}	0	–	0	–	ns	18
Data to $\overline{OE}$ low delay	t_{DZO}	0	–	0	–	ns	18
$\overline{CAS}$ high to data delay	t_{CDD}	15	–	18	–	ns	9,19
$\overline{OE}$ high to data delay	t_{ODD}	15	–	18	–	ns	9,19
Write Cycle							
Write command hold time	t_{WCH}	13	–	15	–	ns	9
Write command pulse width	t_{WP}	8	–	10	–	ns	
Write command setup time	t_{WCS}	2	–	2	–	ns	11,20
Write command to $\overline{RAS}$ lead time	t_{RWL}	18	–	20	–	ns	9
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	–	15	–	ns	
Data setup time	t_{DS}	-2	–	-2	–	ns	10,21
Data hold time	t_{DH}	13	–	15	–	ns	9,21
Read-Modify-Write Cycle							
Read-write cycle time	t_{RWC}	118	–	143	–	ns	9
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	66	–	77	–	ns	11,21
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	29	–	34	–	ns	11,21
Column address to $\overline{WE}$ delay time	t_{AWD}	41	–	49	–	ns	11,21
$\overline{OE}$ command hold time	t_{OEH}	8	–	11	–	ns	10
Hyper Page Mode (EDO) Cycle							
Hyper page mode cycle time	t_{PC}	20	–	25	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	32	–	37	ns	9,13
Output data hold time	t_{COH}	3	–	3	–	ns	10
$\overline{RAS}$ pulse width	t_{RAS}	50	200k	60	200k	ns	
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHCP}	32	–	37	–	ns	9
$\overline{OE}$ setup time prior to $\overline{CAS}$	t_{OES}	5	–	5	–	ns	

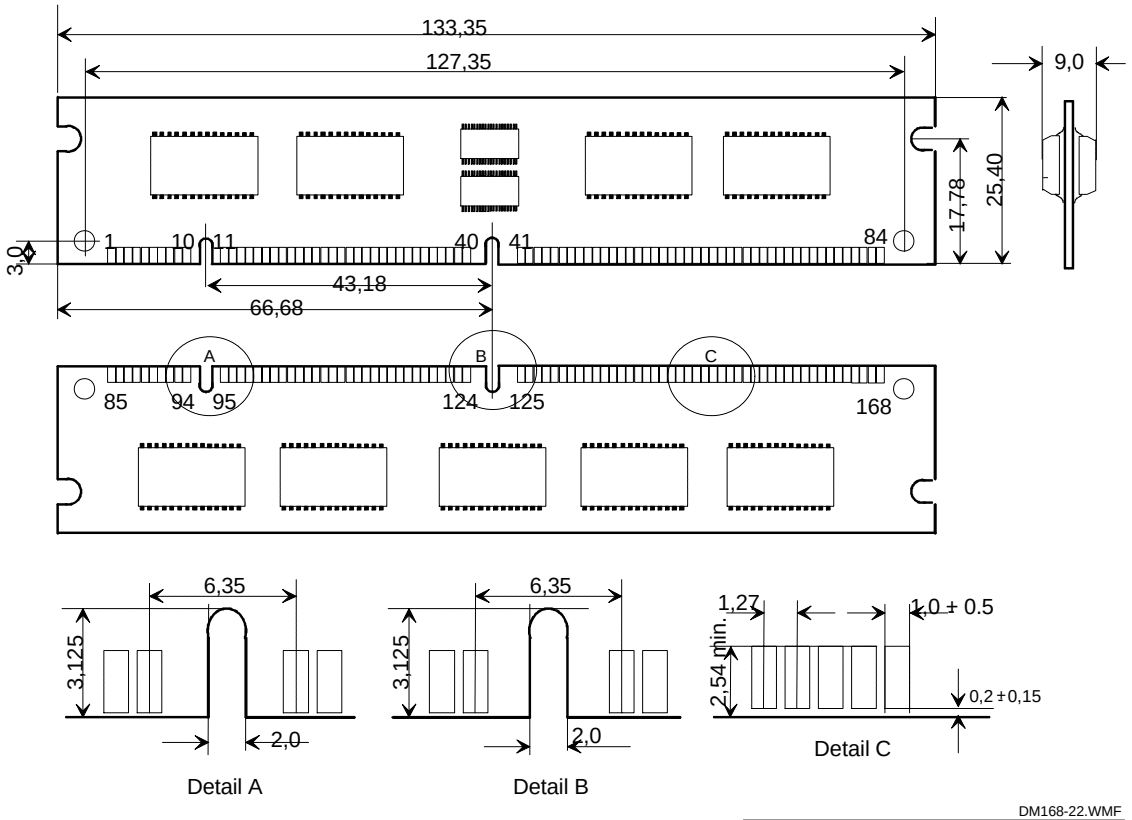
AC Characteristics (cont'd) (note: 5,6,7,8)
T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3 V

Parameter	Symbol	-50		-60		Unit	Note
		min.	max.	min.	max.		
Hyper Page Mode Read-Modify-Write Cycle							
Hyper page mode read-write cycle time	t_{PRWC}	60	–	70	–	ns	11
$\overline{CAS}$ precharge to $\overline{WE}$	t_{CPWD}	43	–	51	–	ns	11,21
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle							
$\overline{CAS}$ setup time	t_{CSR}	12	–	12	–	ns	11
$\overline{CAS}$ hold time	t_{CHR}	8	–	8	–	ns	10
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	ns	
Write to $\overline{RAS}$ precharge time	t_{WRP}	12	–	12	–	ns	11
Write hold time referenced to $\overline{RAS}$	t_{WRH}	8	–	8	–	ns	10
Presence Detect Read Cycle							
$\overline{PDE}$ to valid presence detect data	t_{PD}	–	10	–	10	ns	
$\overline{PDE}$ inactive to presence detects inactive	t_{PDOFF}	0	10	0	10	ns	

Notes:

1) All voltages are referenced to VSS.
2) ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.
3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.
4) Address can be changed once or less while $\overline{RAS}$ = Vil.In the case of ICC4 it can be changed once or less during a hyper page mode (EDO) cycle (thpc).
5) An initial pause of 100 µs is required after power-up followed by 8 RAS-only-refresh cycles, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6) AC measurements assume tT = 2 ns.
7) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH and VIL.
8) The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, addresses) maximum delay, no pulse shrinkage to the DRAM device timings. The data and RAS signals are not buffered, which preserves the DRAMs access specification of 50ns and 60ns.
9) A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
10) A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
11) A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
12) A -2ns (min.) and a -5ns (max.) timing skew from the DRAM to the module resulted from the addition of line drivers.
13) Measured with the specified current load and 100 pF at Voh = 2.0 V and Vol = 0.8 V. Access time is determined by the latter of tRAC, tCAC, tAA, tCPA, tOEA. tCAC is measured from tristate.
14) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.
15) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.
16) Either tRCH or tRRH must be satisfied for a read cycle.
17) tOFF (max.) and tOEZ (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels. tOFF is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.
18) Either tDZC or tDZO must be satisfied.
19) Either tCDD or tODD must be satisfied.
20) tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS > tWCS (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if tRWD > tRWD (min.), tCWD > tCWD (min.), tAWD > tAWD (min.) and tCPWD > tCPWD (min.) , the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
21) These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.

L-DIM-168-22
Module package
(dual read-out, single in-line memory module)



DM168-22.WMF

preliminary drawing