

**FEATURES**

- Low cost integrated amplifier with step attenuator
- Attenuation Range: 0-58 dB, adjustable in 1dB increments via a 3 wire serial control
- Meets DOCSIS distortion requirements at +60dBmV output signal level
- Low distortion and low noise
- Frequency range: 5-100MHz
- 5 Volt operation
- -40 to +85 °C temperature range

**APPLICATIONS**

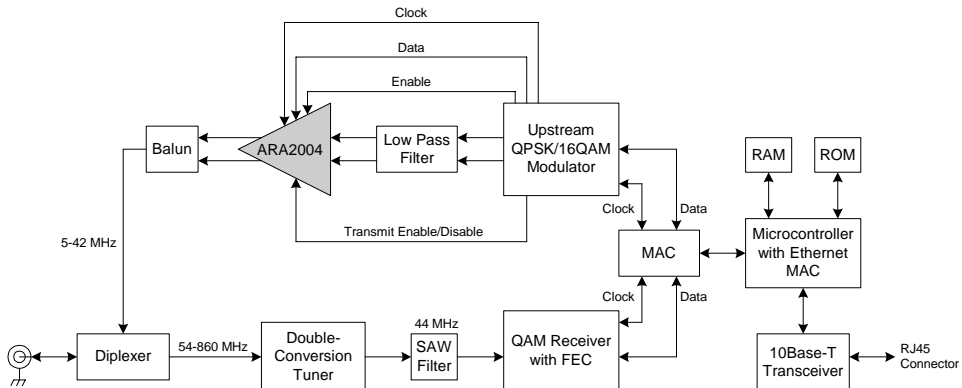
- MCNS/DOCSIS Compliant Cable Modems
- CATV Interactive Set-Top Box
- Telephony over Cable Systems
- OpenCable Set-Top Box
- Residential Gateway



**PRODUCT DESCRIPTION**

The ARA2004 is designed to provide the reverse path amplification and output level control functions in a CATV Set-Top Box or Cable Modem. It incorporates a digitally controlled precision step attenuator that is preceded by an ultra low noise amplifier stage, and followed by an ultra-linear output driver amplifier. This device uses a balanced circuit design that exceeds the MCNS/DOCSIS requirement for harmonic performance at a +60dBmV output level while only requiring a single polarity +5V supply. Both the input

and output are matched to 75 ohms with an appropriate transformer. The precision attenuator provides up to 58 dB of attenuation in 1 dB increments via a three-wire serial interface. With external passive components, this device meets IEC 1000-4-12 and ANSI/IEEE C62.41-1991 100KHz ringwave tests, as well as IEC1000-4-5 1.2/50µs surge tests. The ARA2004 is offered in a 28-pin SSOP package featuring an exposed paddle on the bottom of the package.



**Figure 1: Cable Modem or Set Top Box Application Diagram**

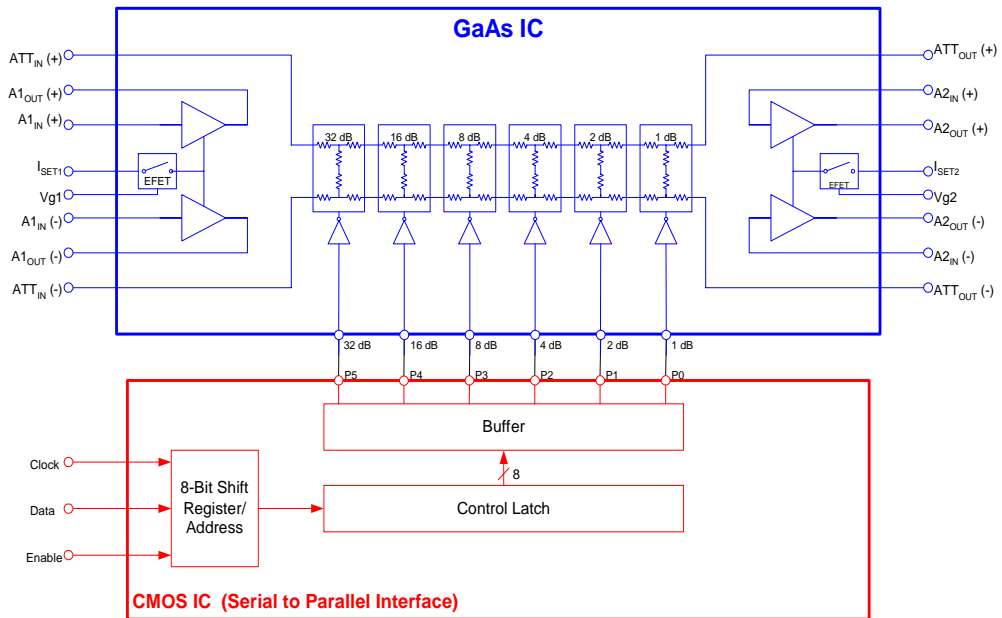


Figure 2: Functional Block Diagram

1	GND	GND	28
2	V <sub>ATTN</sub>	N/C	27
3	ATT <sub>IN</sub> (+)	ATT <sub>OUT</sub> (+)	26
4	A1 <sub>OUT</sub> (+)	A2 <sub>IN</sub> (+)	25
5	A1 <sub>IN</sub> (+)	A2 <sub>OUT</sub> (+)	24
6	Vg1	Vg2	23
7	I <sub>SET1</sub>	I <sub>SET2</sub>	22
8	A1 <sub>IN</sub> (-)	A2 <sub>OUT</sub> (-)	21
9	A1 <sub>OUT</sub> (-)	A2 <sub>IN</sub> (-)	20
10	ATT <sub>IN</sub> (-)	ATT <sub>OUT</sub> (-)	19
11	V <sub>CMOS</sub>	GND <sub>CMOS</sub>	18
12	CLK	N/C	17
13	DAT	N/C	16
14	En	N/C	15

Figure 3: Pin Out

Table 1: Pin Description

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	GND	Ground	15	N/C	No Connection <sup>(1)</sup>
2	V <sub>ATTN</sub>	Supply for Attenuator	16	N/C	No Connection <sup>(1)</sup>
3	ATT <sub>IN</sub> (+)	Attenuator (+) Input <sup>(2)</sup>	17	N/C	No connection <sup>(1)</sup>
4	A1 <sub>OUT</sub> (+)	Amplifier A1 (+) Output	18	GND <sub>CMOS</sub>	Ground for Digital CMOS Circuit
5	A1 <sub>IN</sub> (+)	Amplifier A1 (+) Input <sup>(2)</sup>	19	ATT <sub>OUT</sub> (-)	Attenuator (-) Output <sup>(2)</sup>
6	Vg1	Amplifier A1 (+/-) Control	20	A2 <sub>IN</sub> (-)	Amplifier A2 (-) Input <sup>(2)</sup>
7	I <sub>SET1</sub>	Amplifier A1 (+/-) Current Adjust	21	A2 <sub>OUT</sub> (-)	Amplifier A2 (-) Output
8	A1 <sub>IN</sub> (-)	Amplifier A1 (-) Input <sup>(2)</sup>	22	I <sub>SET2</sub>	Amplifier A2 (+/-) Current Adjust
9	A1 <sub>OUT</sub> (-)	Amplifier A1 (-) Output	23	Vg2	Amplifier A2 (+/-) Control
10	ATT <sub>IN</sub> (-)	Attenuator (-) Input <sup>(2)</sup>	24	A2 <sub>OUT</sub> (+)	Amplifier A2 (+) Output
11	V <sub>CMOS</sub>	Supply For Digital CMOS Circuit	25	A2 <sub>IN</sub> (+)	Amplifier A2 (+) Input <sup>(2)</sup>
12	CLK	Clock	26	ATT <sub>OUT</sub> (+)	Attenuator (+) Output <sup>(2)</sup>
13	DAT	Data	27	N/C	No Connection <sup>(1)</sup>
14	En	Enable	28	GND	Ground

## Notes:

(1) All N/C pins should be grounded.

(2) Pins should be AC-coupled. No external DC bias should be applied.

## ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Analog Supply (pins 2, 4, 9, 21, 24)	0	9	VDC
Digital Supply: $V_{CMOS}$ (pin 11)	0	6	VDC
Amplifier Controls $V_{g1}$ , $V_{g2}$ (pins 6, 23)	-5	2	V
RF Power at Inputs (pins 5, 8)	-	+60	dBmV
Digital Interface (pins 12, 13, 14)	-0.5	$V_{CMOS}+0.5$	V
Storage Temperature	-55	+200	°C
Soldering Temperature	-	260	°C
Soldering Time	-	5	Sec

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Notes:

1. Pins 3, 5, 8, 10, 19, 20, 25 and 26 should be AC-coupled. No external DC bias should be applied.
2. Pins 7 and 22 should be grounded or pulled to ground through a resistor. No external DC bias should be applied.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT
Amplifier Supply: $V_{DD}$ (pins 4, 9, 21, 24)	4.5	5	7	VDC
Attenuator Supply: $V_{ATTN}$ (pin 2)	$V_{DD}-0.5$	5	7	VDC
Digital Supply: $V_{CMOS}$ (pin 11)	3.0	-	5.5	VDC
Digital Interface	0	-	$V_{CMOS}$	V
Amplifier Controls $V_{g1}$ , $V_{g2}$ (pins 6, 23)	-5	1	2	V
Case Temperature	-40	25	85	°C

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Table 4: DC Electrical Specifications

$T_A=25^{\circ}\text{C}$ ;  $V_{DD}$ ,  $V_{ATTN}$ ,  $V_{CMOS} = +5.0\text{ VDC}$ ;  $V_{g1}$ ,  $V_{g2} = +1.0\text{ V}$  (Tx enabled);  $V_{g1}$ ,  $V_{g2} = 0\text{ V}$  (Tx disabled)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Amplifier A1 Current (pins 4, 9)	- -	48 2.4	80 6	mA	Tx enabled Tx disabled
Amplifier A2 Current (pins 21, 24)	- -	77 3.7	120 9	mA	Tx enabled Tx disabled
Attenuator Current (pin 2)	-	9	15	mA	
Total Power Consumption	- -	0.67 75	1.08 150	W mW	Tx enabled Tx disabled

Table 5: AC Electrical Specifications

$T_A=25^{\circ}\text{C}$ ;  $V_{DD}$ ,  $V_{ATTN}$ ,  $V_{CMOS} = +5.0\text{ VDC}$ ;  $V_{g1}$ ,  $V_{g2} = +1.0\text{ V}$  (Tx enabled);  $V_{g1}$ ,  $V_{g2} = 0\text{ V}$  (Tx disabled)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Gain (10 MHz)	27.5	29.3	30.5	dB	0 dB attenuation setting
Gain Flatness	- -	0.75 1.5	- -	dB	5 to 42 MHz 5 to 65 MHz
Gain Variation over Temperature	-	-0.006	-	dB/°C	
Attenuation Steps					
1 dB	0.65	0.83	1.00	dB	Monotonic
2 dB	1.6	1.70	2.05		
4 dB	3.6	3.75	4.0		
8 dB	7.5	7.75	8.0		
16 dB	15.0	15.40	15.8		
32 dB	30.2	30.75	31.3		
Maximum Attenuation	58.6	60.3	-	dB	
2 <sup>nd</sup> Harmonic Distortion Level (10 MHz)	-	-75	-53	dBc	+60 dBmV into 75 Ohms
3 <sup>rd</sup> Harmonic Distortion Level (10 MHz)	-	-60	-53	dBc	+60 dBmV into 75 Ohms
3 <sup>rd</sup> Order Output Intercept	78	-	-	dBmV	
1 dB Gain Compression Point	-	68.5	-	dBmV	
Noise Figure	-	3.0	4.0	dB	Includes input balun loss

Note: As measured in ANADIGICS test fixture

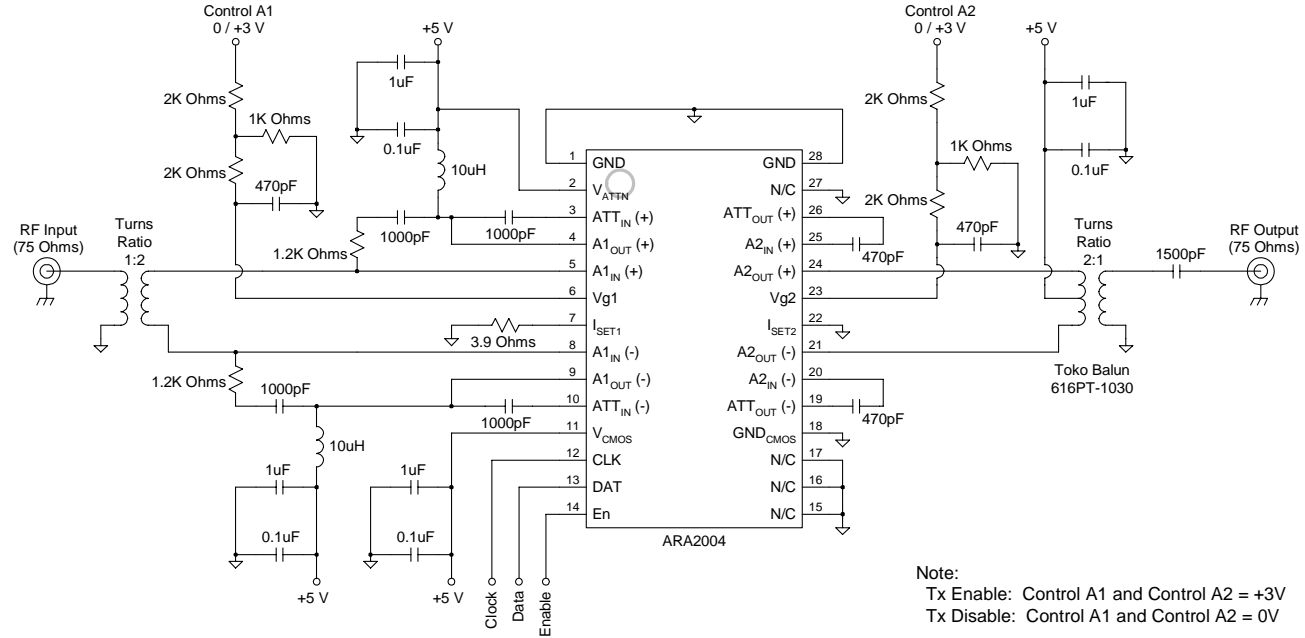
## continued: AC Electrical Specifications

$T_A=25^{\circ}\text{C}$ ;  $V_{DD}$ ,  $V_{ATTN}$ ,  $V_{CMOS} = +5.0\text{ VDC}$ ;  $V_{g1}$ ,  $V_{g2} = +1.0\text{ V}$  (Tx enabled);  $V_{g1}$ ,  $V_{g2} = 0\text{ V}$  (Tx disabled)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Output Noise Power Active / No Signal / Min. Atten. Set. Active / No Signal / Max. Atten. Set.	- -	- -	-38.5 -53.8	dBmV	Any 160 kHz bandwidth from 5 to 42 MHz
Isolation (45 MHz) in Tx disable mode	-	65	-	dB	Difference in output signal between Tx enable and Tx disable
Differential Input Impedance	-	300	-	Ohms	between pins 5 and 8 (Tx enabled)
Input Impedance	-	75	-	Ohms	with transformer (Tx enabled)
Input Return Loss (75 Ohm characteristic impedance)	- -	-20 -5	-12 -	dB	Tx enabled Tx disabled
Differential Output Impedance	-	300	-	Ohms	between pins 21 and 24
Output Impedance	-	75	-	Ohms	with transformer
Output Return Loss (75 Ohm characteristic impedance)	- -	-17 -15	-12 -10	dB	Tx enabled Tx disabled
Output Voltage Transient Tx enable / Tx disable	- -	- 4	100 7	mVp-p	0 dB attenuator setting 24 dB attenuator setting

Note: As measured in ANADIGICS test fixture

Figure 4: Test Circuit



Note:  
Tx Enable: Control A1 and Control A2 = +3V  
Tx Disable: Control A1 and Control A2 = 0V

PERFORMANCE DATA

Figure 5: Attenuation Level vs Control Word

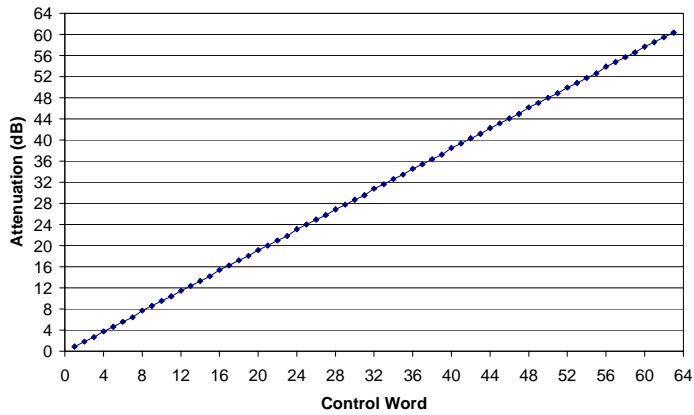


Figure 6: Gain & Noise Figure vs Frequency

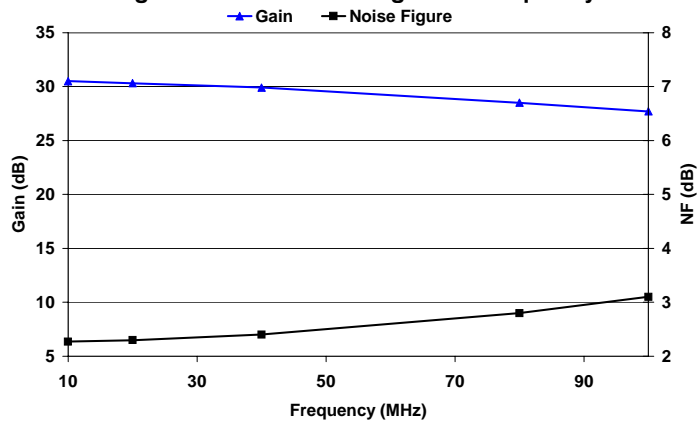


Figure 7: Gain & Noise Figure vs V<sub>DD</sub>

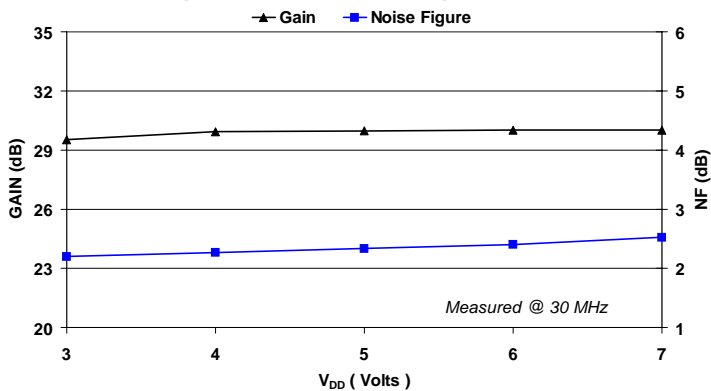




Figure 8: Gain & Noise Figure vs Temperature

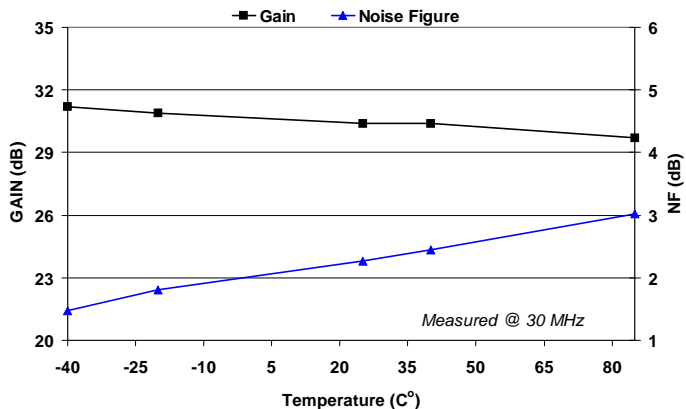


Figure 9: Harmonic Distortion vs V<sub>DD</sub>

P<sub>OUT</sub> = 58dBmV

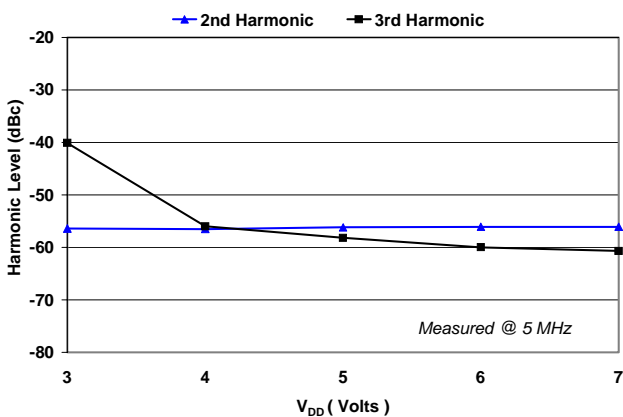
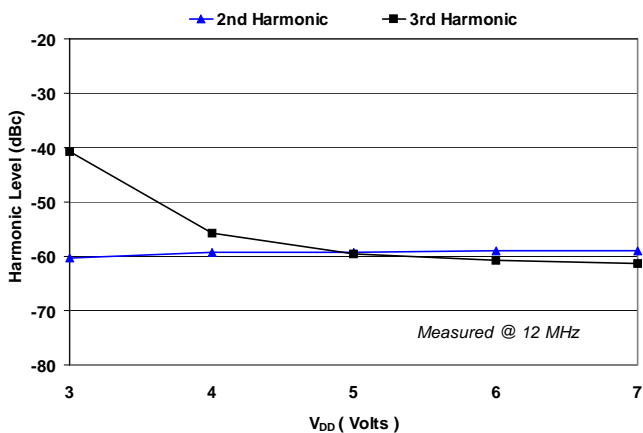
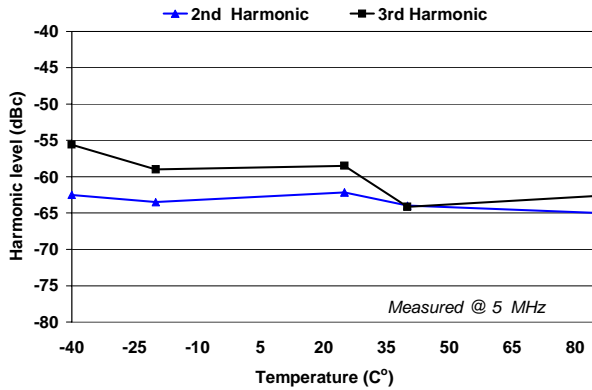


Figure 10: Harmonic Distortion vs V<sub>DD</sub>

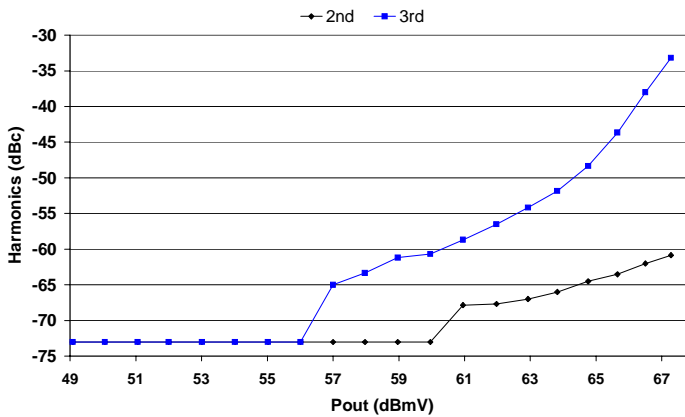
P<sub>OUT</sub> = 58dBmV



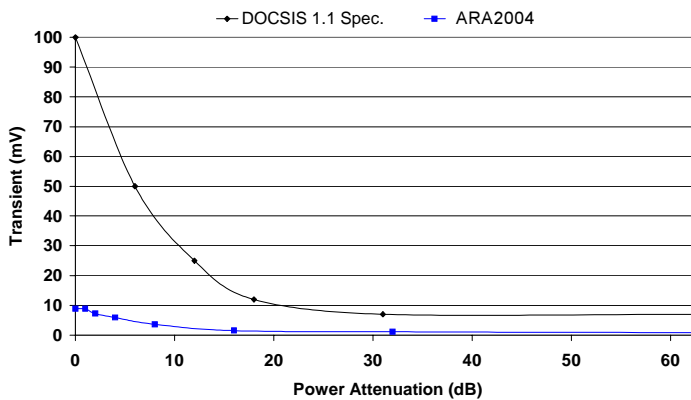
**Figure 11: Harmonic Distortion vs Temperature**  
 POUT = 58dBmV



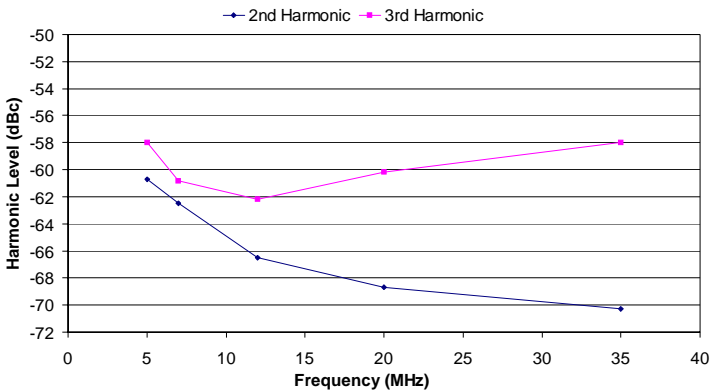
**Figure 12: Harmonic Distortion vs Power Out**



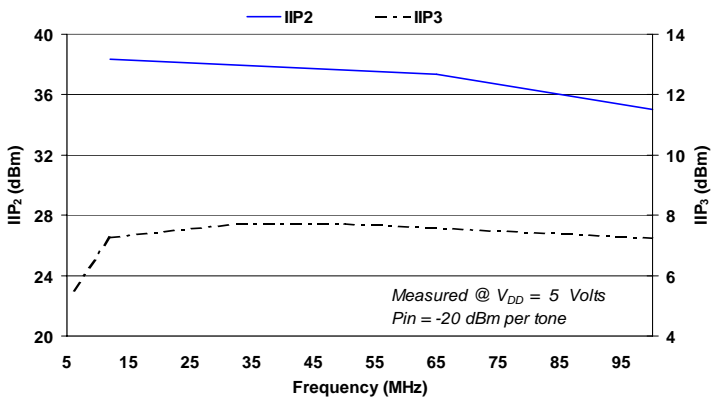
**Figure 13: Transients vs Attenuation**  
 POUT = 55dBmV at 0dB attenuation



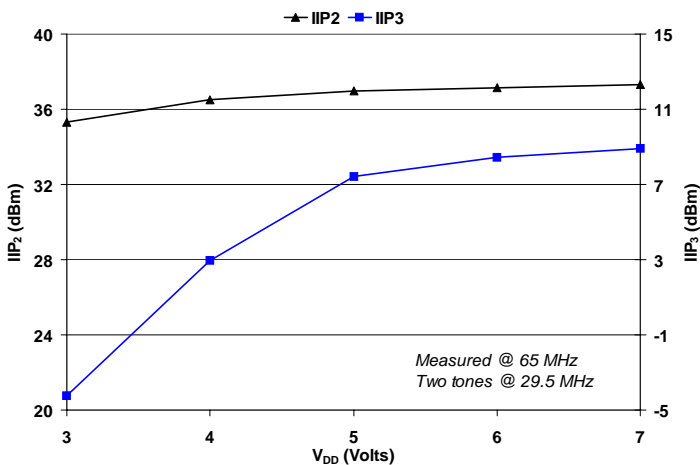
**Figure 14: Harmonic Performance over Frequency P<sub>OUT</sub> = +62dBmV**



**Figure 15: IIP<sub>2</sub> & IIP<sub>3</sub> vs Frequency**



**Figure 16: IIP<sub>2</sub> & IIP<sub>3</sub> vs V<sub>DD</sub>**



**LOGIC PROGRAMMING**

**Programming Instructions**

The programming word is set through an 8 bit shift register via the data, clock and enable lines. The data is entered in order with the most significant bit (MSB) first and the least significant bit (LSB) last.

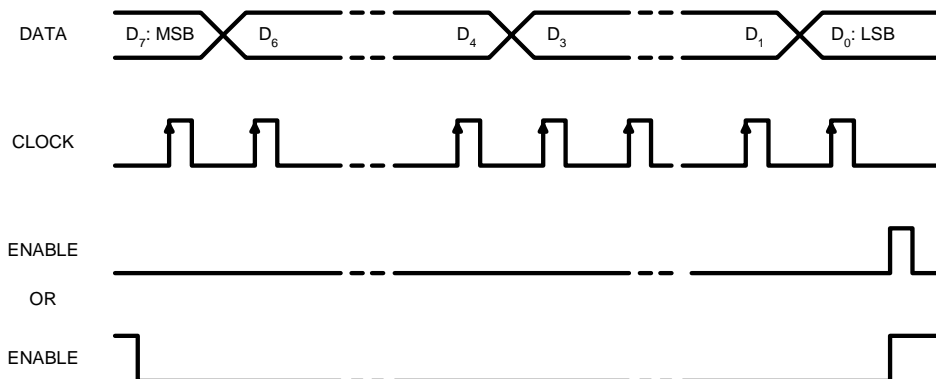
The enable line must be low for the duration of the data entry, then set high to latch the shift register. The rising edge of the clock pulse shifts each data value into the register.

**Table 6: Programming Word**

DATA BIT	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
Value	P7	P6	P5	P4	P3	P2	P1	P0

**Table 7: Data Description**

VALUE	FUNCTION (1 = on, 0 = bypass)
P7	N/A
P6	N/A
P5	32 dB Attenuator Bit
P4	16 dB Attenuator Bit
P3	8 dB Attenuator Bit
P2	4 dB Attenuator Bit
P1	2 dB Attenuator Bit
P0	1 dB Attenuator Bit



**Figure 17: Serial Data Input Timing**

## APPLICATION INFORMATION

### Transmit Enable / Disable

The ARA2004 includes two amplification stages that each can be shut down through external control pins Vg1 and Vg2 (pins 6 and 23, respectively.) By applying a slightly positive bias of typically +1.0 Volts, the amplifier is enabled. In order to disable the amplifier, the control pin needs to be pulled to ground.

A practical way to implement the necessary control is to use bias resistor networks similar to those shown in the test circuit schematic (Figure 4.) Each network includes a resistor shunted to ground that serves as a pull-down to disable the amplifier when no control voltage is applied. When a positive voltage is applied, the network acts as a voltage divider that presents the required +1.0 Volts to enable the amplifier. By selecting different resistor values for the voltage divider, the network can accommodate different control voltage inputs.

The Vg1 and Vg2 pins may be connected together directly, and controlled through a single resistor network from a common control voltage.

### Amplifier Bias Current

The ISET pins (7 and 22) set the bias current for the amplification stages. Grounding these pins results in the maximum possible current. By placing a resistor from the pin to ground, the current can be reduced. The recommended bias conditions use the configuration shown in the test circuit schematic in Figure 4.

### Thermal Layout Considerations

The device package for the ARA2004 features an exposed paddle on the bottom of the package body. Use of the paddle is an integral part of the device design. Soldering this paddle to the ground plane of the PC board will ensure the lowest possible thermal resistance for the device, and will result in the longest MTF (mean time to failure.)

A PC board layout that optimizes the benefits of the paddle is shown in Figure 18. The via holes located under the body of the device must be plated through to a ground plane layer of metal, in order to provide a sufficient heat sink. The recommended solder mask outline is shown in Figure 19.

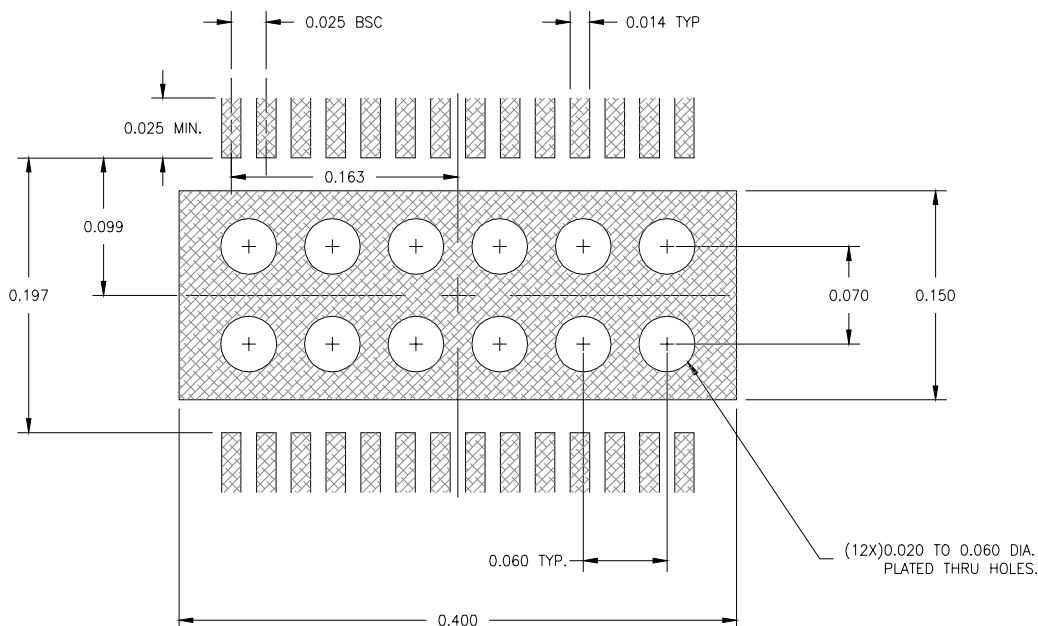
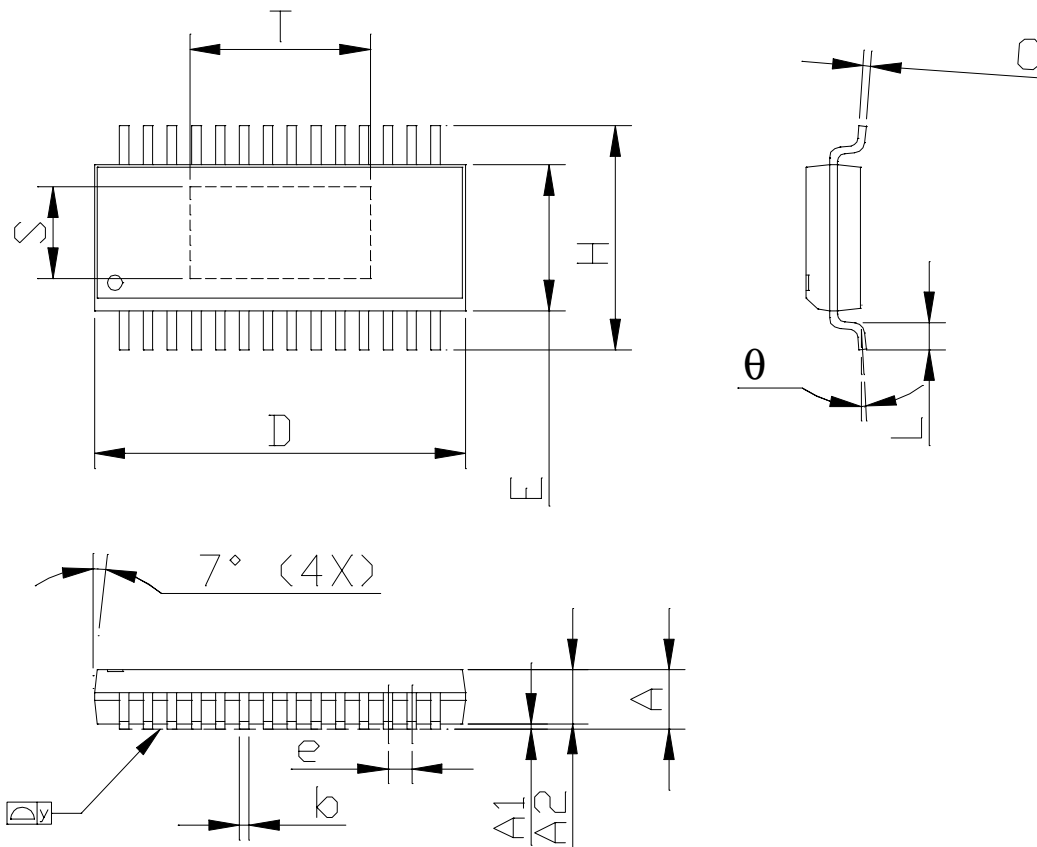


Figure 18: PC Board Layout



PACKAGE OUTLINE



- NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS
  2. TOLERANCE 0.004in.[0.10 mm] UNLESS OTHERWISE SPECIFIED
  3. CONTROLLING DIMENSION ARE INCHES.
  4. REF. - MO-137

SYMBOLS	DIMENSIONS IN INCHES		DIMENSIONS IN MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.057	0.061	1.45	1.55
A1	0.000	0.004	0.00	0.10
A2	0.057 (NOMINAL)		1.45 (NOMINAL)	
b	0.008	0.012	0.20	0.30
C	0.007	0.010	0.18	0.25
D	0.386	0.394	9.80	10.00
E	0.150	0.157	3.81	4.00
H	0.228	0.244	5.80	6.20
e	0.025 BSC		.64 BSC	
L	0.016	0.050	0.40	1.27
y	---	0.004	---	0.10
theta	0°	8°	0°	8°
T	---	0.190	---	4.82
S	---	0.096	---	2.43

98000-031

Figure 20: S23 Package Outline - 28 Pin SSOP with Exposed Paddle

### COMPONENT PACKAGING

Volume quantities of the ARA2004 are supplied on tape and reel. Each reel holds 3,500 pieces. Smaller quantities are available in plastic tubes of 50 pieces.

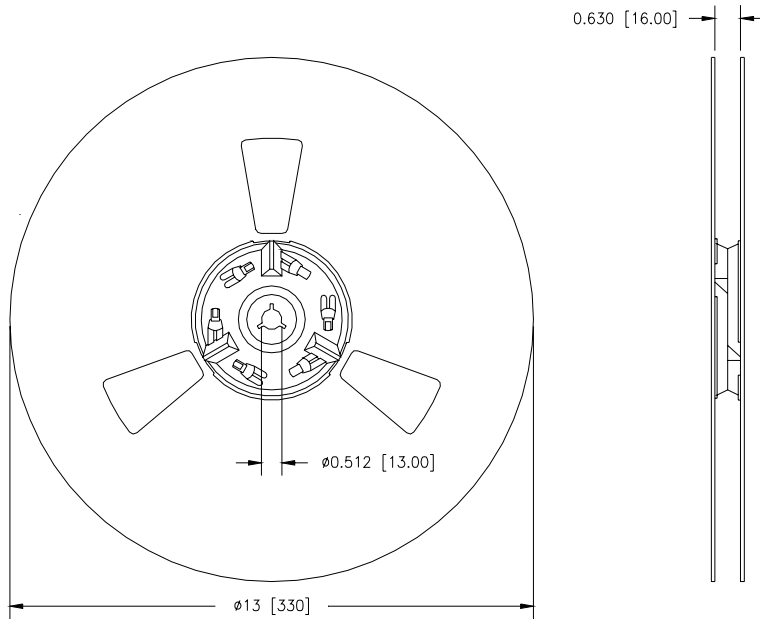


Figure 21: Reel Dimensions

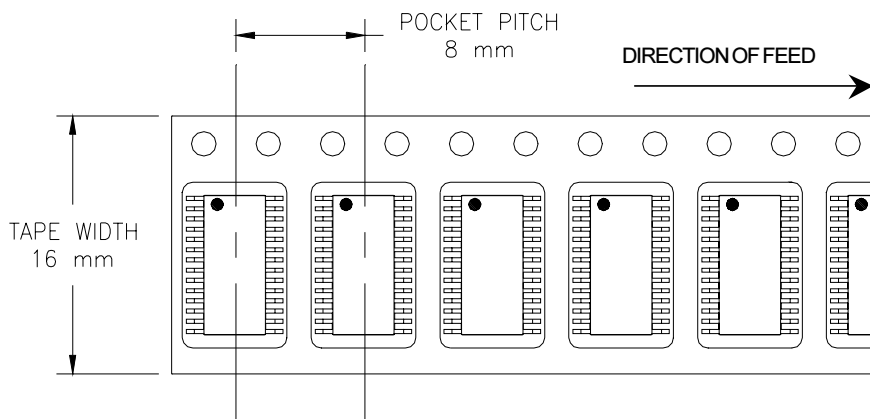


Figure 22: Tape Dimensions



NOTES



NOTES

**ORDERING INFORMATION**

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ARA2004S23P1	-40 to 85 °C	28 Pin SSOP with Exposed Paddle	3,500 piece tape and reel
ARA2004S23P0	-40 to 85 °C	28 Pin SSOP with Exposed Paddle	Plastic tubes (50 pieces per tube)

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