

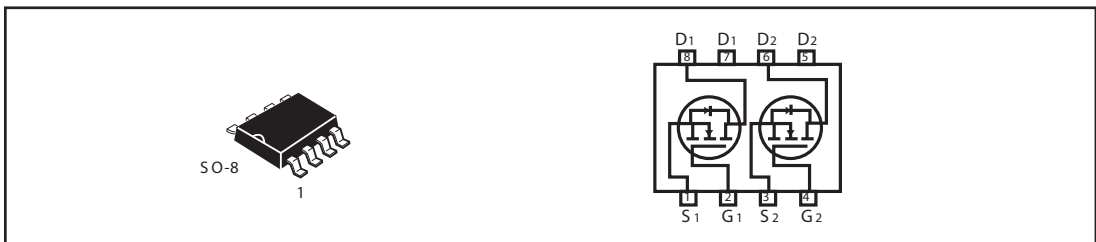


## Dual N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> ( mΩ ) Max
20V	6A	30 @ V <sub>GS</sub> = 4.5V
		32 @ V <sub>GS</sub> = 4.0V
		40 @ V <sub>GS</sub> = 2.7V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	±12	V
Drain Current-Continuous <sup>a</sup> @ T <sub>J</sub> =125 °C -Pulsed <sup>b</sup> (300us Pulse Width)	I <sub>D</sub>	6.0	A
	I <sub>DM</sub>	35	A
Drain-Source Diode Forward Current <sup>a</sup>	I <sub>S</sub>	1.7	A
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	2	W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient <sup>a</sup>	R θ <sub>JA</sub>	62.5	°C/W
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## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250uA	20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V			1	uA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±8V, V <sub>DS</sub> = 0V			±100	nA
<b>ON CHARACTERISTICS<sup>b</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250uA		1.1		V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 6.0A V <sub>GS</sub> = 4.0V, I <sub>D</sub> = 6.0A V <sub>GS</sub> = 2.7V, I <sub>D</sub> = 5.2A		28 29 36	30 32 40	m ohm
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> = 5V, V <sub>GS</sub> = 4.5V	20			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 6.0A		17		S
<b>DYNAMIC CHARACTERISTICS<sup>c</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 8V, V <sub>GS</sub> = 0V f = 1.0MHz		710		pF
Output Capacitance	C <sub>OSS</sub>			300		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			80		pF
<b>SWITCHING CHARACTERISTICS<sup>c</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> = 10V, I <sub>D</sub> = 1A, V <sub>GEN</sub> = 4.5V, R <sub>L</sub> = 10 ohm R <sub>GEN</sub> = 6 ohm		10	20	ns
Rise Time	t <sub>r</sub>			15	30	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			26	50	ns
Fall Time	t <sub>f</sub>			20	40	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 6A, V <sub>GS</sub> = 4.5V		12	15	nC
Gate-Source Charge	Q <sub>gs</sub>			4		nC
Gate-Drain Charge	Q <sub>gd</sub>			2		nC

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## ELECTRICAL CHARACTERISTICS ( $T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>b</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_s = 1.7A$		0.72	1.2	V

### Notes

- a. Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$ .
- b. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- c. Guaranteed by design, not subject to production testing.

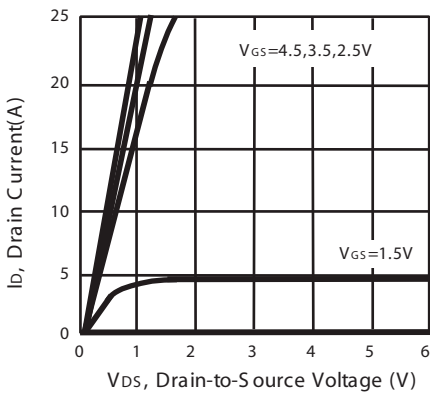


Figure 1. Output Characteristics

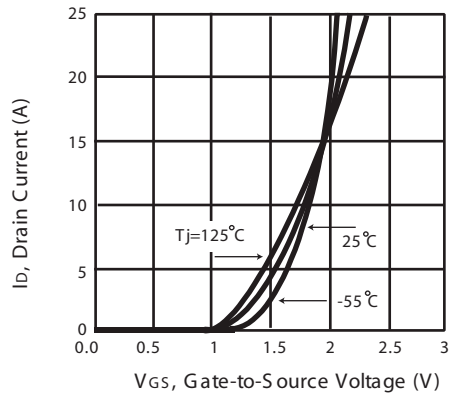


Figure 2. Transfer Characteristics

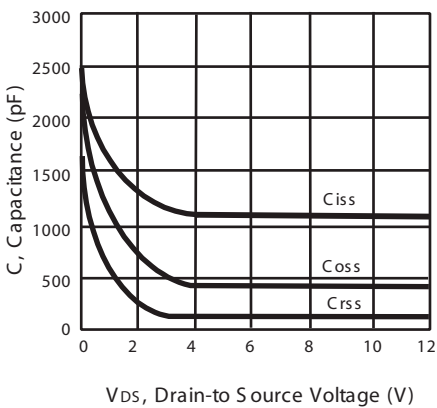


Figure 3. Capacitance

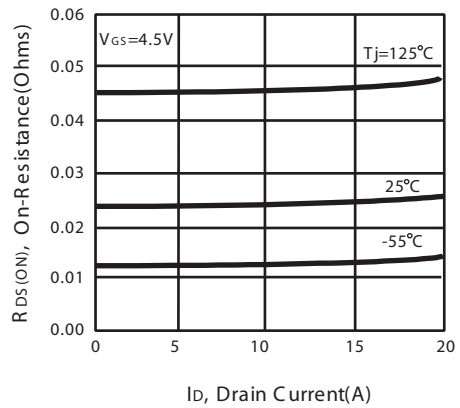


Figure 4. On-Resistance Variation with Drain Current and Temperature

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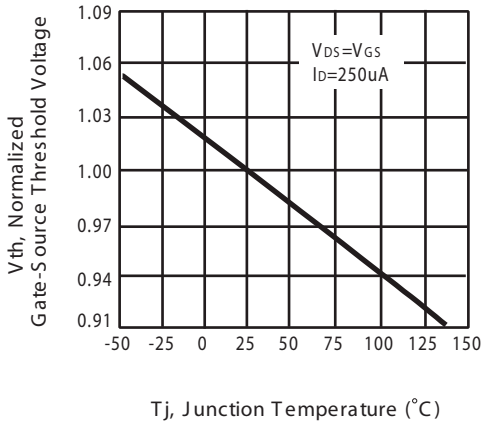


Figure 5. Gate Threshold Variation with Temperature

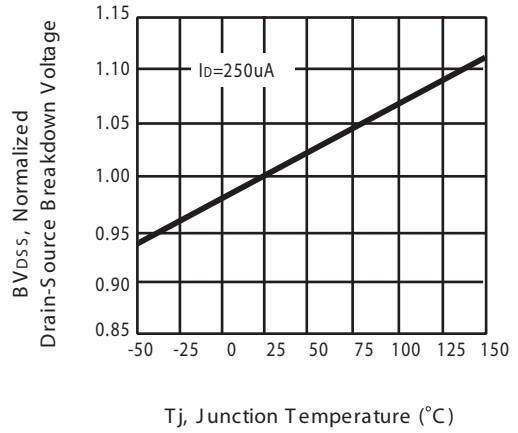


Figure 6. Breakdown Voltage Variation with Temperature

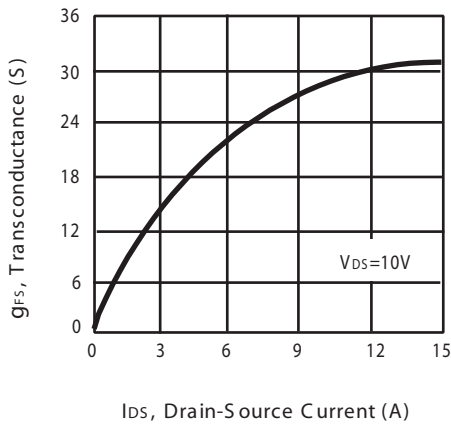


Figure 7. Transconductance Variation with Drain Current

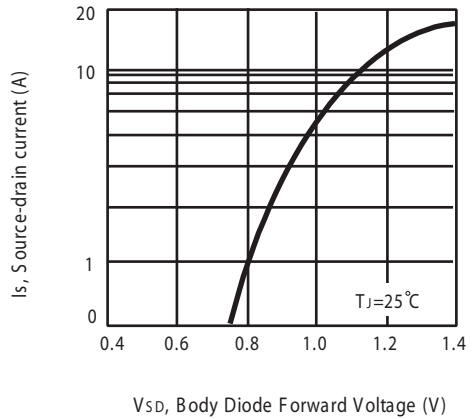


Figure 8. Body Diode Forward Voltage Variation with Source Current

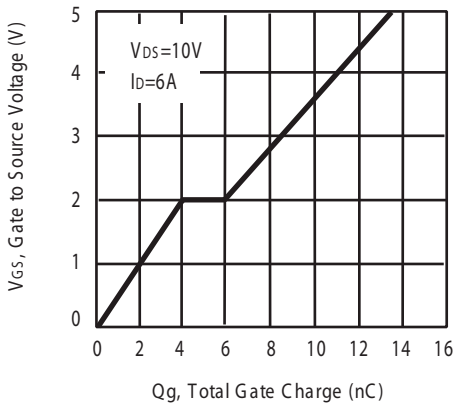


Figure 9. Gate Charge

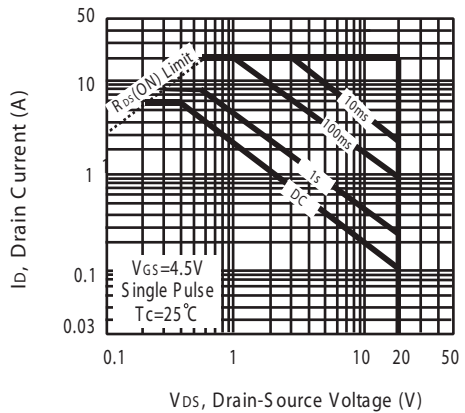


Figure 10. Maximum Safe Operating Area

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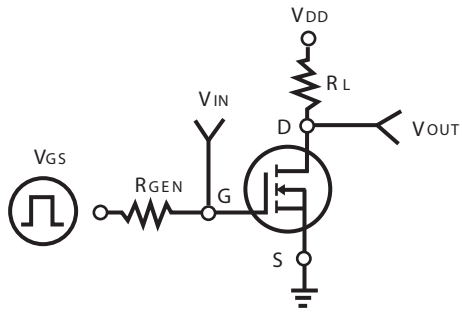


Figure 11. Switching Test Circuit

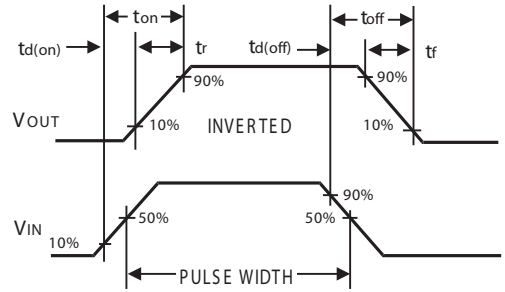


Figure 12. Switching Waveforms

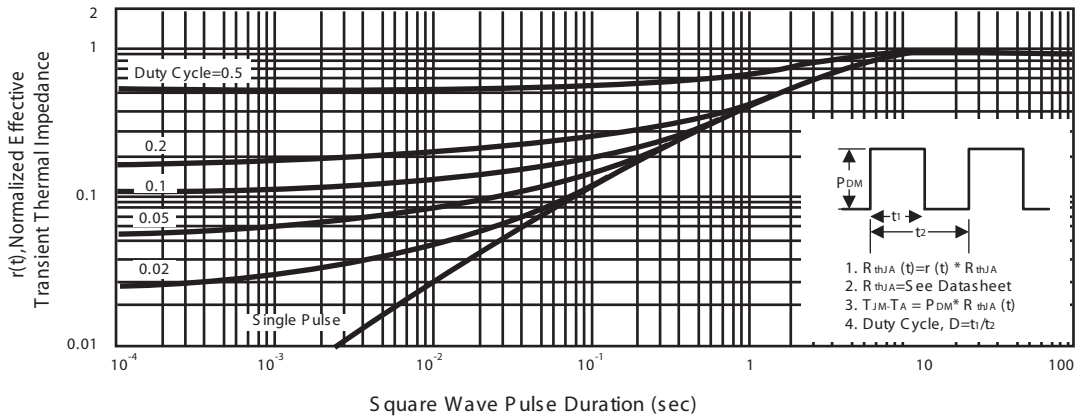


Figure 13. Normalized Thermal Transient Impedance Curve