PCI 9030 Data Book

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Version 1.1

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PREFACE

The information contained in this document is subject to change without notice. Although an effort has been made to keep the information accurate, there may be misleading or even incorrect statements made herein.

The following is a list of additional documentation to provide the reader with more information about the PCI 9030 and related subjects:

- *PCI Local Bus Specification, Revision 2.2*, December 18, 1998
  PCI Special Interest Group (PCI SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 800 433-5177 (domestic only) or 503 693-6232, Fax: 503 693-8344, http://www.pcisig.com
- *PCI Hot-Plug Specification, Revision 1.0*
  PCI Special Interest Group (PCI SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 800 433-5177 (domestic only) or 503 693-6232, Fax: 503 693-8344, http://www.pcisig.com
- *PCI Bus Power Management Interface Specification, Revision 1.1*, December 18, 1998
  PCI Special Interest Group (PCI SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 800 433-5177 (domestic only) or 503 693-6232, Fax: 503 693-8344, http://www.pcisig.com
- *PICMG 2.1, R1.0, CompactPCI Hot Swap Specification*, August 3, 1998
  PCI Industrial Computer Manufacturers Group (PICMG)
  c/o Virtual Inc., 401 Edgewater Place, Suite 500, Wakefield, MA 01880, USA
  Tel: 781 224-1100, Fax: 781 224-1239, http://www.picmg.org

Revision History

Date	Revision	Comment
3/1999	New Release	New Release PCI 9030 Preliminary Data Book, Version 0.9.
8/1999	0.90	Update.
10/1999	0.90	Initial Release Red Book.
10/1999	0.91	Update.
11/1999	0.92	Update.
12/1999	0.93	Initial Release Blue Book.
4/2000	1.0	Production Release.
1/31/2001	1.1	Incorporate 1/31/2001 Addendum changes, including past design notes.

PCI 9030

PCI SMARTarget™ I/O Accelerator

January 2001
Version 1.1

CompactPCI Hot Swap Ready
for Adapters and Embedded Systems

1 INTRODUCTION

1.1 FEATURES

- *PCI Local Bus Specification* v2.2-compliant 32-bit, 33 MHz Bus Target Interface Device enabling PCI Burst Transfers up to 132 MB/s
- *PCI Bus Power Management Interface Specification* v1.1 compliant
- *PCI Local Bus Specification* v2.2 Vital Product Data (VPD) configuration support
- *PICMG 2.1, CompactPCI® Hot Swap Specification,* Revision 1.0® Hot Swap *Ready* compliant
- PCI Target Programmable Burst Management
- PCI Target Read Ahead mode
- PCI Target Delayed Read mode
- PCI Target Delayed Write mode
- Programmable Interrupt Generator/Controller
- Two programmable FIFOs for zero wait state burst operation
- Flexible Local Bus runs up to 60 MHz
- 3.3/5V tolerant PCI and Local signaling supports Universal PCI Adapter designs
- Flexible Local Bus provides 32-bit Multiplexed or Non-Multiplexed Protocol for 8-, 16-, or 32-bit Peripheral and Memory devices
- Serial EEPROM interface
- Nine programmable General Purpose I/O (GPIOs)
- Five programmable Local Address spaces
- Four programmable independent chip selects
- Programmable Local Bus wait states
- Programmable Local Read prefetch mechanism
- Local Bus can run asynchronously to the PCI Bus
- Two programmable Local-to-PCI interrupts
- Endian Byte Swapping
- 3.3V Core, Low-Power CMOS in 176-pin PQFP or 180-pin µBGA
- Industrial Temp Range operation

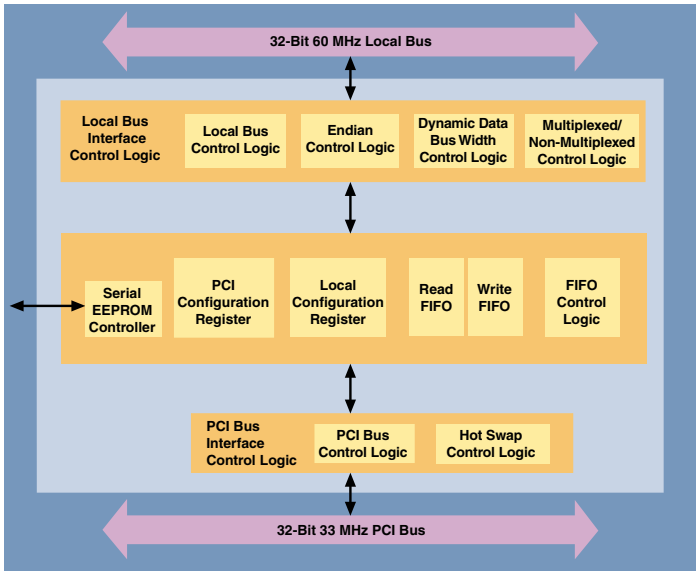


Figure 1-1. PCI 9030 Internal Block Diagram

1.2 COMPANY AND PRODUCT BACKGROUND

PLX Technology, Inc. is the world leader in PCI-to-Local Bus I/O accelerator chips, which are used in a wide variety of PCI applications. Customer applications include PCI add-in boards in PC workstations and servers, embedded PCI communication systems (such as routers and switches), and industrial PCI implementations (such as CompactPCI, PMC, and Passive Backplane PCI).

PLX Technology, Inc. is an active member of industry-standard committees, including the PCI SIG®, I_2O SIG®, and PICMG, and maintains active developer technology and cross-marketing partnerships with industry leaders, such as Intel, IBM, Hewlett-Packard, Motorola, WindRiver, and others.

Focused on providing complete solutions for PCI implementations, PLX provides design assistance to customers in the form of Reference Design and Software Development kits. Depending upon the application, these kits may include reference boards, API libraries, software debug tools, and sample device drivers, enabling customers to quickly bring new designs to production. New tools, application notes, FAQs, and information updates are frequently being added to the PLX website (http://www.plxtech.com) for customer convenience. PLX's expertise and total solutions for the PCI interface allow customers to focus on adding value in their designs without worrying about the complexities of implementing PCI and CompactPCI.

1.2.1 PCI 9030 SMARTarget I/O Accelerator

The PCI 9030, a 32-bit, 33-MHz PCI Bus Target Interface chip with SMARTarget™ Technology, is the most advanced general-purpose PCI Target device available. It offers a complete *PCI Local Bus Specification* (v2.2) implementation, enabling Burst transfers up to 132 MB/s, and is the industry's first CompactPCI Hot Swap Ready Target device. The PCI 9030 is the perfect solution for migrating legacy designs to PCI while adding new features that enhance next generation Target designs. The PCI 9030 SMARTarget I/O Accelerator brings PLX's industry-leading experience in the PCI design world to the customer in a way that is simple and convenient to use.

1.2.2 SMARTarget Technology

Many PCI chip and core designs implement only basic *PCI Local Bus Specification* v2.2 bus interface signaling, leaving the difficult performance and compatibility issues to the designer. The PCI 9030, with SMARTarget Technology, incorporates features which simplify design implementation. These features go far beyond the minimum to provide the highest possible design performance and flexibility.

SMARTarget Technology performance features:

- PCI v2.2 compliant, 32-bit, 33 MHz Target Interface, enabling PCI Burst Transfers up to 132 MB/s
- Up to 60 MHz Local Bus Operation, Enabling Burst Transfers up to 240 MB/s
- PCI Target Read Ahead mode
- PCI Target Programmable Burst
- PCI Target Delayed Write
- Posted Memory Writes

SMARTarget Technology flexibility features:

- Programmable 32-bit Local Bus operates up to 60 MHz
- Supports five PCI-to-Local Address spaces
- Nine Programmable General Purpose I/Os (GPIOs)
- Four Programmable Chip Selects
- CompactPCI Hot Swap Ready
- Big/Little Endian Byte Conversion
- Interrupt Generator/Controller
- PCI v2.2 Vital Product Data (VPD)
- *PCI Bus Power Management Interface Specification* v1.1
- 3.3/5V Tolerant PCI Signaling
- 3.3V CMOS Device in 176-PQFP or 180-pin µBGA
- Programmable Read and Write Strobe Timing on the Local Bus

1.2.3 PCI 9030 Applications

The PCI 9030 can be used in a wide variety of networking, telecom, imaging, industrial and storage applications. The PCI 9030 simplifies legacy design migration to PCI by providing a convenient off-the-shelf solution that enables prototypes to be operational in a short time period.

1.2.3.1 High-Performance PCI Target Interface

The PCI 9030's built-in SMARTarget performance features (such as 3.3/5V tolerant I/O buffers and Local Bus operation up to 60 MHz), enable designers to connect a wide variety of memory and I/O devices. With SMARTarget in action, PCI Target Adapter designs have never been simpler to implement. Figure 1-2 illustrates a typical PCI Target adapter card.

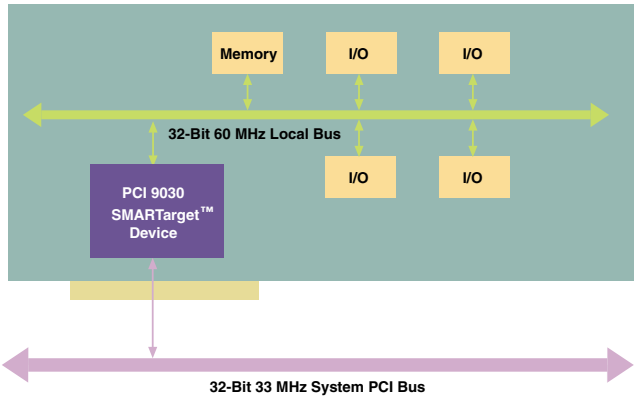


Figure 1-2. Typical PCI Target Adapter Card

1.2.3.2 High Performance CompactPCI Adapter Designs

Built upon substantial CompactPCI experience, the PLX PCI 9030 is the industry's first CompactPCI Hot Swap *Ready* Target device. This allows CompactPCI I/O board designs to be compatible with both traditional CompactPCI and new Hot Swap system designs. Figure 1-3 illustrates a typical CompactPCI adapter card.

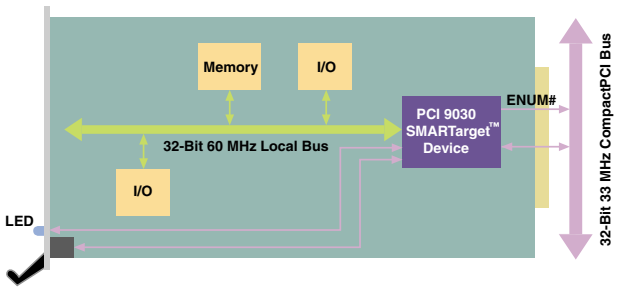


Figure 1-3. High-Performance CompactPCI Adapter Card

1.2.3.2.1 Hot Swap Ready

Hot Swap Ready performance features include:

- *PCI Local Bus Specification* v2.2
- Tolerant of Vcc from early power
- Tolerant of asynchronous reset
- Tolerant of precharge voltage
- Limited I/O pin leakage at precharge voltage
- Incorporates the Hot Swap Control/Status register (HS_CSR)
- Incorporates an Extended Capability Pointer (ECP) mechanism
- Incorporates added resources for software control of ENUM#, the ejector switch, and the status LED, which indicates insertion and removal status to the user
- Precharge 10K ohm resistor network and BIAS voltage internal to the PCI 9030
- Early power support internal to the PCI 9030

1.2.3.3 PMC Adapter Cards

In the real estate-conscious world of PMC, PC-MIP, and PCMCIA PC cards, the PCI 9030 offers an attractive packaging option with the dime-size 180-pin µBGA. SMARTarget flexibility features, such as GPIOs and Programmable Chip selects, save additional valuable board space. The PCI 9030 enables a whole new generation of mini form factor PCI cards.

Figure 1-4 illustrates a typical PMC adapter card and Figure 1-5 illustrates a typical PCMCIA PC card.

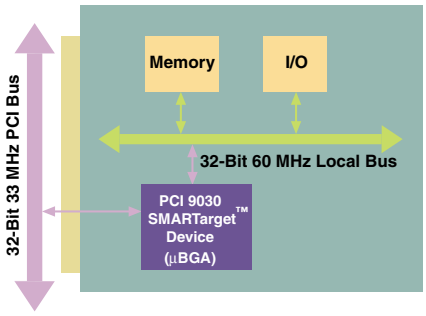


Figure 1-4. Typical PMC Adapter Card

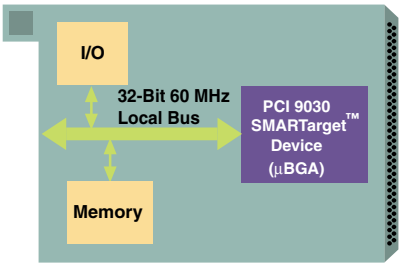


Figure 1-5. Typical PCMCIA PC Card

1.2.4 PCI 9030 SMARTarget Features

1.2.4.1 Performance Features

PCI v2.2 Compliant. This 32-bit, 33 MHz Target Interface Chip enables PCI Burst Transfers up to 132 MB/s.

Up to 60 MHz Local Bus Operation. Enables burst transfers up to 240 MB/s.

PCI Target Read Ahead Mode. Prefetches a programmable amount of data from the Local Bus. This data can then be burst-transferred onto the PCI bus from the PCI 9030 internal PCI Target Read FIFO. The prefetch size can be programmed to match the PCI master burst length or can be used in the PCI Target Read Ahead mode data. This feature also allows for increased bandwidth and reduced read latency.

PCI Target Programmable Burst. The PCI 9030 may be programmed for several burst lengths, including unlimited burst. This allows for maximum transfer rates on both the PCI and Local Buses.

PCI Target Delayed Write Mode. The PCI Target Write data accumulates in the PCI Target Write FIFO to allow uninterrupted burst transactions on the Local Bus. This allows for a higher throughput for conditions in which the PCI Clock frequency is slower than the Local Clock frequency.

Posted Memory Writes. A PCI Memory write is posted to the PCI 9030 for later transfer to the Local Bus. This allows for maximum PCI performance and avoids potential deadlock situations.

1.2.4.2 Flexibility Features

Programmable Local Bus. Operates up to 60 MHz and supports both Multiplexed and Non-Multiplexed 32-bit address/data protocol, and dynamic Local Bus width control allowing slave accesses to 8-,16- or 32-bit devices.

PCI-to-Local Address Spaces. Supports five PCI-to-Local Address spaces. Spaces 0, 1, 2, 3, and the Expansion ROM space all allow a PCI Bus Master to access the Local Memory spaces with individually programmable wait states, bus width, and burst capabilities.

GPIOs. The PCI 9030 has nine programmable general purpose I/O pins, which may be used for generic interface purposes.

Four Programmable Chip Selects. Eliminates decode logic, which improves performance.

CompactPCI Hot Swap Ready. Compliant with *PICMG 2.1 R1.0*.

Big/Little Endian Conversion. Supports automatic on-the-fly Big Endian and Little Endian conversion for all operations and data widths.

Interrupt Generator/Controller. Can assert PCI interrupts from external and internal sources.

VPD Support. Fully supports the PCI v2.2 Vital Product Data (VPD) extension, including the New Capabilities Structure. Provides an alternate access method for user- or system-defined parameters or configuration data.

PCI Power Management. Supports both the D_0 and D_{3hot} power states.

Two Programmable FIFOs for Zero Wait State Burst Operation. The following table describes the FIFO depth.

Table 1-1. FIFO Depth

FIFO	Length
PCI Target Read	16 Lwords
PCI Target Write	32 Lwords

3.3/5V Tolerant PCI Signaling. Enables Universal PCI Adapters.

3.3V CMOS Device in 176-pin PQFP or 180-pin μBGA.

1.2.4.3 Additional Features

5 Volt Tolerant Operation. The PCI 9030 requires a 3.3V supply. It provides 3.3V signaling with 5V I/O tolerance on both the PCI and Local Buses.

Serial EEPROM Interface. Contains a serial EEPROM interface that offers the option of loading configuration information from an EEPROM device.

Clocks. The Local Bus interface runs from a Local Bus clock, which runs asynchronously to the PCI clock. In addition, the PCI 9030 provides a PCI Buffered clock, which can be used as a Local Bus clock.

RST# Timing. Supports response to first configuration accesses after de-assertion of PCI RST# in less than 2^{25} clocks.

Subsystem and Subsystem Vendor IDs. Contains Subsystem ID and Subsystem Vendor ID in the PCI Configuration register space, in addition to Device and Vendor IDs. The PCI 9030 also contains a permanent Vendor ID (10B5h) and Device ID (9030h).

Silicon Revision ID. Contains the PCI 9030 Silicon Revision ID, which is programmable by way of the serial EEPROM.

1.2.5 PCI 9030 Data Assignment Convention

The following table describes the PCI 9030 data assignment convention.

Table 1-2. PCI 9030 Data Assignment Convention

Data Width	PCI 9030 Convention
1 byte (8 bits)	Byte
2 bytes (16 bits)	Word
4 bytes (32 bits)	Lword

1.2.6 PLX Chip Compatibility

1.2.6.1 Pin Compatibility

The PCI 9030 is ***not*** pin compatible with the PCI 9050, PCI 9052, PCI 9054, ***nor*** the PCI 9080.

1.2.6.2 Register Compatibility

All registers implemented in the PCI 9050 and 9052 are implemented in the PCI 9030. The PCI 9030 includes many new bit definitions and several new registers. Refer to Table 1-3 for details.

The PCI 9030 is ***not*** register-compatible with the PCI 9080 nor the PCI 9054.

1.2.7 PCI 9030, PCI 9050, and PCI 9052 Comparison

The following table compares the PCI 9030, PCI 9050, and PCI 9052.

Table 1-3. PCI 9030, PCI 9050, and PCI 9052 Comparison

Feature	PCI 9030	PCI 9050	PCI 9052
Pin Count and Type	176 PQFP/180 µBGA	160 PQFP	160 PQFP
Package Size	27 x 27 mm	31 x 31 mm	31 x 31 mm
Local Address Spaces	5	5	5
PCI Initiator Mode	No	No	No
Number of FIFOs	2	2	2
FIFO Depth—PCI Target Write	32 Lwords (128 bytes)	16 Lwords (64 bytes)	16 Lwords (64 bytes)
FIFO Depth—PCI Target Read	16 Lwords (64 bytes)	8 Lwords (32 bytes)	8 Lwords (32 bytes)
LLOCKo# Pin for Lock Cycles	Yes	Yes	Yes
WAITo# Pin for Wait State Generation	Yes	Yes	Yes
BCLKo (BCLKO) Pin; Buffered PCI Clock	Yes	Yes	Yes
ISA Bus Interface	No	No	Yes
Register Addresses	Identical to the PCI 9050 and PCI 9052, except the PCI 9030 contains additional registers related to added functionality	—	—
Big Endian ⇔ Little Endian Conversion	Yes	Yes	Yes
PCI Target Delayed Read Transactions	Yes	Yes	Yes
PCI Target Delayed Write Transactions	Yes	No	No
PCI Target Local Bus READY# Timeout	Yes	No	No
PCI Bus Power Management Interface v1.1	Yes	No	No
PCI Local Bus Specification v2.2 VPD Support	Yes	No	No
Programmable Prefetch Counter	Yes	Yes	Yes
Programmable Wait States	Yes	Yes	Yes
Programmable Ready Timeout	Yes	No	No
Programmable GPIOs	9	4	4
Additional Device and Vendor ID Registers	Yes	Yes	Yes
Core and Local Bus Vcc	3.3V	5V	5V
PCI Bus Vcc	3.3V	5V	5V
3.3V PCI Bus and Local Bus Signaling	Yes	No	No
5V Tolerant PCI Bus and Local Bus Signaling	Yes	Yes	Yes
Serial EEPROM Support	2K-, 4K-bit devices	1K-bit devices	1K-bit devices
Serial EEPROM Read Control	Reads allowed via VPD function (refer to Section 9) and CNTRL Register	Reads allowed via Serial EEPROM Control Register (CNTRL)	Reads allowed via Serial EEPROM Control Register (CNTRL)
PCI Target Read Ahead Mode	Yes	No	No
CompactPCI Hot Swap Capability	Ready	Capable	Capable

2 PCI AND LOCAL BUS

This section discusses PCI and Local Bus operation.

2.1 PCI BUS

2.1.1 PCI Bus Interface and Bus Cycles

The PCI 9030 is compliant with *PCI Local Bus Specification* v2.2. Refer to the specification for specific PCI Bus functions as a PCI Target Interface chip.

2.1.1.1 PCI Target Command Codes

As a Target, the PCI 9030 allows access to the PCI 9030 internal registers and the Local Bus, using the commands listed in Table 2-1.

All Read or Write accesses to the PCI 9030 can be Byte, Word, or Lword (32-bit data). All memory commands are aliased to basic memory commands. All PCI 9030 I/O accesses are decoded to an Lword boundary. Byte enables are used to determine which bytes are read or written. An I/O access with illegal byte enable combinations is terminated with a Target abort.

Table 2-1. PCI Target Command Codes

Command Type	Code (C/BE[3:0]#)
I/O Read	0010 (2h)
I/O Write	0011 (3h)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Configuration Read	1010 (Ah)
Configuration Write	1011 (Bh)

2.1.1.2 Wait States—PCI Bus

The PCI Bus Master throttles IRDY# and the PCI Bus Slave throttles TRDY# to assert PCI Bus wait state(s).

2.1.1.3 PCI Target Accesses to an 8- or 16-Bit Local Bus Device

Direct PCI access to an 8- or 16-bit Local Bus device results in the PCI Bus Lword being broken into multiple Local Bus transfers. For each 8-bit transfer, byte enables are encoded as in the i960C to provide Local Address bits LA[1:0]. For each 16-bit transfer, byte enables are encoded to provide BLE#, BHE# and LA1.

2.1.1.4 PCI Bus Little Endian Mode

The PCI Bus is a Little Endian bus (*that is*, the address is invariant and data is Lword-aligned to the lowermost byte lane).

Table 2-2. PCI Bus Little Endian Byte Lanes

Byte Number	Byte Lane
0	AD[7:0]
1	AD[15:8]
2	AD[23:16]
3	AD[31:24]

2.2 LOCAL BUS

2.2.1 Introduction

The Local Bus provides a data path between the PCI Bus and non-PCI devices, including memory devices and peripherals. The Local Bus is a 32-bit multiplexed or non-multiplexed bus, with bus memory regions that can be programmed for 8-, 16-, or 32-bit widths. The PCI 9030 Local Bus is signal-compatible with popular RISC and Bridge architecture, including the i960Cx, i960Jx, and PPC401 GF. In addition, the Local Bus can directly connect to Texas Instruments DSP devices (such as the TMS320C6202 and TMS320C54x).

The PCI 9030 is the Local Bus master. The PCI 9030 can transfer data between the Local Bus, internal registers and FIFOs. Burst lengths are not limited. The width of the bus depends upon the Local Address Space register setting. There are four address spaces and one default space (the expansion ROM that can be used as another address space). Each space contains a set of configuration registers that determine

all Local Bus characteristics when that space is accessed.

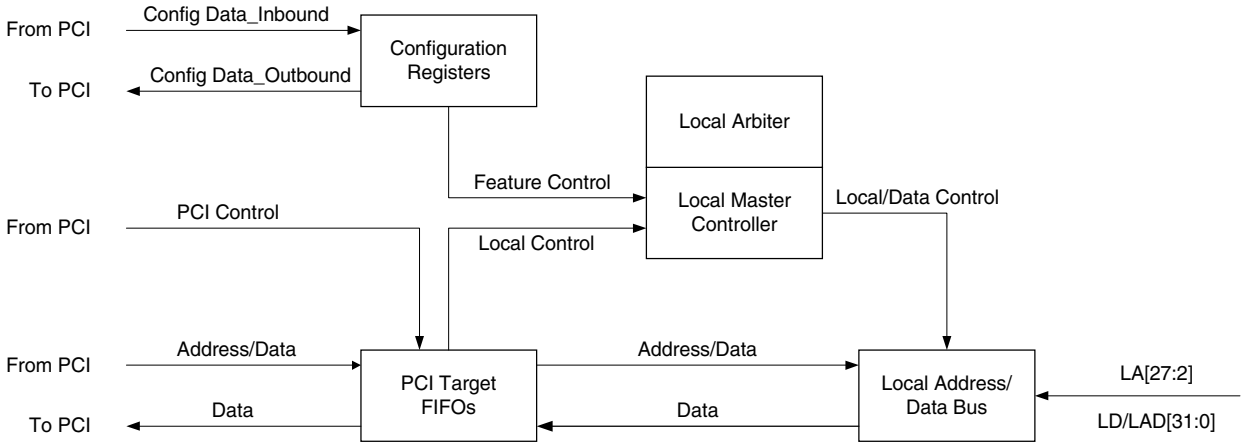


Figure 2-1. Local Bus Block Diagram

2.2.1.1 Transactions

Four types of transactions can occur on a Local Bus:

- Read
- Write
- Read Burst
- Write Burst

A Bus access is a transaction which is bounded by the assertion of ADS# at the beginning and de-assertion of BLAST# at the end. A Bus access consists of an address cycle followed by one or more data transfers. During each clock cycle of an access, the Local Bus is in one of four basic states defined in Section 2.2.1.2, “Basic Bus States.” A clock cycle consists of one period of the Local Bus clock.

2.2.1.2 Basic Bus States

The four basic bus states are idle, address, data/wait, and recovery. Once the Local Bus master owns the Bus and needs to start a bus access, the address state is entered, ADS# or ALE is asserted, and a valid address is presented on the address/data bus. Data is then transferred while in a data/wait state. READY# or WAITo# is used to insert wait states. BLAST# is asserted during the last data/wait state to signify the last transfer of the access. After all data has been transferred, the bus enters the recovery state to allow the bus devices to recover. After recovery state, the bus enters the idle state and waits for another access.

2.2.2 Local Signals

The key Local Bus control signals shown in most timing diagram examples are as follows:

- ADS# or ALE indicates the start of an access
- READY#, WAITo#, and BTERM# are used to assert wait states and terminating Burst cycles during Data transfers
- LW/R#, direction of Data transfer
- BLAST#, BTERM# indicate the end of an access

The key data signals are:

- LAD address, data bus
- LBE# local byte enables, indicating valid byte lanes

2.2.3 Local Bus Signals

There are four groups of Local Bus signals:

- Clock
- Address/Data
- Control/Status
- Arbitration

Signal usage varies upon application.

2.2.3.1 Clock

LCLK, the Local Bus clock, operates at frequencies up to 60 MHz, and is asynchronous to the PCI Bus clock. Most Local Bus signals are driven and sampled on the rising edge of LCLK. Setup and hold times, with respect to LCLK, must be observed. (Refer to Section 12.2 for setup and hold timing requirements.)

2.2.3.2 Address/Data

2.2.3.2.1 LAD[31:0] (Multiplexed Bus)

The LAD[31:0] bus is a 32-bit multiplexed address/data bus. During an Address phase, LAD[27:2] contains the word address of the transfer.

Note: *Dedicated address pins are available.*

During Data phases, LAD[31:0], LAD[15:0], or LAD[7:0] contain transfer data for a 32-, 16-, or 8-bit bus, respectively. If the bus is 8- or 16-bit wide, the data supplied by the PCI 9030 is replicated across the entire 32-bit wide bus.

2.2.3.2.2 LD[31:0] (Non-Multiplexed Bus)

The LD[31:0] bus is a 32-bit non-multiplexed data bus. During Data phases, LD[31:0], LD[15:0], or LD[7:0] contain transfer data for a 32-, 16-, or 8-bit bus, respectively. If the bus is 8- or 16-bit wide, the data supplied by the PCI 9030 is replicated across the entire 32-bit wide bus.

2.2.3.2.3 LA[27:2] (Non-Multiplexed Bus)

LA[27:2] contains the word address of the transfer.

2.2.3.3 Control/Status

The control/status signals control the address latches and flow of data across the Local Bus.

2.2.3.3.1 ADS#, ALE

A Local Bus access starts when ADS# (address/data status) is asserted during an address state by the Local Bus Master. ALE is used to strobe the LA/LAD Bus into an external address latch.

2.2.3.3.2 LBE[3:0]#

During an Address phase, the LBE[3:0]# byte enables denote which byte lanes are being used during access of a 32-bit bus. They remain asserted until the end of the data transfer.

2.2.3.3.3 LW/R#

During an Address phase, LW/R# is driven to a valid state, and signifies direction of the data transfer. Since the PCI 9030 is the Local Bus master, LWR# is driven high when the PCI 9030 is writing data to a Local Bus, and low when it is reading the bus.

2.2.3.3.4 READY#

The READY# input pin has a corresponding Enable bit in the Configuration registers for each Local address space. If READY# is enabled, this indicates that Write data is being accepted or Read data is being provided by the bus slave. If a Bus Slave needs to insert wait states, it can de-assert READY# until it is ready to accept or provide data. If READY# is disabled, then the length of the Local Bus transfer can be determined by internal wait state generators. (Refer to Table 2-3.)

Table 2-3. READY Data Transfers

Master Device	Slave Device	READY# Input Enable	READY# Signal	Description
PCI 9030	Address spaces	0	Ignored	READY# is not sampled by the PCI 9030. Data transfers determined by the internal wait state generator. READY# is ignored and the Data transfer takes place after the internal wait state counter expires.
		1	Sampled	READY# is sampled by the PCI 9030. Data transfers are determined by an external device, which asserts READY# to indicate a Data transfer is taking place.

2.2.3.3.5 WAITo#

Because the PCI 9030 is the Local Bus Master, WAITo# is an output that provides status of the internal wait state generators. It is asserted while internal wait states are being inserted. READY# as an input is not sampled until WAITo# is de-asserted.

2.2.3.3.6 LLOCKo#

When the PCI 9030 owns the Local Bus, LLOCKo# is asserted to indicate that an atomic operation for a PCI Target access may require multiple transactions to complete. LLOCKo# is asserted during the Address phase of the first transaction of the atomic operation, and de-asserted one clock after the last transaction of the atomic operation is complete. If enabled, the Local Bus arbiter does not grant the Bus to another Master until the atomic operation is complete.

2.2.3.3.7 WR#

WR# is a general purpose write output strobe. The timing is controlled by the current Bus Region Descriptor register. The WR# strobe is asserted during the entire data transfer.

2.2.3.3.8 RD#

RD# is a general purpose read output strobe. The timing is controlled by the current Bus Region Descriptor register. The RD# strobe is asserted during the entire data transfer.

2.2.3.3.9 LREQ

LREQ is asserted by a Local Bus Master to request Local Bus use.

2.2.3.3.10 LGNT

LGNT is asserted by the PCI 9030 to grant control of the Local Bus to a Local Bus Master. When the PCI 9030 requires the Local Bus, it can signal a preempt by de-asserting LGNT, if configured to do so in the Configuration register.

2.2.4 Local Bus Interface and Bus Cycles

The PCI 9030 is the Local Bus Master. The PCI 9030 interfaces a PCI Host Bus to two Local Bus types, as listed in Table 2-4. It operates in one of two modes, selected through the MODE pin, corresponding to two bus types—Multiplexed and Non-Multiplexed.

Notes: *No PCI Initiator capability.*

Internal registers are not readable/writable from the Local Bus. The internal registers are accessible from the Host CPU on the PCI Bus or from the serial EEPROM.

Table 2-4. Local Bus Types

MODE Pin	Mode	Bus Type
1	Multiplexed	32-bit multiplexed
0	Non-Multiplexed	32-bit non-multiplexed

2.2.4.1 Local Bus Arbitration

The PCI 9030 is the Local Bus Master. When the PCI Bus initiates a new transfer request, the PCI 9030 takes Local Bus control. Another device can gain Local Bus control by asserting LREQ. If the PCI 9030 has no cycles to run, it asserts LGNT, transferring control to the external master. If the PCI 9030 requires the Local Bus before the external master has completed, LGNT is de-asserted (default preempt condition). The PCI 9030 Local Bus Arbiter also allows the LGNT signal to remain active until the external Local Bus Master completes the transfer, although the PCI 9030 has a PCI Target transaction pending (CNTRL[7]; 50h). The arbiter waits for LREQ to de-assert before taking control of the bus.

2.2.4.2 Wait State Control

The following figure illustrates wait state control.

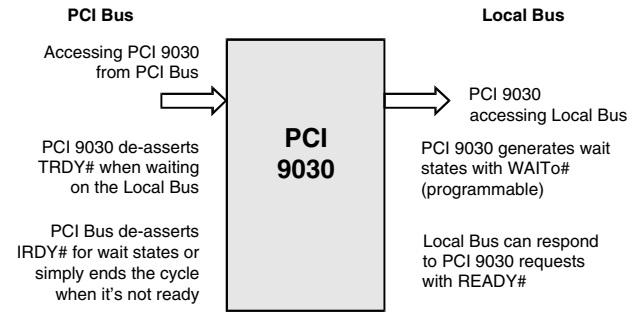


Figure 2-2. Wait States

Note: *The figure represents a sequence of Bus cycles.*

If READY# mode is disabled, the external READY# input signal has no effect on wait states for a Local access. Wait states between Data cycles are asserted internally by a wait state counter. The wait state counter is initialized with its Configuration register value at the start of each data access.

If READY# mode is enabled and the internal wait state counter is zero (default value), the READY# input controls the number of additional wait states.

If READY# mode is enabled and the internal wait state counter is programmed to a non-zero value, READY# has no effect until the wait state counter reaches 0. When it reaches 0, the READY# input controls the number of additional wait states.

If the internal wait state counter is programmed to a non-zero value and BTERM# is enabled, BTERM# input is not sampled until the wait state counter reaches 0.

2.2.4.2.1 Wait States—Local Bus

In PCI Target mode, the PCI 9030 as a Local Bus Master inserts internal wait states with the WAITo# signal. The Local Memory Controller can assert external wait states by delaying the READY# signal.

The following Internal Wait State bit(s) can be used to program the number of internal wait states between the first address-to-data state (and subsequent data-to-data in Burst mode):

- LAS0BRD[10:6, 12:11, 19:15, 21:20],
- LAS1BRD1[10:6, 12:11, 19:15, 21:20],
- LAS2BRD[10:6, 12:11, 19:15, 21:20], and/or
- LAS3BRD[10:6, 12:11, 19:15, 21:20]

2.2.4.3 Burst Mode and Continuous Burst Mode (Bterm "Burst Terminate" Mode)

Note: *In the following sections, Bterm refers to the PCI 9030 internal register bit and BTERM# refers to the PCI 9030 external signal.*

2.2.4.3.1 Burst and Bterm Modes

As an input, BTERM# is asserted by external logic. It instructs the PCI 9030 to break up a Burst cycle.

Table 2-5. Burst and Bterm on the Local Bus

Mode	Burst	Bterm	Result
Single Cycle	0	0	One ADS# per data (default)
	0	1	One ADS# per data
Burst-4 Lword	1	0	One ADS# per four data
Continuous Burst	1	1	One ADS# per BTERM# (refer to Section 2.2.4.3.2.1)

On the Local Bus, BLAST# and BTERM# perform the following:

- If the Burst Mode bit is enabled, but the Bterm Mode bit is disabled, the PCI 9030 bursts (up to four Data phases). BLAST# is asserted at the beginning of the fourth Lword Data phase (LA[3:2]=11) and a new ADS# is asserted at the first Lword (LA[3:2]=00) of the next burst.
- If BTERM# is enabled and asserted, the PCI 9030 terminates the Burst cycle at the end of the current Data phase without generating BLAST#. The PCI 9030 generates a new burst transfer, starting with a new ADS#, terminating it normally using BLAST#.
- The BTERM# input is valid only when the PCI 9030 is performing a PCI Target transaction.
- BTERM# is used to indicate a Memory access is crossing a page boundary or requires a new Address cycle.
- If the internal wait state counter is programmed to a non-zero value and BTERM# is enabled, the BTERM# input is not sampled until the wait state counter reaches 0.
- BTERM# always overrides READY#, even if both signals are asserted. BTERM# executes the ongoing transaction and causes the PCI 9030 to initiate a new Address/Data cycle for Burst transactions.

Note: *If the Bterm Mode bit is disabled, the PCI 9030 performs the following:*

- ***32-bit Local Bus****—Bursts up to four Lwords*
- ***16-bit Local Bus****—Bursts up to two Lwords*
- ***8-bit Local Bus****—Bursts up to one Lword*

In every case, it performs four data beats.

2.2.4.3.2 Burst-4 Lword Mode

If the Burst Mode bit is enabled and the Bterm Mode bit is disabled, bursting can start on any Lword boundary and continue up to a 16-byte address boundary. After data up to the boundary is transferred, the PCI 9030 asserts a new Address cycle (ADS#).

Table 2-6. Burst-4 Lword Mode

Bus Width	Burst
32 bit	Four Lwords or up to a quad Lword boundary (LA3, LA2 = 11)
16 bit	Four words or up to a quad word boundary (LA2, LA1 = 11)
8 bit	Four bytes or up to a quad byte boundary (LA1, LA0 = 11)

2.2.4.3.2.1 Continuous Burst Mode (Bterm "Burst Terminate" Mode)

If both the Burst and Bterm Mode bits are enabled, the PCI 9030 can operate beyond the Burst-4 Lword mode.

Bterm mode enables the PCI 9030 to perform long bursts to devices that can accept bursts of longer than four Lwords. The PCI 9030 asserts one Address cycle and continues to burst data. If a device requires a new Address cycle (ADS#), it can assert the BTERM# input to cause the PCI 9030 to assert a new Address cycle. The BTERM# input acknowledges the current Data transfer (replacing READY#) and requests that a new Address cycle be asserted (ADS#). The new address is for the next Data transfer. If the Bterm Mode bit is enabled and the BTERM# signal is asserted, the PCI 9030 asserts BLAST# only if its Read FIFO is full, its Write FIFO is empty, or a transfer is complete.

2.2.4.3.3 Partial Lword Accesses

Partial Lword accesses are Lword accesses in which not all byte enables are asserted.

Table 2-7. PCI Target Single and Burst Reads

Bus	PCI Target Single Reads	PCI Target Burst Reads
32-, 16-, or 8-bit Local Bus	Passes the byte enables	Ignores the byte enables and all 32-bit data is passed

Burst Start addresses can be any Lword boundary. If the Burst Start address in a PCI Target transfer is not aligned to an Lword boundary, the PCI 9030 first performs a Single cycle. It then starts to burst on the Lword boundary.

2.2.4.4 Recovery States (Multiplexed Mode Only)

In Multiplexed mode, the PCI 9030 inserts one recovery state between the last Data transfer and the next Address cycle. The recovery state prevents possible bus contention during the completion of a Read cycle. If the PCI 9030 began driving the bus prior to the Slave device providing the Read data, bus contention could occur.

Note: *The PCI 9030 does not support the i960J function that uses the READY# input to add recovery states. No additional recovery states are added if the READY# input remains asserted during the last Data cycle.*

2.2.4.5 Local Bus Read Accesses

For all Single-Cycle Local Bus Read accesses, the PCI 9030 reads only bytes corresponding to byte enables requested by a PCI Initiator. For all Burst Read cycles, the PCI 9030 can be programmed to:

- Perform PCI Target Delayed Reads
- Perform PCI Target Read Ahead
- Generate internal wait states
- Enable external wait control (READY# input)
- Enable type of Burst mode to perform

2.2.4.6 Local Bus Write Accesses

For Local Bus writes, only bytes specified by a PCI Bus Master are written.

For all Burst Write cycles, the PCI 9030 can be programmed to:

- Perform PCI Target Delayed Writes
- Generate internal wait states
- Enable external wait control (READY# input)

2.2.5 Local Bus Big/Little Endian Mode

For each of the following transfer types, the PCI 9030 Local Bus can be independently programmed to operate in Little Endian or Big Endian mode:

- PCI Target accesses to Local Address Space 0
- PCI Target accesses to Local Address Space 1
- PCI Target accesses to Local Address Space 2
- PCI Target accesses to Local Address Space 3
- PCI Target accesses to Expansion ROM

Notes: *The PCI Bus is always Little Endian.*
Only byte lanes are swapped, not individual bits.

The PCI 9030 Local Bus can be programmed to operate in Big or Little Endian mode, as shown in Table 2-8 and Table 2-9.

Table 2-8. Byte Number and Lane Cross-Reference—Multiplexed Mode

Byte Number		Byte Lane
Big Endian	Little Endian	
3	0	LAD[7:0]
2	1	LAD[15:8]
1	2	LAD[23:16]
0	3	LAD[31:24]

Table 2-9. Byte Number and Lane Cross-Reference—Non-Multiplexed Mode

Byte Number		Byte Lane
Big Endian	Little Endian	
3	0	LD[7:0]
2	1	LD[15:8]
1	2	LD[23:16]
0	3	LD[31:24]

The following table lists PCI Target cycle register information.

Table 2-10. Cycle Reference Table

Cycle	Register Bits
PCI Target	LAS0BRD[24] Space 0 LAS1BRD[24] Space 1 LAS2BRD[24] Space 2 LAS3BRD[24] Space 3 EROMBRD[24] Expansion ROM

In Big Endian mode, the PCI 9030 transposes data byte lanes. Data is transferred as listed in Table 2-11 through Table 2-15.

2.2.5.1 32-Bit Local Bus—Big Endian Mode

Data is Lword aligned to the uppermost byte lane (Address Invariance).

Table 2-11. Upper Lword Lane Transfer—32-Bit Local Bus

Burst Order	Byte Lane
First Transfer	PCI Byte 0 appears on Local Data [31:24]
	PCI Byte 1 appears on Local Data [23:16]
	PCI Byte 2 appears on Local Data [15:8]
	PCI Byte 3 appears on Local Data [7:0]

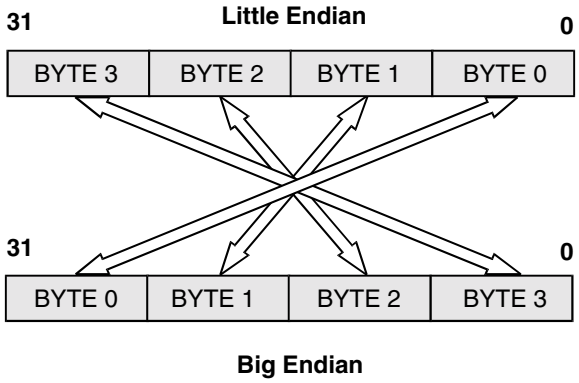


Figure 2-3. Big/Little Endian—32-Bit Local Bus

2.2.5.2 16-Bit Local Bus—Big Endian Mode

For a 16-bit Local Bus, the PCI 9030 can be programmed to use upper or lower word lanes.

Table 2-12. Upper Word Lane Transfer—16-Bit Local Bus

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [31:24]
	Byte 1 appears on Local Data [23:16]
Second Transfer	Byte 2 appears on Local Data [31:24]
	Byte 3 appears on Local Data [23:16]

Table 2-13. Lower Word Lane Transfer—16-Bit Local Bus

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [15:8]
	Byte 1 appears on Local Data [7:0]
Second Transfer	Byte 2 appears on Local Data [15:8]
	Byte 3 appears on Local Data [7:0]

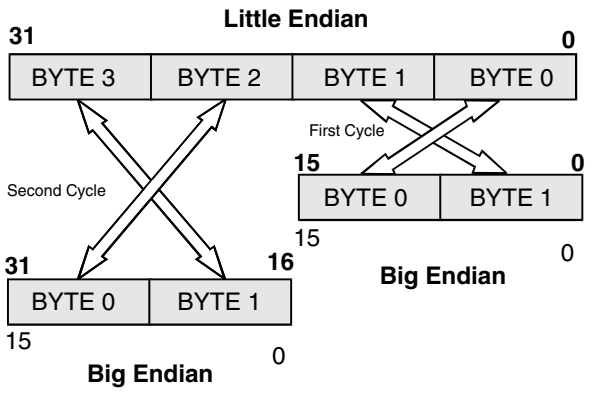


Figure 2-4. Big/Little Endian—16-Bit Local Bus

2.2.5.3 8-Bit Local Bus—Big Endian Mode

For an 8-bit Local Bus, the PCI 9030 can be programmed to use upper or lower byte lanes.

Table 2-14. Upper Byte Lane Transfer—8-Bit Local Bus

Burst Order	Byte Lane
First transfer	Byte 0 appears on Local Data [31:24]
Second transfer	Byte 1 appears on Local Data [31:24]
Third transfer	Byte 2 appears on Local Data [31:24]
Fourth transfer	Byte 3 appears on Local Data [31:24]

Table 2-15. Lower Byte Lane Transfer—8-Bit Local Bus

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [7:0]
Second Transfer	Byte 1 appears on Local Data [7:0]
Third Transfer	Byte 2 appears on Local Data [7:0]
Fourth Transfer	Byte 3 appears on Local Data [7:0]

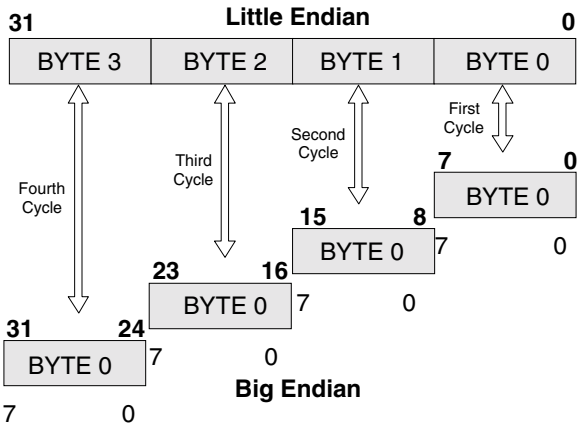


Figure 2-5. Big/Little Endian—8-Bit Local Bus

3 SERIAL EEPROM RESET AND INITIALIZATION

Functional operation described can be modified through the PCI 9030 programmable internal registers.

3.1 OVERVIEW

The PCI 9030 initialization procedures follow these steps:

1. Power on
2. Reset
3. PCI 9030 initialization
4. Serial EEPROM
5. Internal Register Access

3.2 RESET OPERATION

3.2.1 PCI Bus RST# Input

The PCI Bus RST# input pin is a PCI Host reset. It causes all PCI Bus outputs to float, resets the entire PCI 9030 and causes the Local reset LRESETo# signal to be asserted.

3.2.2 Software Reset

A Host on the PCI Bus can set the PCI Adapter Software Reset bit (CNTRL[30]; 50h) to reset the PCI 9030 and assert LRESETo#. The PCI and Local Configuration register contents are not reset as a result. When the Software Reset bit is set (CNTRL[30]=1), the PCI 9030 responds only to Configuration register accesses, and not to Local Bus accesses. The PCI 9030 remains in this reset condition until the PCI Host clears the bit (CNTRL[30]=0).

3.3 PCI 9030 INITIALIZATION

The PCI 9030 Configuration registers can be programmed by an optional serial EEPROM. The serial EEPROM can be reloaded by setting the Reload Configuration Registers bit (CNTRL[29]; 50h).

The PCI 9030 retries all PCI cycles until either the blank serial EEPROM is detected or the serial EEPROM configuration is complete.

After a PCI reset and serial EEPROM load, the software determines the amount of required address space by writing all ones (1) to a PCI Base Address register and then reading back the value. The PCI 9030 returns zeroes (0) in the Don't Care Address bits, effectively specifying the address space required, at which time the PCI software maps the Local Address space into the PCI Address space by programming the PCI Base Address register. (Refer to Figure 3-1.)

3.4 SERIAL EEPROM

3.4.1 Vendor ID and Device ID Registers

The PCI 9030 supports two Vendor ID and Device ID registers:

- **PCIIDR**—Contains the normal Device and Vendor IDs. Can be loaded from the serial EEPROM or Local processor(s).
- **PCISVID**—Contains the Subsystem and Subsystem Vendor IDs. Can be loaded from the serial EEPROM.

3.4.1.1 Serial EEPROM Initialization

During serial EEPROM initialization, the PCI 9030 responds to PCI Target accesses with a Retry.

3.4.2 Serial EEPROM Operation

After reset, the PCI 9030 attempts to read the serial EEPROM to determine its presence. An active start bit set to 0 indicates a serial EEPROM is present. The PCI 9030 supports 93CS56L (2K bit) or 93CS66L (4K bit). (Refer to manufacturer's data sheet for the particular serial EEPROM being used.) The first 33 bits are then checked to verify that the serial EEPROM is programmed. If the first 33 bits are all ones, a blank serial EEPROM is present.

For blank serial EEPROM conditions, the PCI 9030 reverts to the default values (refer to Table 3-1). When the Serial EEPROM Valid bit is set to 1 (CNTRL[28]=1), if programmed, real or random data is detected in the serial EEPROM.

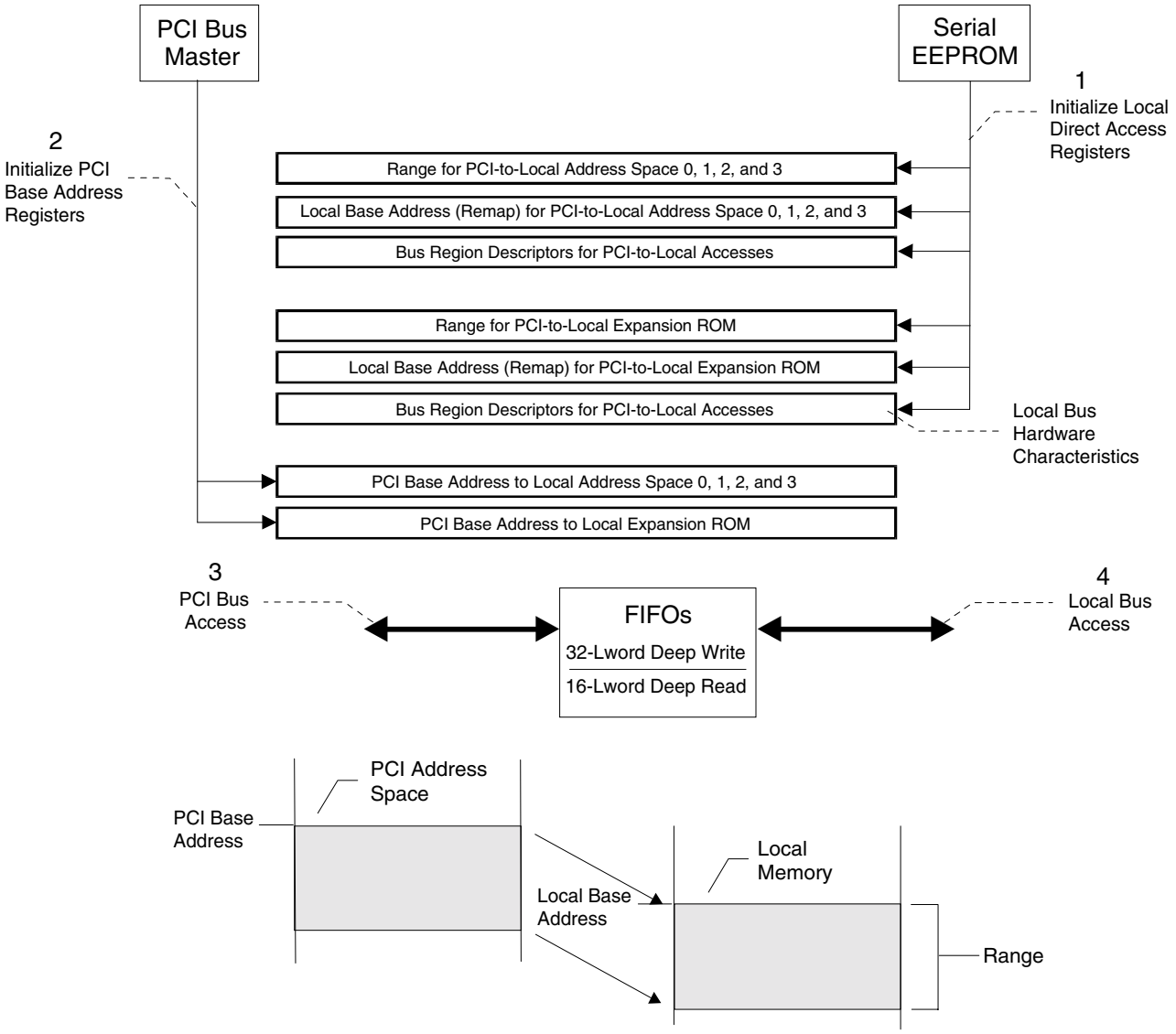


Figure 3-1. Local Bus PCI Target Access

An active start bit set to 1 indicates that a serial EEPROM is not present. For missing serial EEPROM conditions, the PCI 9030 stops the serial EEPROM load and reverts to the default values within 13 serial EEPROM clocks (EESK).

The 3.3V serial EEPROM clock is derived from the PCI clock. The PCI 9030 generates the serial EEPROM clock by internally dividing the PCI clock by 132.

Table 3-1. Serial EEPROM Guidelines

Serial EEPROM	PCI 9030 System Boot Condition
None	Uses default values (Start bit is 1).
Programmed	Boots with serial EEPROM values (Start bit is 0).
Blank	Detects a blank device and reverts to default values (Start bit is 0).

The serial EEPROM can be read or written from the PCI Bus. The Serial EEPROM Control Register bits (CNTRL[28:24]) control the PCI 9030 pins that enable reading or writing of serial EEPROM data bits. (Refer to manufacturer's data sheet for the particular serial EEPROM being used.)

The serial EEPROM can also be read or written, using the VPD function (refer to Section 9). The PCI 9030 loads 34 Lwords from the serial EEPROM.

3.4.2.1 Serial EEPROM Load

The registers listed in Table 3-2 are loaded from the serial EEPROM after a reset is de-asserted. The serial EEPROM is organized in words (16 bit). The PCI 9030 first loads the Most Significant Word bits (MSW[31:16]), starting from the most significant bit ([31]). The PCI 9030 then loads the Least Significant Word bits (LSW[15:0]), starting again from the most significant bit ([15]). Therefore, the PCI 9030 loads the Device ID, Vendor ID, class code, and so forth.

The serial EEPROM values can be programmed using a Data I/O programmer. The values can also be programmed using the PCI 9030 VPD function (refer to Section 9) or through the Serial EEPROM Control register (CNTRL).

The CNTRL register allows programming of the serial EEPROM, one bit at a time. To read back the value from the serial EEPROM, the Vital Product Data (VPD) function should be utilized. With full utilization of VPD, the designer can perform reads and writes from/to the serial EEPROM, 32 bits at a time. Values should be programmed in the order listed in Table 3-2. The 68, 16-bit words listed in the table are stored sequentially in the serial EEPROM.

Table 3-2. Serial EEPROM Register Load Sequence

Serial EEPROM Offset	Register Offset	Register Description	Register Bits Affected
00h	PCI 02h	Device ID	PCIIDR[31:16]
02h	PCI 00h	Vendor ID	PCIIDR[15:0]
04h	PCI 06h	PCI Status	PCISR[15:0]
06h	PCI 04h	PCI Command	***Reserved***
08h	PCI 0Ah	Class Code	PCICCR[15:0]
0Ah	PCI 08h	Class Code / Revision	PCICCR[7:0] / PCIREV[7:0]
0Ch	PCI 2Eh	Subsystem ID	PCISID[15:0]
0Eh	PCI 2Ch	Subsystem Vendor ID	PCISVID[15:0]
10h	PCI 36h	MSB New Capability Pointer	***Reserved***
12h	PCI 34h	LSB New Capability Pointer	CAP_PTR[7:0]
14h	PCI 3Eh	(Maximum Latency and Minimum Grant are not loadable)	***Reserved***
16h	PCI 3Ch	Interrupt Pin (Interrupt Line Routing is not loadable)	PCIIPR[7:0] / PCIILR [7:0]
18h	PCI 42h	MSW of Power Management Capabilities	PMC[14:11, 5, 3:0]
1Ah	PCI 40h	LSW of Power Management Next Capability Pointer / Power Management Capability ID	PMNEXT[7:0] / PMCAPID[7:0]
1Ch	PCI 46h	MSW of Power Management Data / PMCSR Bridge Support Extension	***Reserved***
1Eh	PCI 44h	LSW of Power Management Control/Status	PMCSR[14:8]
20h	PCI 4Ah	MSW of Hot Swap Control/Status	***Reserved***
22h	PCI 48h	LSW of Hot Swap Next Capability Pointer / Hot Swap Control	HS_NEXT[7:0] / HS_CNTL[7:0]
24h	PCI 4Eh	PCI Vital Product Data Address	***Reserved***
26h	PCI 4Ch	PCI Vital Product Data Next Capability Pointer/ PCI Vital Product Data Control	PVPD_NEXT[7:0] / PVPDCNTL[7:0]
28h	Local 02h	MSW of Range for PCI-to-Local Address Space 0	LAS0RR[31:16]
2Ah	Local 00h	LSW of Range for PCI-to-Local Address Space 0	LAS0RR[15:0]
2Ch	Local 06h	MSW of Range for PCI-to-Local Address Space 1	LAS1RR[31:16]
2Eh	Local 04h	LSW of Range for PCI-to-Local Address Space 1	LAS1RR[15:0]
30h	Local 0Ah	MSW of Range for PCI-to-Local Address Space 2	LAS2RR[31:16]
32h	Local 08h	LSW of Range for PCI-to-Local Address Space 2	LAS2RR[15:0]
34h	Local 0Eh	MSW of Range for PCI-to-Local Address Space 3	LAS3RR[31:16]
36h	Local 0Ch	LSW of Range for PCI-to-Local Address Space 3	LAS3RR[15:0]
38h	Local 12h	MSW of Range for PCI-to-Local Expansion ROM	EROMRR[31:16]
3Ah	Local 10h	LSW of Range for PCI-to-Local Expansion ROM	EROMRR[15:0]
3Ch	Local 16h	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	LAS0BA[31:16]
3Eh	Local 14h	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	LAS0BA[15:0]

Table 3-2. Serial EEPROM Register Load Sequence (Continued)

Serial EEPROM Offset	Register Offset	Register Description	Register Bits Affected
40h	Local 1Ah	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	LAS1BA[31:16]
42h	Local 18h	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	LAS1BA[15:0]
44h	Local 1Eh	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 2	LAS2BA[31:16]
46h	Local 1Ch	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 2	LAS2BA[15:0]
48h	Local 22h	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 3	LAS3BA[31:16]
4Ah	Local 20h	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 3	LAS3BA[15:0]
4Ch	Local 26h	MSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM	EROMBA[31:16]
4Eh	Local 24h	LSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM	EROMBA[15:0]
50h	Local 2Ah	MSW of Bus Region Descriptors for Local Address Space 0	LAS0BRD[31:16]
52h	Local 28h	LSW of Bus Region Descriptors for Local Address Space 0	LAS0BRD[15:0]
54h	Local 2Eh	MSW of Bus Region Descriptors for Local Address Space 1	LAS1BRD[31:16]
56h	Local 2Ch	LSW of Bus Region Descriptors for Local Address Space 1	LAS1BRD[15:0]
58h	Local 32h	MSW of Bus Region Descriptors for Local Address Space 2	LAS2BRD[31:16]
5Ah	Local 30h	LSW of Bus Region Descriptors for Local Address Space 2	LAS2BRD[15:0]
5Ch	Local 36h	MSW of Bus Region Descriptors for Local Address Space 3	LAS3BRD[31:16]
5Eh	Local 34h	LSW of Bus Region Descriptors for Local Address Space 3	LAS3BRD[15:0]
60h	Local 3Ah	MSW of Bus Region Descriptors for Expansion ROM	EROMBRD[31:16]
62h	Local 38h	LSW of Bus Region Descriptors for Expansion ROM	EROMBRD[15:0]
64h	Local 3Eh	MSW of Chip Select (CS) 0 Base and Range	CS0BASE[31:16]
66h	Local 3Ch	LSW of Chip Select (CS) 0 Base and Range	CS0BASE[15:0]
68h	Local 42h	MSW of Chip Select (CS) 1 Base and Range	CS1BASE[31:16]
6Ah	Local 40h	LSW of Chip Select (CS) 1 Base and Range	CS1BASE[15:0]
6Ch	Local 46h	MSW of Chip Select (CS) 2 Base and Range	CS2BASE[31:16]
6Eh	Local 44h	LSW of Chip Select (CS) 2 Base and Range	CS2BASE[15:0]
70h	Local 4Ah	MSW of Chip Select (CS) 3 Base and Range	CS3BASE[31:16]
72h	Local 48h	LSW of Chip Select (CS) 3 Base and Range	CS3BASE[15:0]
74h	Local 4Eh	Serial EEPROM Write-Protected Address Boundary	PROT_AREA[7:0]
76h	Local 4Ch	LSW of Interrupt Control/Status Register	INTCSR[15:0]
78h	Local 52h	MSW of PCI Target Response, Serial EEPROM, and Initialization Control	CNTRL[31:16]
7Ah	Local 50h	LSW of PCI Target Response, Serial EEPROM, and Initialization Control	CNTRL[15:0]
7Ch	Local 56h	MSW of General Purpose I/O Control	GPIOC[31:16]
7Eh	Local 54h	LSW of General Purpose I/O Control	GPIOC[15:0]

Table 3-2. Serial EEPROM Register Load Sequence (Continued)

Serial EEPROM Offset	Register Offset	Register Description	Register Bits Affected
80h	Local 72h	MSW of Hidden 1 Power Management Data Select (refer to Section 7.2.1)	PMDATA[7:0] hidden, D_0 and D_{3hot} Power Dissipated
82h	Local 70h	LSW of Hidden 1 Power Management Data Select (refer to Section 7.2.1)	PMDATA[7:0] hidden, D_0 and D_{3hot} Power Consumed
84h	Local 76h	MSW of Hidden 2 Power Management Data Scale (refer to Section 7.2.1)	***Reserved***
86h	Local 74h	LSW of Hidden 2 Power Management Data Scale (refer to Section 7.2.1)	PMCSR[14:13] hidden, Bits [7:0] are used as follows: [7:6] D_{3hot} Power Dissipated, [5:4] D_0 Power Dissipated, [3:2] D_{3hot} Power Consumed, [1:0] D_0 Power Consumed

3.4.2.2 Recommended Serial EEPROMs

The PCI 9030 is designed to use either a 2K-bit (NM93CS56L or compatible) or 4K-bit (NM93CS66L or compatible) device.

Note: *The PCI 9030 does not support serial EEPROMs that do not support sequential reads and writes (such as the NM93C56L).*

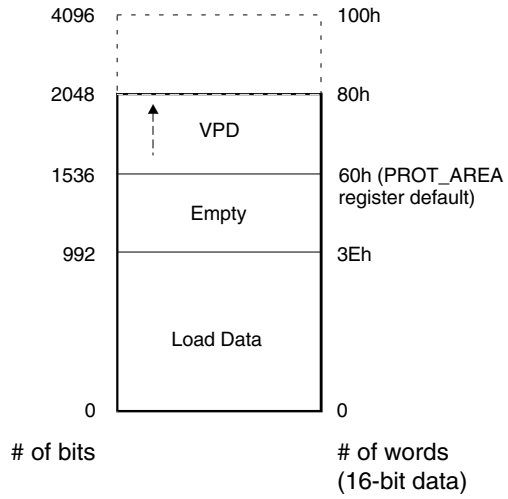


Figure 3-2. Serial EEPROM Memory Map

3.5 INTERNAL REGISTER ACCESS

The PCI 9030 provides several internal registers, which allow for maximum flexibility in the bus-interface design and performance. They are accessible from the PCI Bus and include the following registers:

- PCI Configuration
- Local Configuration
- Power Management
- Hot Swap
- VPD

The following figure illustrates how these registers are accessed.

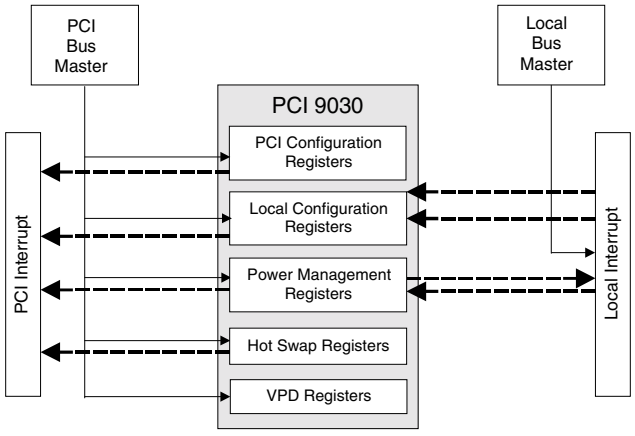


Figure 3-3. PCI 9030 Internal Register Access

3.5.1 PCI Bus Access to Internal Registers

The PCI 9030 PCI Configuration registers can be accessed from the PCI Bus with a Configuration Type 0 cycle.

All other PCI 9030 internal registers can be accessed by a Memory cycle, with the PCI Bus address that matches the base address specified in PCI Base Address 0 (PCIBAR0[31:4]) for the PCI 9030 Memory-Mapped Configuration register. These registers can also be accessed by an I/O cycle, with the PCI Bus address matching the base address specified in PCI Base Address 1 (PCIBAR1[31:2] for the PCI 9030 I/O-Mapped Configuration register.

All PCI Read or Write accesses to the PCI 9030 registers can be Byte, Word, or Lword accesses. All PCI Memory accesses to the PCI 9030 registers can be Burst or Non-Burst accesses. The PCI 9030 responds with a PCI disconnect for all Burst I/O accesses (PCIBAR1[31:2]) to the PCI 9030 Internal registers.

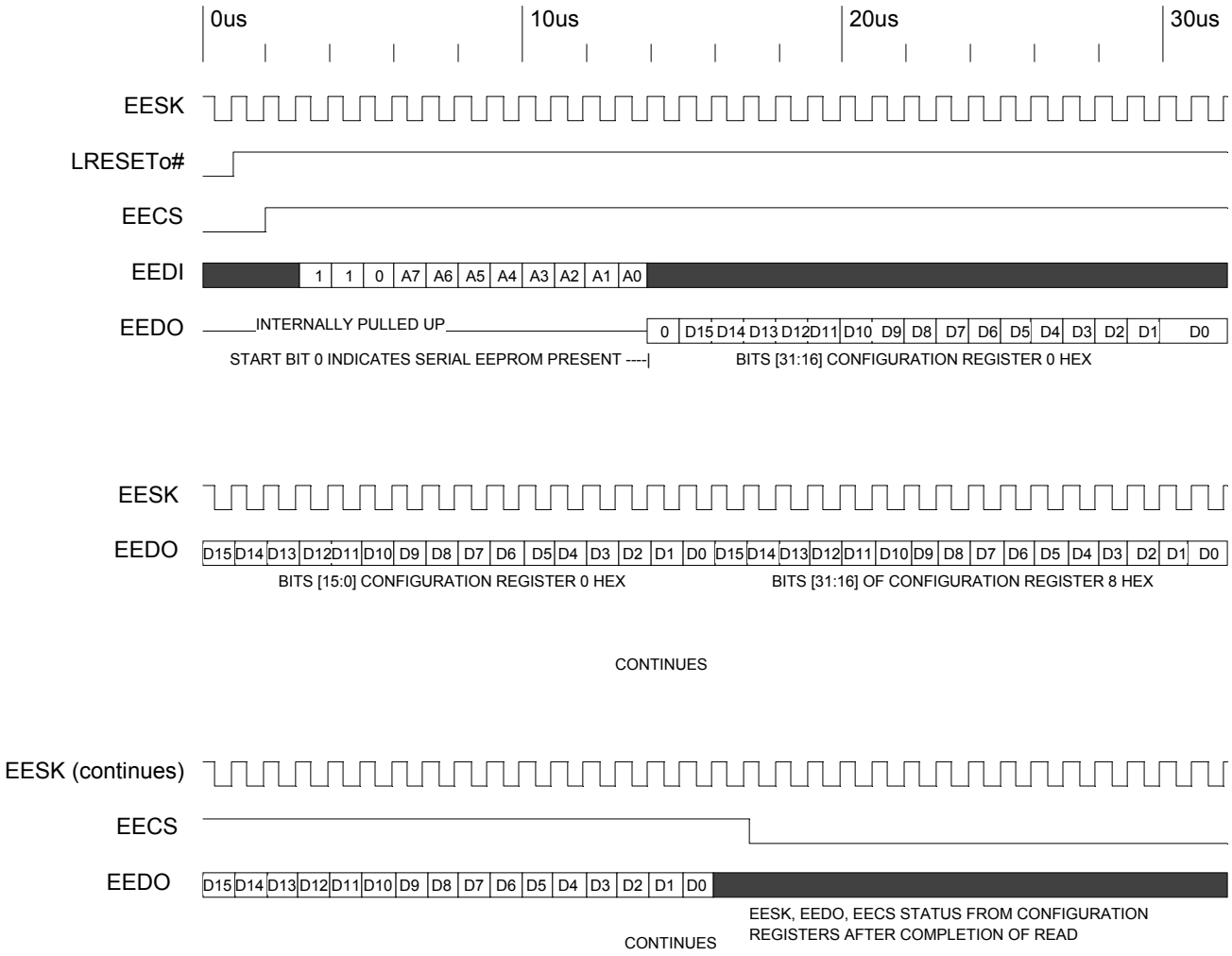
3.6 NEW CAPABILITIES FUNCTION SUPPORT

The New Capabilities Function Support includes PCI Power Management, Hot Swap, and VPD features, as listed in the following table.

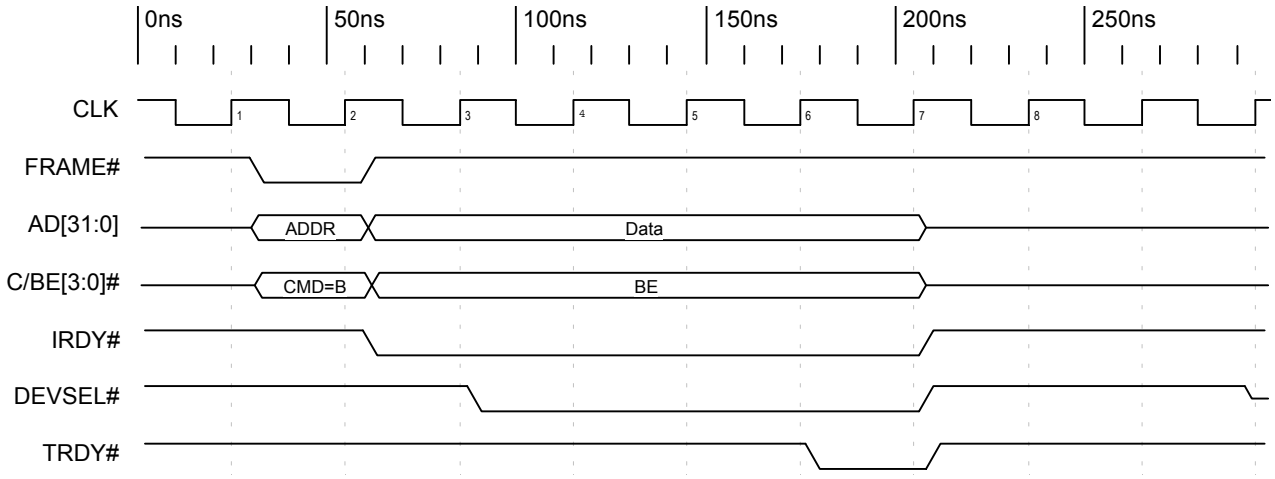
Table 3-3. New Capabilities Function Support Features

New Capability Function	PCI Register Offset Location
First (Power Management)	40h, which is pointed to, from CAP_PTR [7:0].
Second (Hot Swap)	48h, which is pointed to, from PMNEXT[7:0].
Third (VPD)	4Ch, which is pointed to, from HS_NEXT[7:0]. Because PVPD_NEXT[7:0] defaults to zero, this indicates that VPD is the last PCI 9030 New Capability Function Support feature.

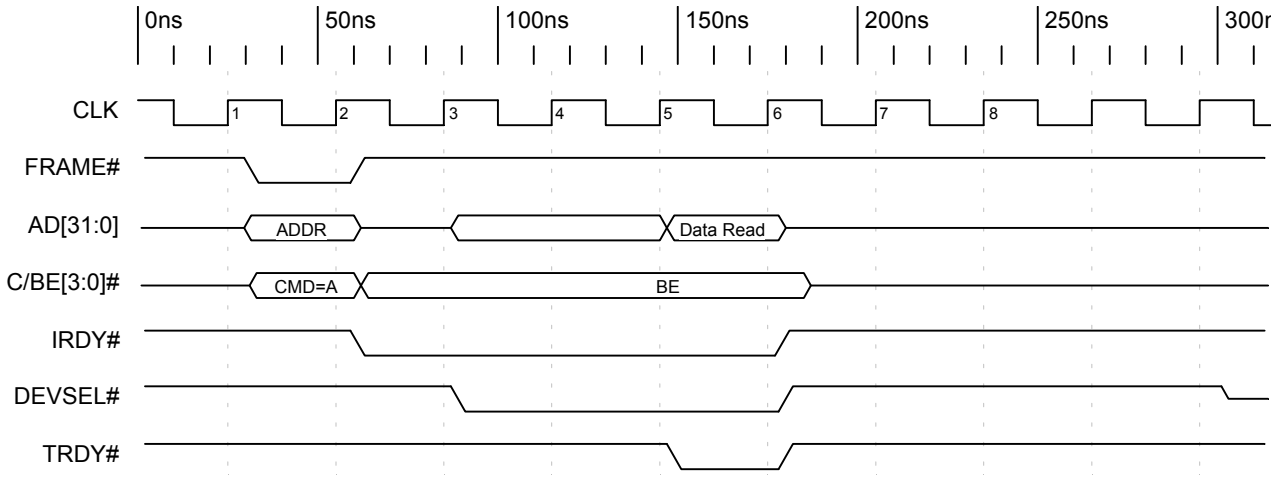
3.7 SERIAL EEPROM AND CONFIGURATION INITIALIZATION TIMING DIAGRAMS



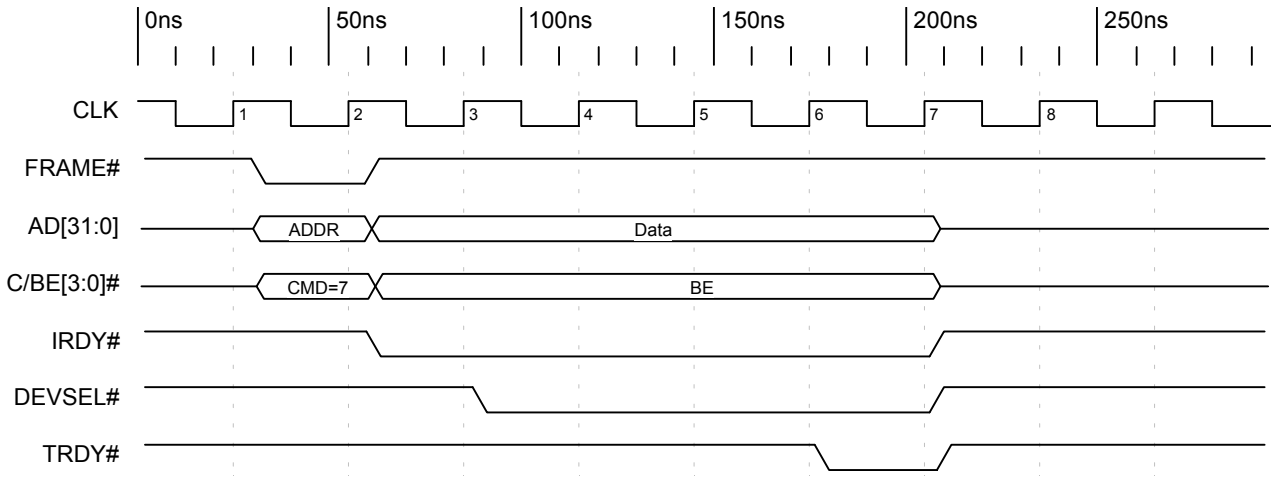
Timing Diagram 3-1. Initialization from Serial EEPROM (2K or 4K Bit)



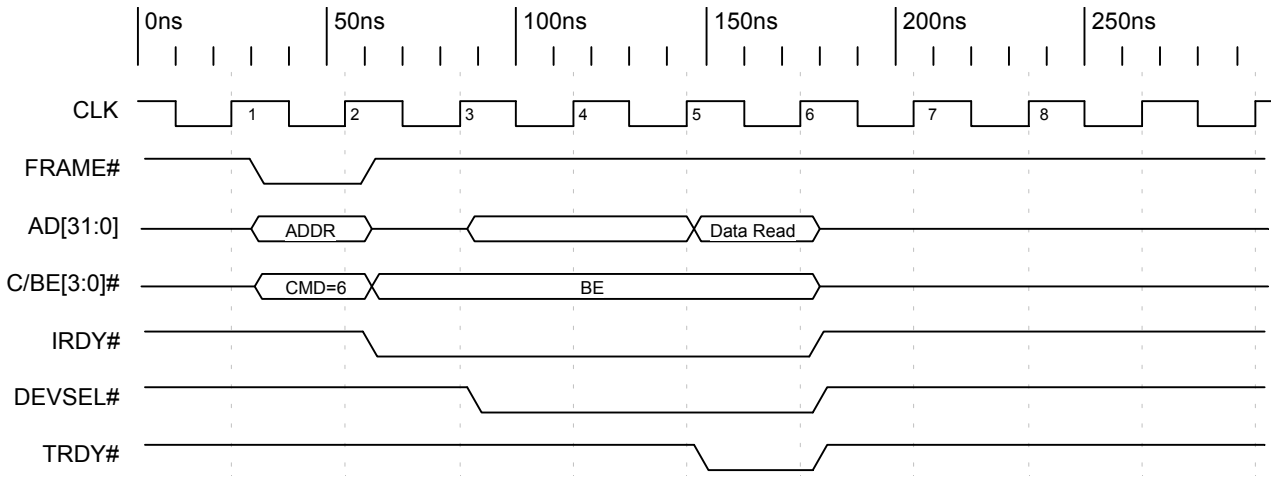
Timing Diagram 3-2. PCI Configuration Write to PCI Configuration Register



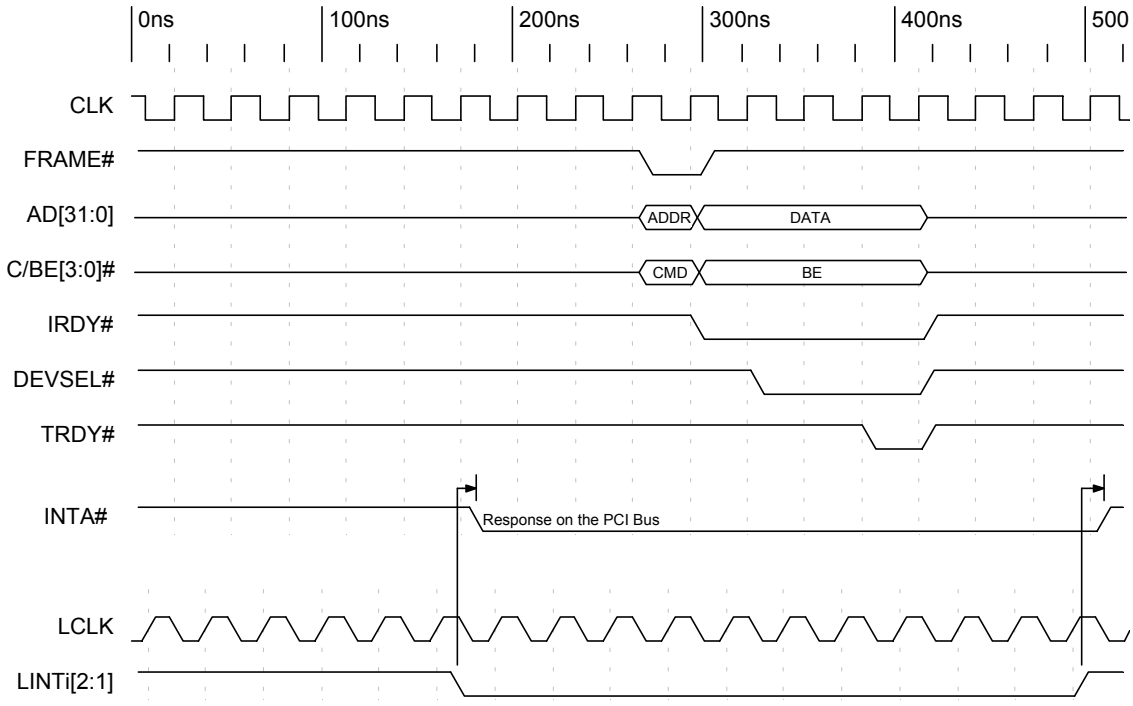
Timing Diagram 3-3. PCI Configuration Read from PCI Configuration Register



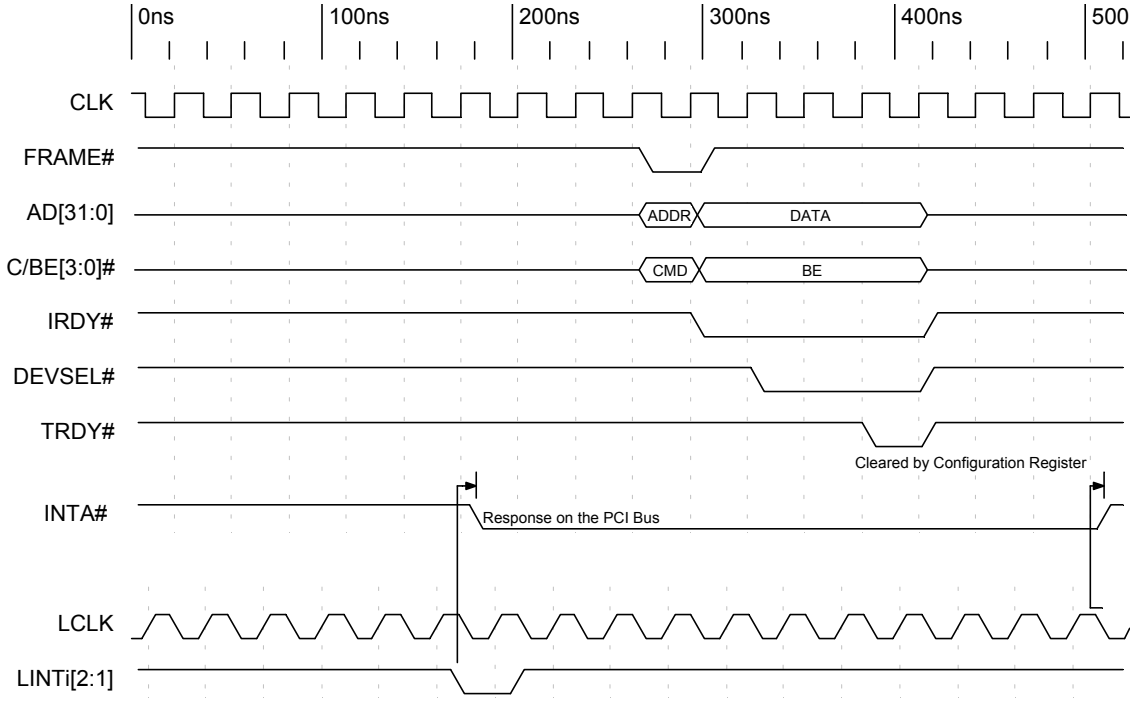
Timing Diagram 3-4. PCI Memory Write to Local Configuration Register



Timing Diagram 3-5. PCI Memory Read from Local Configuration Register



Timing Diagram 3-6. Local Level Triggered Interrupt Asserting PCI Interrupt



Timing Diagram 3-7. Local Edge Triggered Interrupt Asserting PCI Interrupt

4 PCI TARGET (DIRECT SLAVE) OPERATION

Functional operation described can be modified through the PCI 9030 programmable internal registers.

4.1 OVERVIEW

PCI Target (Direct Slave) operations originate on the PCI Bus, go through the PCI 9030, and finally access the Local Bus. The PCI 9030 is a PCI Bus Target and a Local Bus Master.

4.2 DIRECT DATA TRANSFER MODE

The PCI 9030 supports PCI Target accesses to Local Memory or I/O Transfer mode.

4.2.1 PCI Target Operation (PCI Master-to-Local Bus Access)

The PCI 9030 supports both Burst Memory-Mapped Transfer accesses and I/O-Mapped, Single-Transfer accesses to the Local Bus from the PCI Bus through a 16-Lword (64-byte) PCI Target Read FIFO and a 32-Lword (128-byte) PCI Target Write FIFO. The PCI Base Address registers are provided to set up the adapter location in the PCI memory and I/O space. In addition, Local Mapping registers allow address translation from the PCI Address Space to the Local Address Space. Five spaces are available:

- Space 0
- Space 1
- Space 2
- Space 3
- Expansion ROM space

Expansion ROM space is intended to support a bootable ROM device for the Host.

For Single-Cycle PCI Target reads, the PCI 9030 reads a single Local Bus Lword or partial Lword. The PCI 9030 disconnects after one transfer for all PCI Target I/O accesses.

For the highest data-transfer rate, the PCI 9030 supports posted writes and can be programmed to prefetch data during a PCI Burst Read. The Prefetch size, when enabled, can be from one to 16 Lwords or until the PCI Bus stops requesting. When the PCI 9030 prefetches, if enabled, it drops the Local Bus read after reaching the prefetch counter. In Continuous Prefetch mode, the PCI 9030 prefetches as long as FIFO space is available and stops prefetching when the PCI Bus terminates the request. If Read prefetching is disabled, the PCI 9030 stops after one Read transfer.

In addition to Prefetch mode, the PCI 9030 supports PCI Target Read Ahead mode (refer to Section 4.2.1.3).

Each Local space can be programmed to operate in an 8-, 16-, or 32-bit Local Bus width. The PCI 9030 contains an internal wait state generator and external wait state input, READY#. READY# can be disabled or enabled by way of the Internal Configuration registers.

With or without wait state(s), the Local Bus, independent of the PCI Bus, can:

- Burst as long as data is available (Continuous Burst mode)
- Burst four Lwords at a time
- Perform continuous Single cycles

4.2.1.1 PCI Target Lock

The PCI 9030 supports direct PCI-to-Local-Bus Exclusive accesses (locked atomic operations). A PCI-locked operation to the Local Bus results in the entire address Space 0, Space 1, Space 2, Space 3, and Expansion ROM space being locked until they are released by the PCI Bus Master. Locked operations are enabled or disabled with the PCI Target LOCK# Enable bit (CNTRL[23]; 50h) for PCI-to-Local accesses.

4.2.1.2 PCI Target Delayed Read Mode

The PCI 9030 can be programmed to perform PCI Target Delayed Reads (CNTRL[14]; 50h) (refer to Figure 4-1).

In addition to delayed reads, the PCI 9030 supports the following *PCI Local Bus Specification* v2.2 functions:

- No write while a read is pending (PCI Retry for reads)
- Write and flush pending read

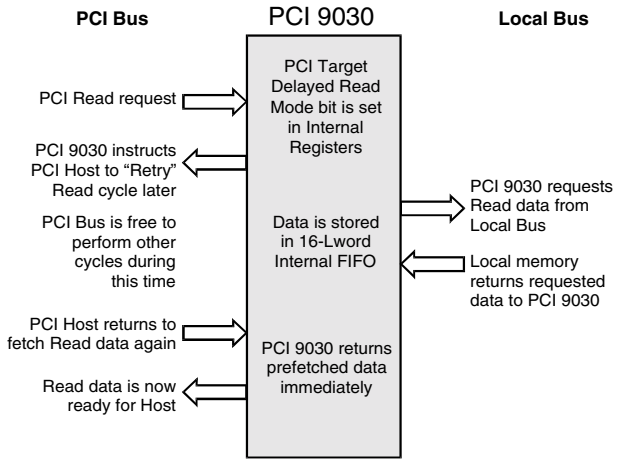


Figure 4-1. PCI Target Delayed Reads

Note: *The figure represents a sequence of Bus cycles.*

4.2.1.3 PCI Target Read Ahead Mode

The PCI 9030 also supports PCI Target Read Ahead mode (CNTRL[16]; 50h), where prefetched data can be read from the PCI 9030 internal FIFO instead of the Local Bus. The address must be subsequent to the previous address and 32-bit aligned (next address = current address + 4). The PCI Target Read Ahead mode functions can be used with or without the PCI Target Delayed Read mode.

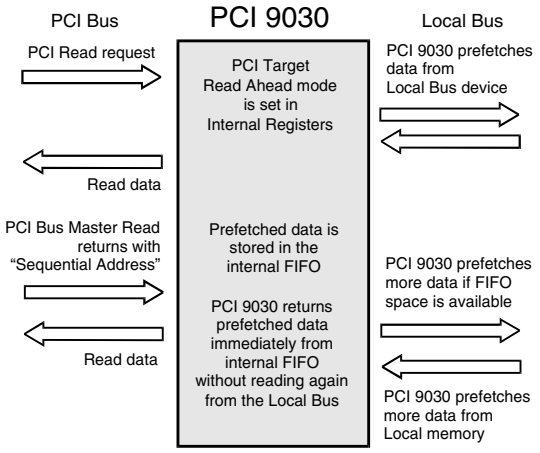


Figure 4-2. PCI Target Read Ahead Mode

Note: *The figure represents a sequence of Bus cycles.*

4.2.1.4 PCI Target Delayed Write Mode

The PCI 9030 supports PCI Target Delayed Write mode transactions, where posted Write data accumulates in the PCI Target Write FIFO before the PCI 9030 requests a Write transaction (ADS# and/or ALE assertion) to be performed on the Local Bus. The PCI Target Delayed Write mode is programmable to delay the ADS# and/or ALE assertion in the amount of Local clocks (CNTRL[11:10]; 50h). This feature is useful for gaining higher throughput during PCI Target Write burst transactions for conditions in which the PCI clock frequency is slower than the Local clock frequency.

4.2.1.5 PCI Target Local Bus READY# Timeout Mode

The PCI 9030 supports PCI Target Local Bus READY# Timeout mode transactions, where the PCI 9030 asserts an internal READY# signal to recover from stalling the Local and PCI Buses. The PCI Target Local Bus READY# Timeout mode transaction is programmable to select the amount of Local clocks before READY# times out (CNTRL[9:8]; 50h). If a Local Target stalls with a READY# assertion during PCI Target Write transactions, the PCI 9030 empties the Write FIFO by dumping the data into the Local Bus and does not pass an error condition to the PCI Bus Initiator. During PCI Target Read transactions, the PCI 9030 issues a PCI Target Abort

to the PCI Bus Initiator every time the PCI Target Local Bus READY# Timeout is detected.

4.2.1.6 PCI Target Transfer

A PCI Bus Master addressing the Memory space decoded for the Local Bus initiates transactions. Upon a PCI Read/Write, the PCI 9030 being a Local Bus Master executes a transfer, at which time it reads data into the PCI Target Read FIFO or writes data to the Local Bus.

The PCI 9030 is programmable to "disconnect" or "keep" the PCI Bus by generating a wait state(s) and de-asserting TRDY# if the Write FIFO becomes full (CNTRL[22:19]; 50h).

For PCI Target writes, the PCI Bus Initiator writes data to the Local Bus. For PCI Target reads, the PCI Bus Initiator reads data from the Local Bus Slave.

The PCI 9030 supports on-the-fly Endian conversion for Space 0, Space 1, Space 2, Space 3, and Expansion ROM space. The Local Bus can be Big/ Little Endian by using the programmable internal register configuration.

Note: *The PCI Bus is always Little Endian.*

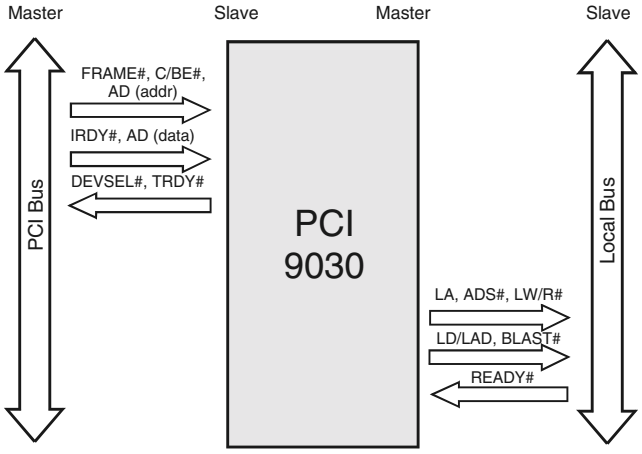


Figure 4-3. PCI Target Write

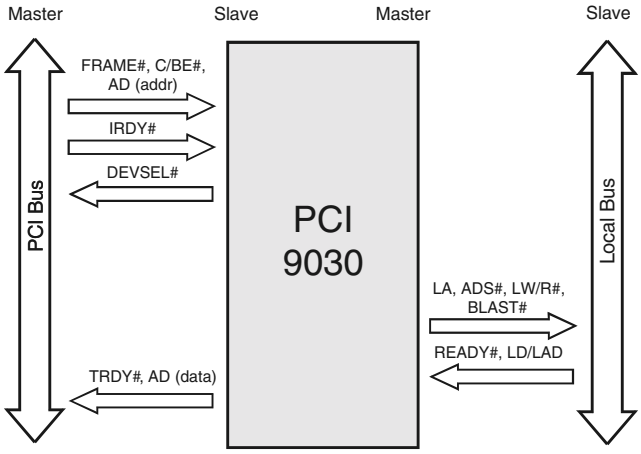


Figure 4-4. PCI Target Read

Note: *The figures represent a sequence of Bus cycles.*

4.2.1.7 PCI Target PCI-to-Local Address Mapping

Five Local Address spaces—Space 0, Space 1, Space 2, Space 3, and Expansion ROM—are accessible from the PCI Bus. Each is defined by a set of three registers:

- Local Address Range (LAS0RR, LAS1RR, LAS2RR, LAS3RR, and/or EROMRR)
- Local Base Address (LAS0BA, LAS1BA, LAS2BA, LAS3BA, and/or EROMBA)
- PCI Base Address (PCIBAR2, PCIBAR3, PCIBAR4, PCIBAR5, and/or PCIERBAR)

A fourth register, the Bus Region Descriptor register for PCI-to-Local Accesses (LAS0BRD, LAS1BRD, LAS2BRD, LAS3BRD, and/or EROMBRD), defines the Local Bus characteristics for the PCI Target regions (refer to Figure 4-5).

Each PCI-to-Local Address space is defined as part of reset initialization (refer to Section 4.2.1.7.1). These Local Bus characteristics can be modified at any time before actual data transactions.

4.2.1.7.1 PCI Target Local Bus Initialization

Range—Specifies the PCI Address bits to use for decoding a PCI access to Local Bus space. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to address bit 31. Write 1 to all bits required to be included in decode, and 0 to all others.

Remap PCI-to-Local Addresses into a Local Address Space—Bits in this register remap (replace) the PCI Address bits used in decode as the Local Address bits.

Local Bus Region Descriptor—Specifies the Local Bus characteristics.

4.2.1.7.2 PCI Target Initialization

After a PCI reset and serial EEPROM load, the software determines the amount of required address space by writing all ones (1) to a PCI Base Address register and then reading back the value. The PCI 9030 returns zeroes (0) in the Don't Care Address bits, effectively specifying the address space required, at which time the PCI software maps the Local Address space into the PCI Address space by programming the PCI Base Address register. (Refer to Figure 4-5.)

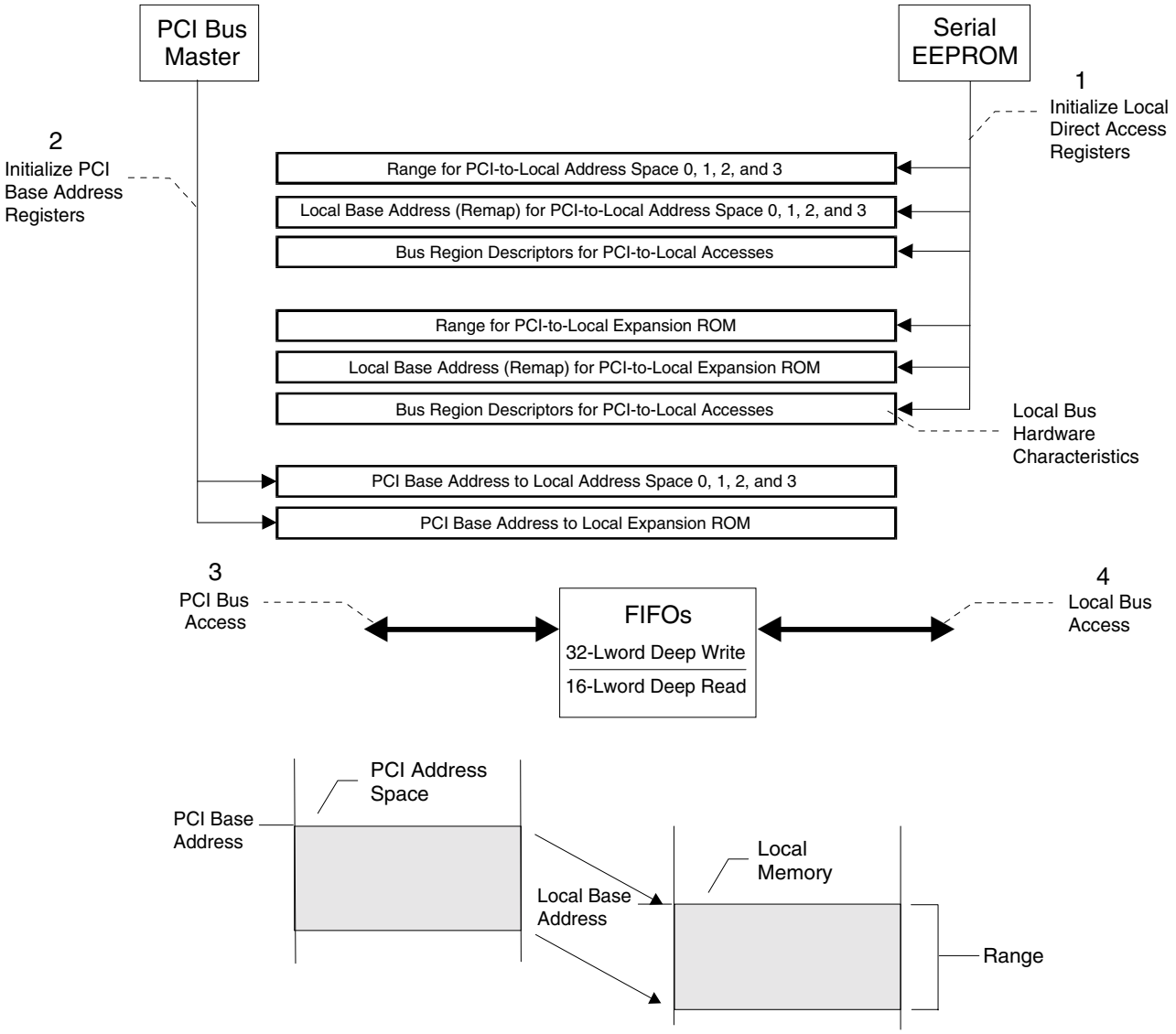


Figure 4-5. Local Bus PCI Target Access

4.2.1.7.3 PCI Target Byte Enables (Multiplexed Mode)

During a PCI Target transfer, each of five spaces (Space 0, Space 1, Space 2, Space 3, and Expansion ROM space) can be programmed to operate in an 8-, 16-, or 32-bit Local Bus width by encoding the Local Byte Enables (LBE[3:0]#).

LBE[3:0]# (PQFP—pins 55, 58-60; µBGA—pins M5, P5, M6, N6) are encoded, based on the configured bus width, as follows:

32-Bit Bus—The four-byte enables indicate which of the four bytes are active during a Data cycle:

- LBE3# Byte Enable 3—LAD[31:24]
- LBE2# Byte Enable 2—LAD[23:16]
- LBE1# Byte Enable 1—LAD[15:8]
- LBE0# Byte Enable 0—LAD[7:0]

16-Bit Bus—LBE3#, LBE1# and LBE0# are encoded to provide BHE#, LAD1, and BLE#, respectively:

- LBE3# Byte High Enable (BHE#)—LAD[15:8]
- LBE2# ***not used***
- LBE1# Address bit 1 (LAD1)
- LBE0# Byte Low Enable (BLE#)—LAD[7:0]

8-Bit Bus—LBE1# and LBE0# are encoded to provide LAD1 and LAD0, respectively:

- LBE3# ***not used***
- LBE2# ***not used***
- LBE1# Address bit 1 (LAD1)
- LBE0# Address bit 0 (LAD0)

4.2.1.7.4 PCI Target Example

A 1 MB Local Address Space, 12300000h through 123FFFFFh, is accessible from the PCI Bus at PCI addresses 78900000h through 789FFFFFh.

a. Local initialization software sets the Range and Local Base Address registers as follows:
   - **Range**—FFF00000h (1 MB, decode the upper 12 PCI Address bits)
   - **Local Base Address (Remap)**—123XXXXXh, (Local Base Address for PCI-to-Local accesses) [Space Enable bit(s) must be set to be recognized by the PCI Host (LAS0BA[0]=1, LAS1BA[0]=1)]

b. PCI Initialization software writes all ones to the PCI Base Address, then reads it back.
   - The PCI 9030 returns a value of FFF00000h, at which time the PCI software writes to the PCI Base Address register(s).
   - **PCI Base Address**—789XXXXXh (PCI Base Address for Access to the Local Address Space registers, PCIBAR2 and PCIBAR3).

For a PCI Direct access to the Local Bus, the PCI 9030 has a 32-Lword (128-byte) Write FIFO and a 16-Lword (64-byte) Read FIFO. The FIFOs enable the Local Bus to operate independent of the PCI Bus. The PCI 9030 can be programmed to return a Retry response or to throttle TRDY# for PCI Bus transactions attempting to write to the PCI 9030 Local Bus when the FIFO is full.

For PCI Read transactions from the Local Bus, the PCI 9030 holds off TRDY# while gathering data from the Local Bus. For Read accesses mapped to PCI Memory space, the PCI 9030 prefetches up to 16 Lwords (in Continuous Prefetch mode) from the Local Bus. Unused Read data is flushed from the FIFO. For Read accesses mapped to PCI I/O space, the PCI 9030 does not prefetch Read data. Rather, it breaks each read of a Burst cycle into a Single Address/Data cycle on the Local Bus.

The PCI Target Retry Delay Clocks bits (CNTRL[22:19]; 50h) can be used to program the period of time in which the PCI 9030 holds off TRDY#. The PCI 9030 issues a Retry to the PCI Bus Transaction Master when the programmed time period expires. This occurs when the PCI 9030 cannot gain Local Bus control and return TRDY# within the programmed time period or the Local Bus is slowly emptying the Write FIFO, and filling the Read FIFO.

4.2.1.7.5 PCI Target Byte Enables (Non-Multiplexed Mode)

During a PCI Target transfer, each of five spaces (Space 0, Space 1, Space 2, Space 3, and Expansion ROM space) can be programmed to operate in an 8-, 16-, or 32-bit Local Bus width by encoding the Local Byte Enables (LBE[3:0]#).

LBE[3:0]# (PQFP—pins 55, 58-60; µBGA—pins M5, P5, M6, N6) are encoded, based on the configured bus width, as follows:

32-Bit Bus—The four-byte enables indicate which of the four bytes are active during a Data cycle:

- LBE3# Byte Enable 3—LD[31:24]
- LBE2# Byte Enable 2—LD[23:16]
- LBE1# Byte Enable 1—LD[15:8]
- LBE0# Byte Enable 0—LD[7:0]

16-Bit Bus—LBE3#, LBE1# and LBE0# are encoded to provide BHE#, LA1, and BLE#, respectively:

- LBE3# Byte High Enable (BHE#)—LD[15:8]
- LBE2# ***not used***
- LBE1# Address bit 1 (LA1)
- LBE0# Byte Low Enable (BLE#)—LD[7:0]

8-Bit Bus—LBE1# and LBE0# are encoded to provide LA1 and LA0, respectively:

- LBE3# ***not used***
- LBE2# ***not used***
- LBE1# Address bit 1 (LA1)
- LBE0# Address bit 0 (LA0)

4.3 RESPONSE TO FIFO FULL OR EMPTY

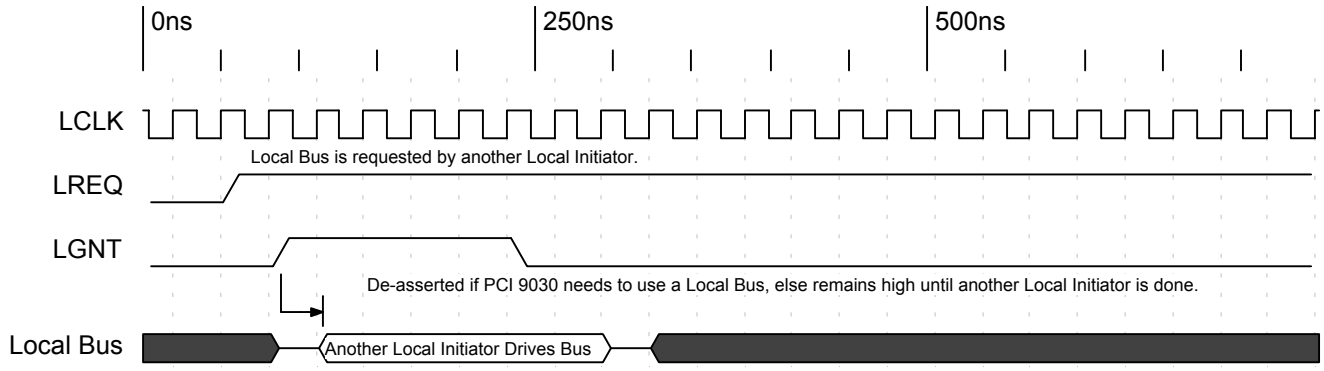
Table 4-1 lists the PCI 9030 response to full or empty FIFOs.

Table 4-1. Response to FIFO Full or Empty

Mode	Direction	FIFO	PCI Bus	Local Bus
PCI Target Write	PCI-to-Local	Full	Disconnect or Throttle TRDY#[1]	De-assert LGNT if Local Bus is busy and wait for LREQ to be de-asserted
		Empty	Normal	Normal, assert BLAST#
PCI Target Read	Local-to-PCI	Full	Normal	Normal, assert BLAST#
		Empty	Disconnect or Throttle TRDY#[1]	Normal

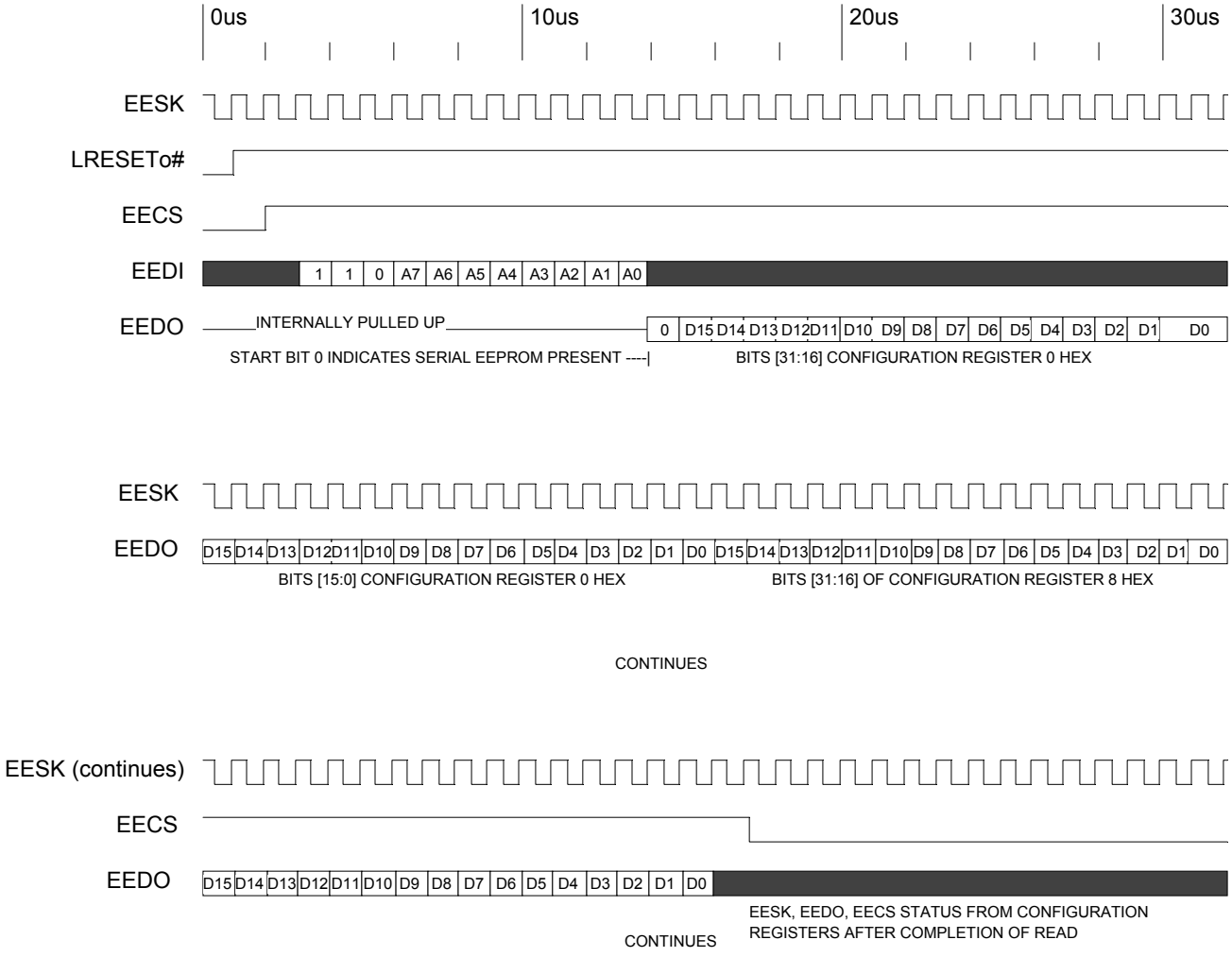
1. Throttle TRDY# depends on the PCI Target Retry Delay Clocks (CNTRL[22:19]).

4.4 TIMING DIAGRAMS

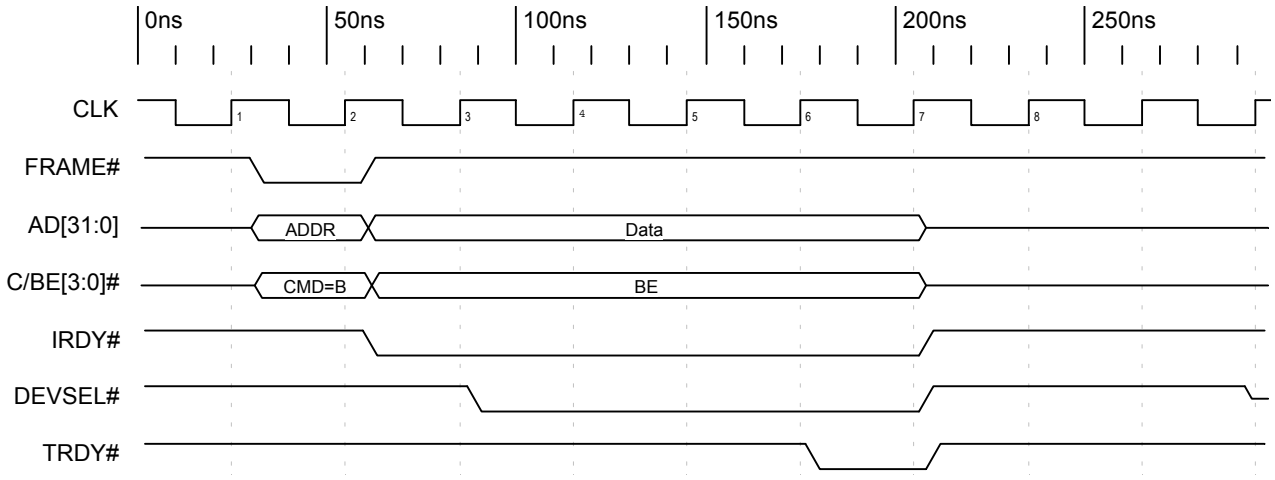


Timing Diagram 4-1. Local Bus Arbitration from the PCI 9030 by Another Local Bus Initiator (LREQ and LGNT)

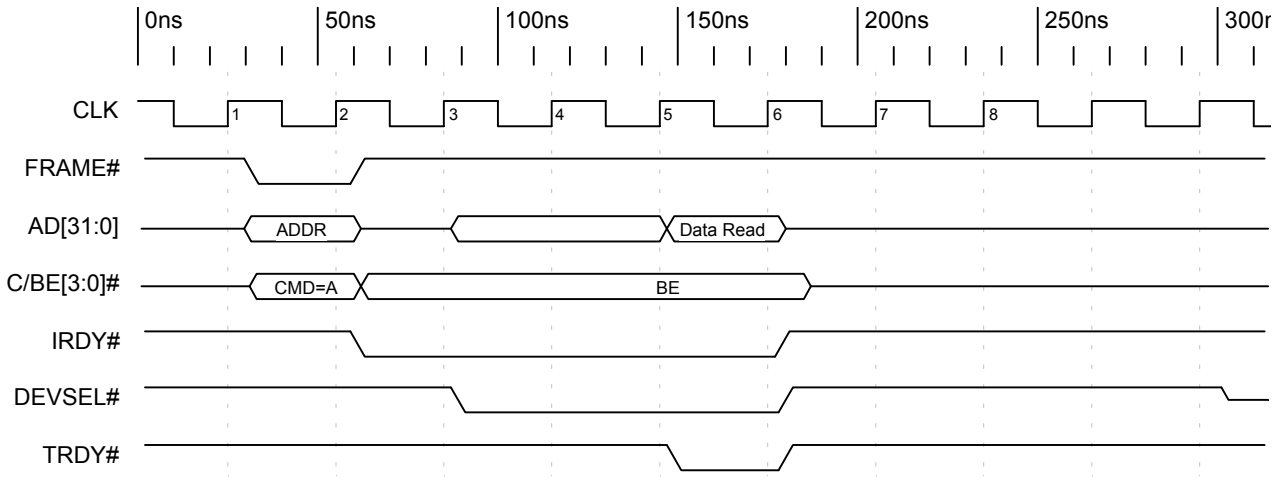
4.4.1 Serial EEPROM and Configuration Initialization Timing Diagrams



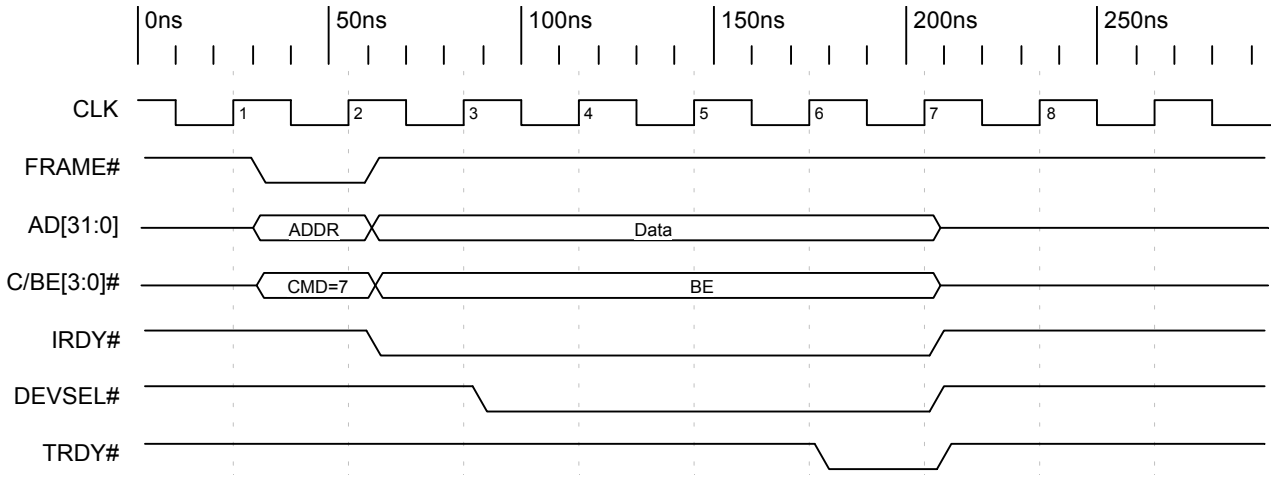
Timing Diagram 4-2. Initialization from Serial EEPROM (2K or 4K Bit)



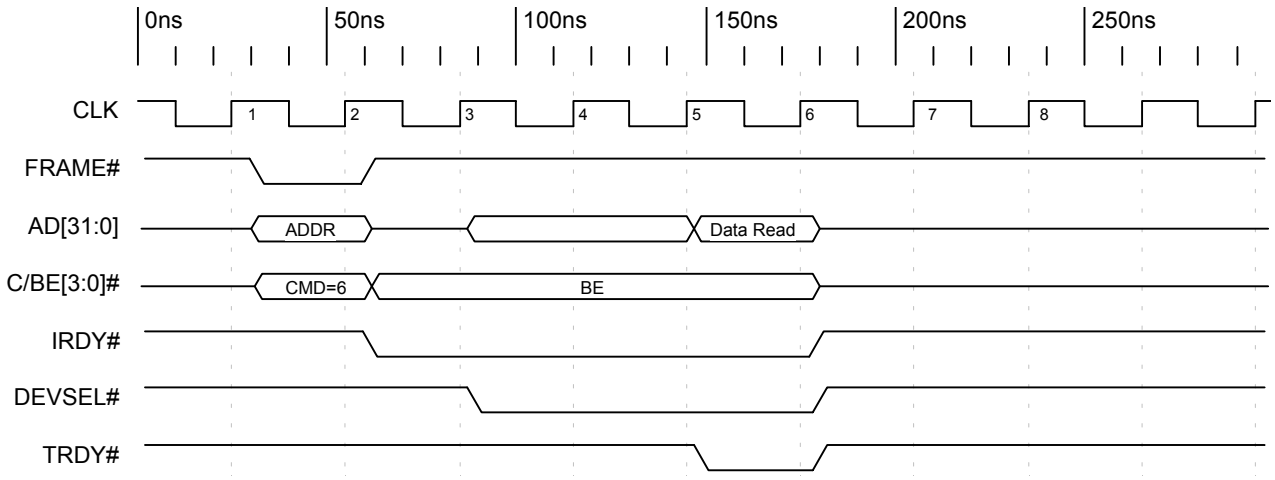
Timing Diagram 4-3. PCI Configuration Write to PCI Configuration Register



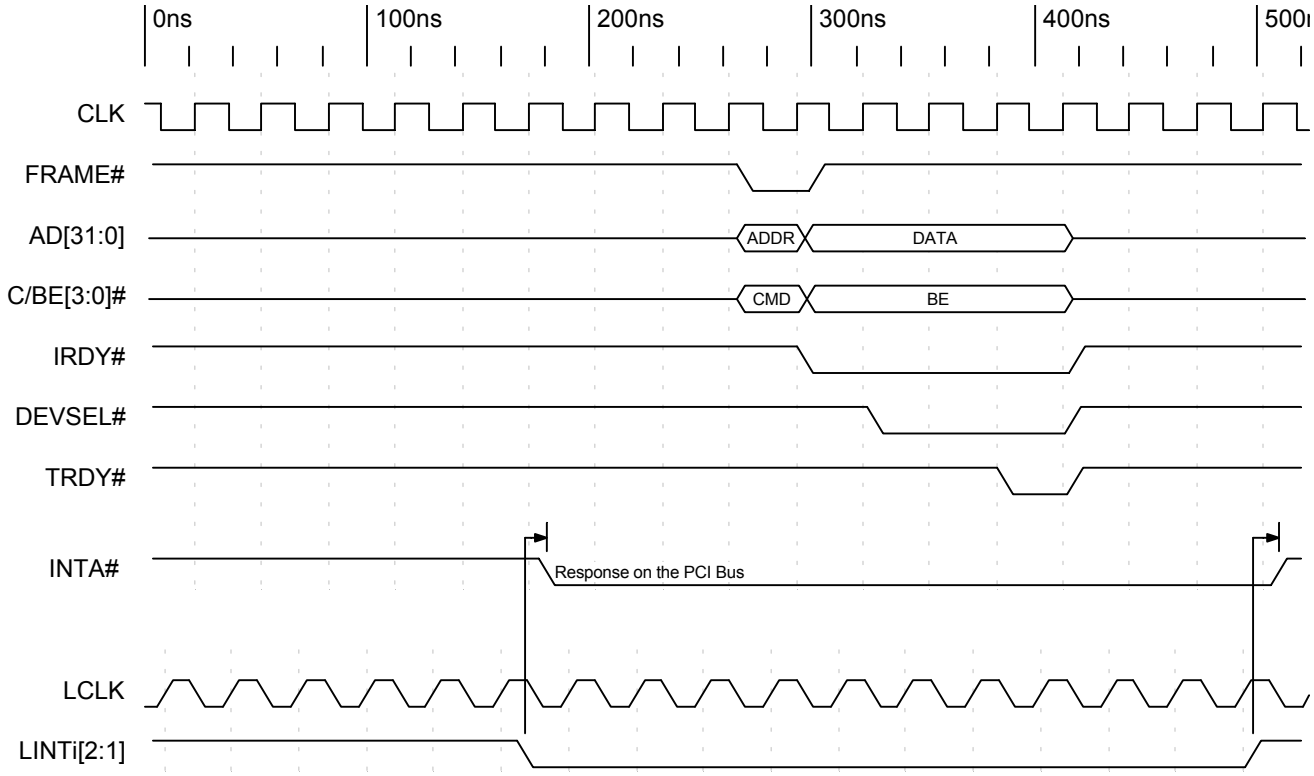
Timing Diagram 4-4. PCI Configuration Read from PCI Configuration Register



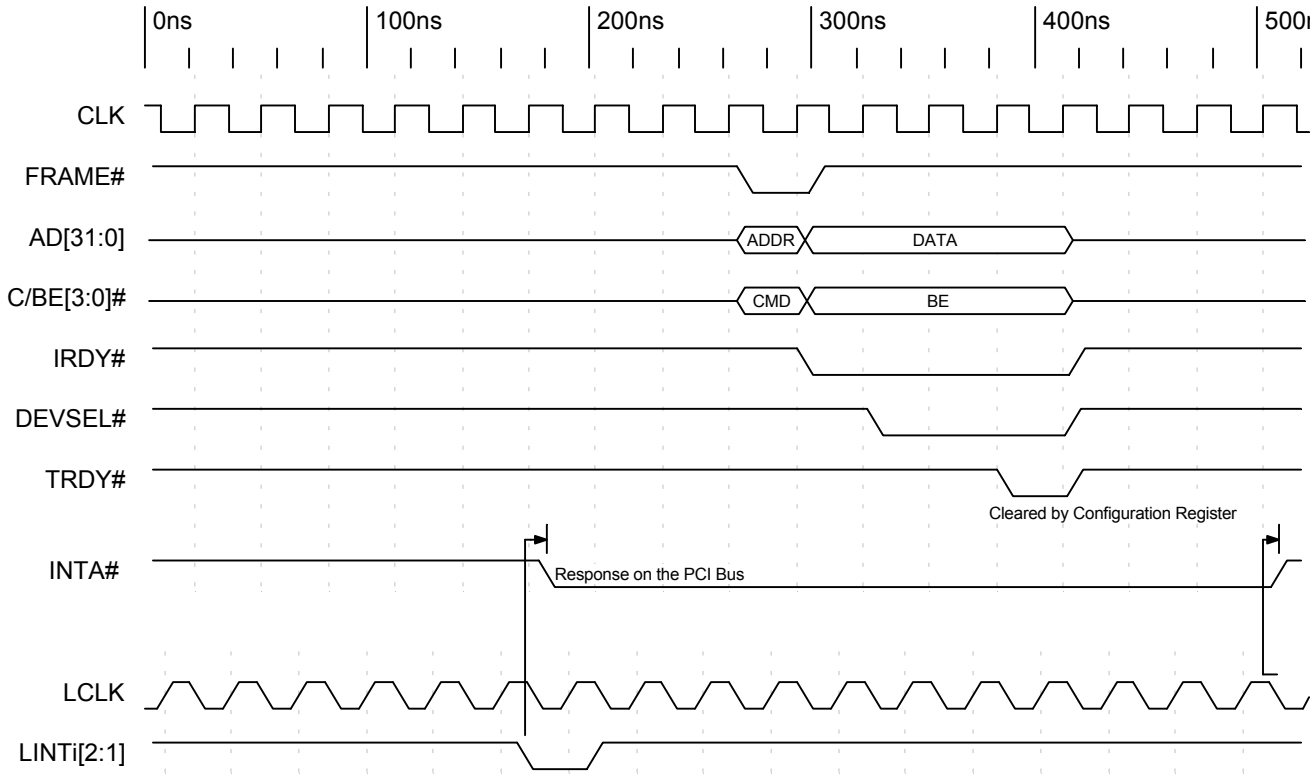
Timing Diagram 4-5. PCI Memory Write to Local Configuration Register



Timing Diagram 4-6. PCI Memory Read from Local Configuration Register

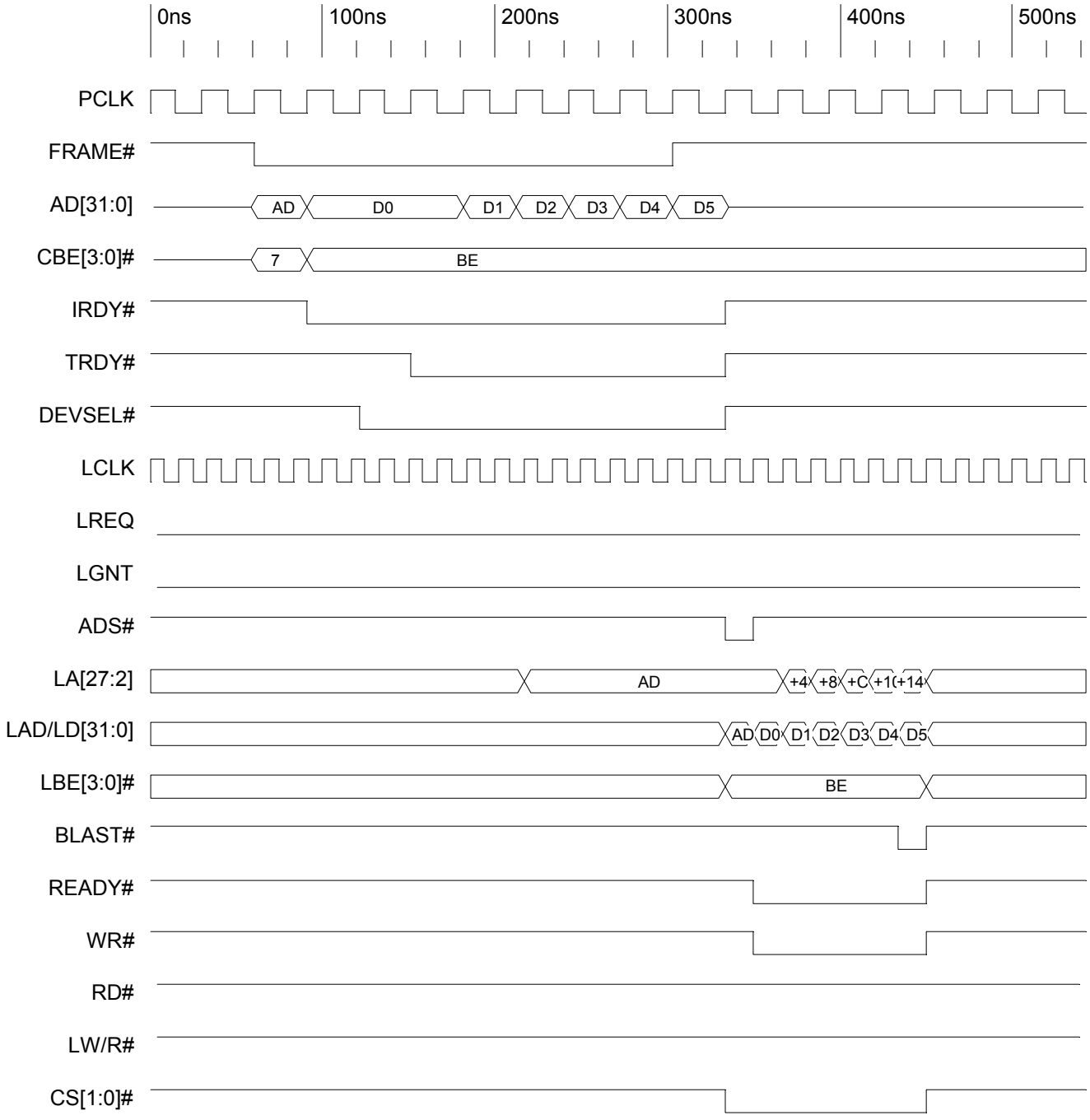


Timing Diagram 4-7. Local Level Triggered Interrupt Asserting PCI Interrupt



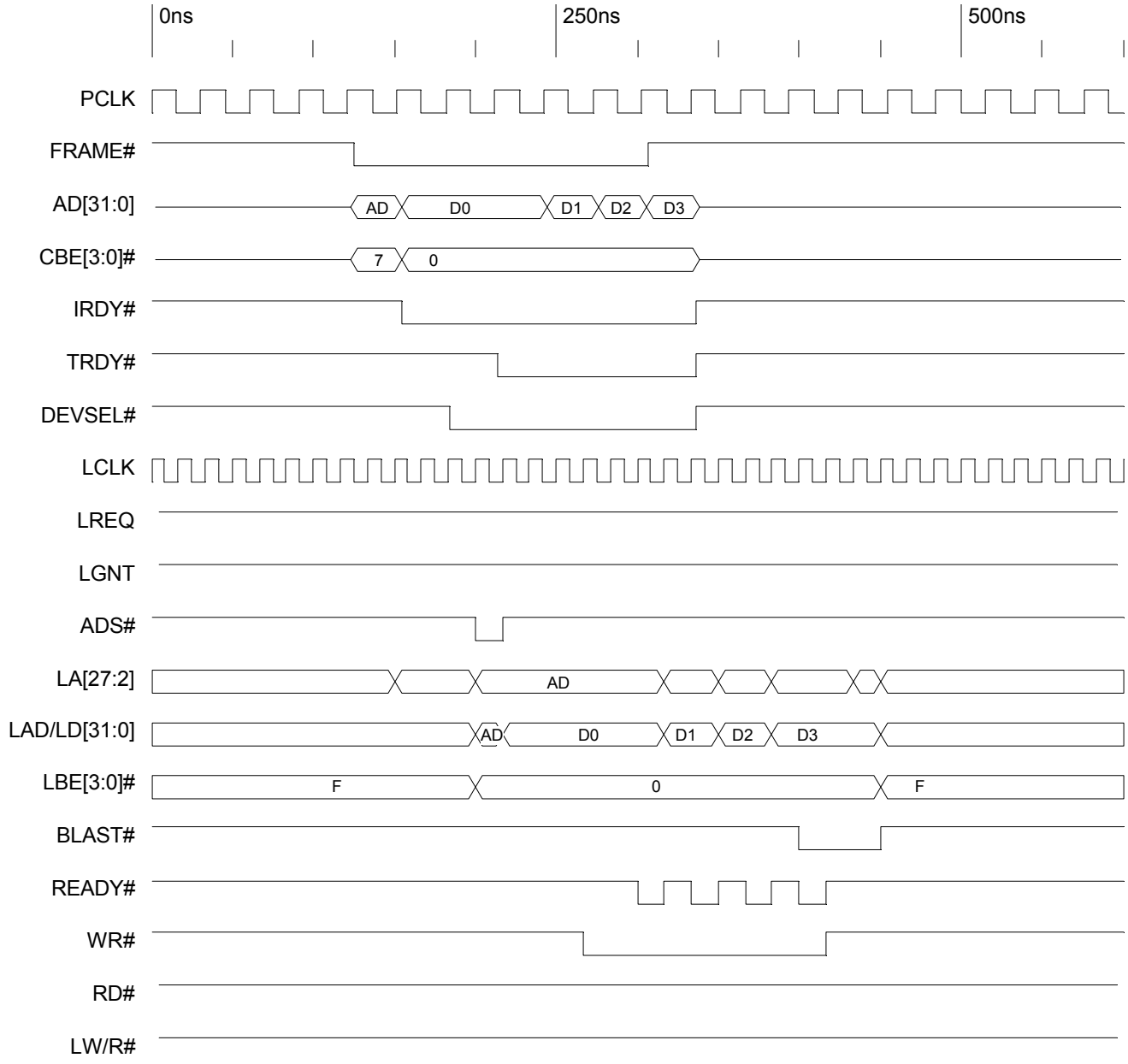
Timing Diagram 4-8. Local Edge Triggered Interrupt Asserting PCI Interrupt

4.4.2 PCI Target, Multiplexed and Non-Multiplexed Modes



Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

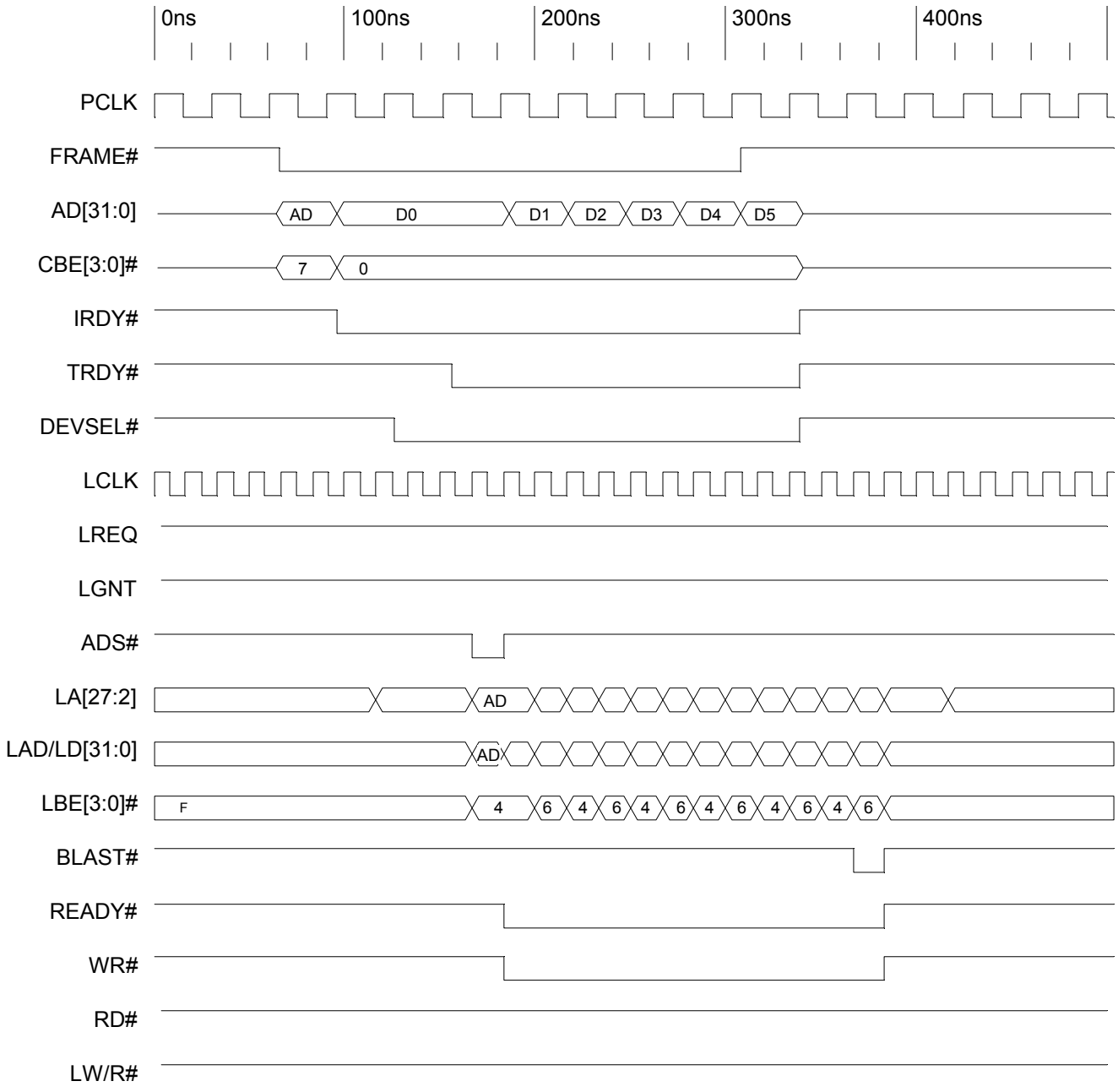
Timing Diagram 4-9. PCI Target Burst Write with Delayed Write and SRAM Chip Select Enabled



Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

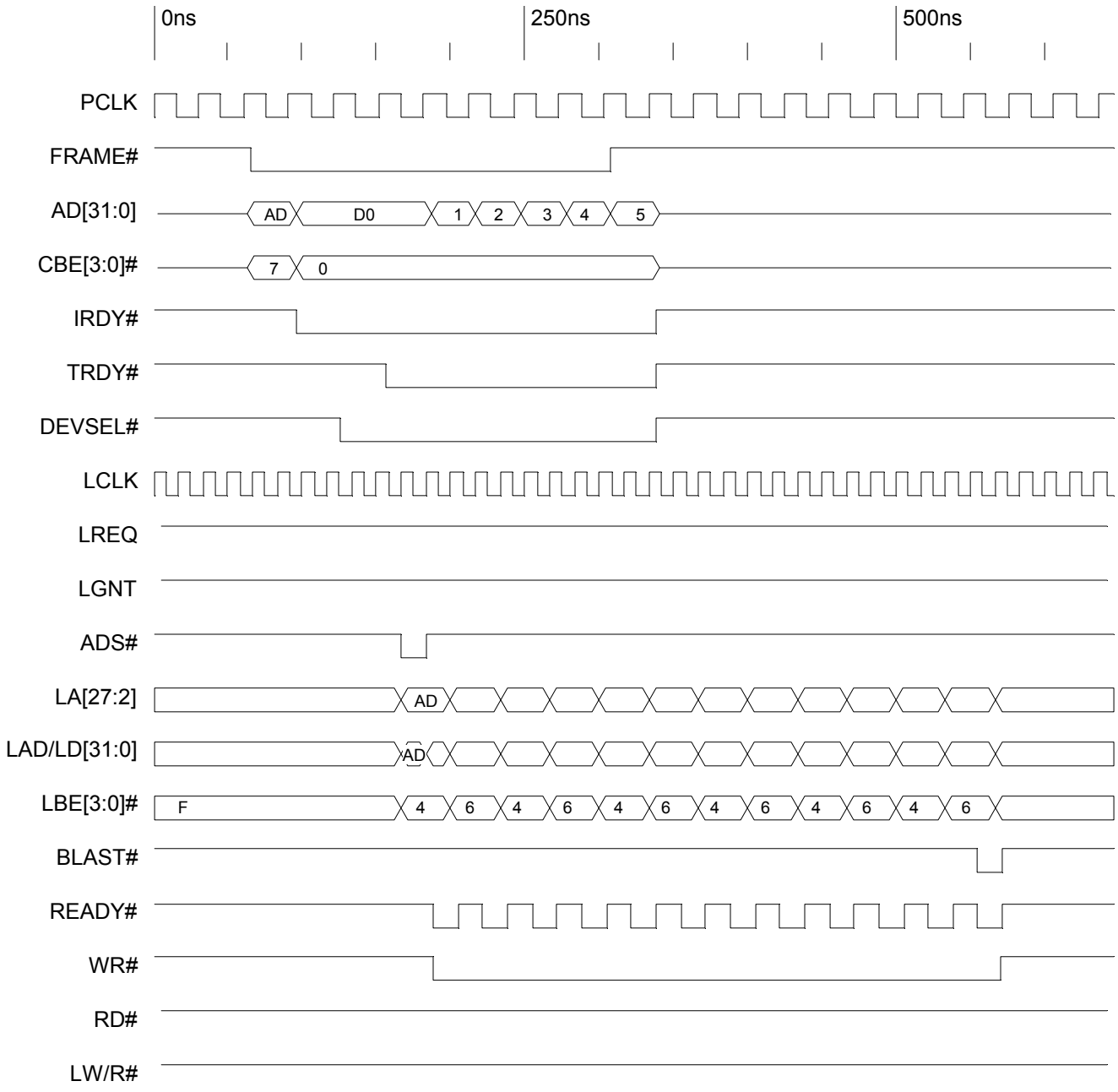
Five Address-to-Data Wait States; One Data-to-Data Wait State;
Three Write Strobe Wait States; Two Write Hold Wait States.

Timing Diagram 4-10. PCI Target Burst Write (32-Bit Local Bus)



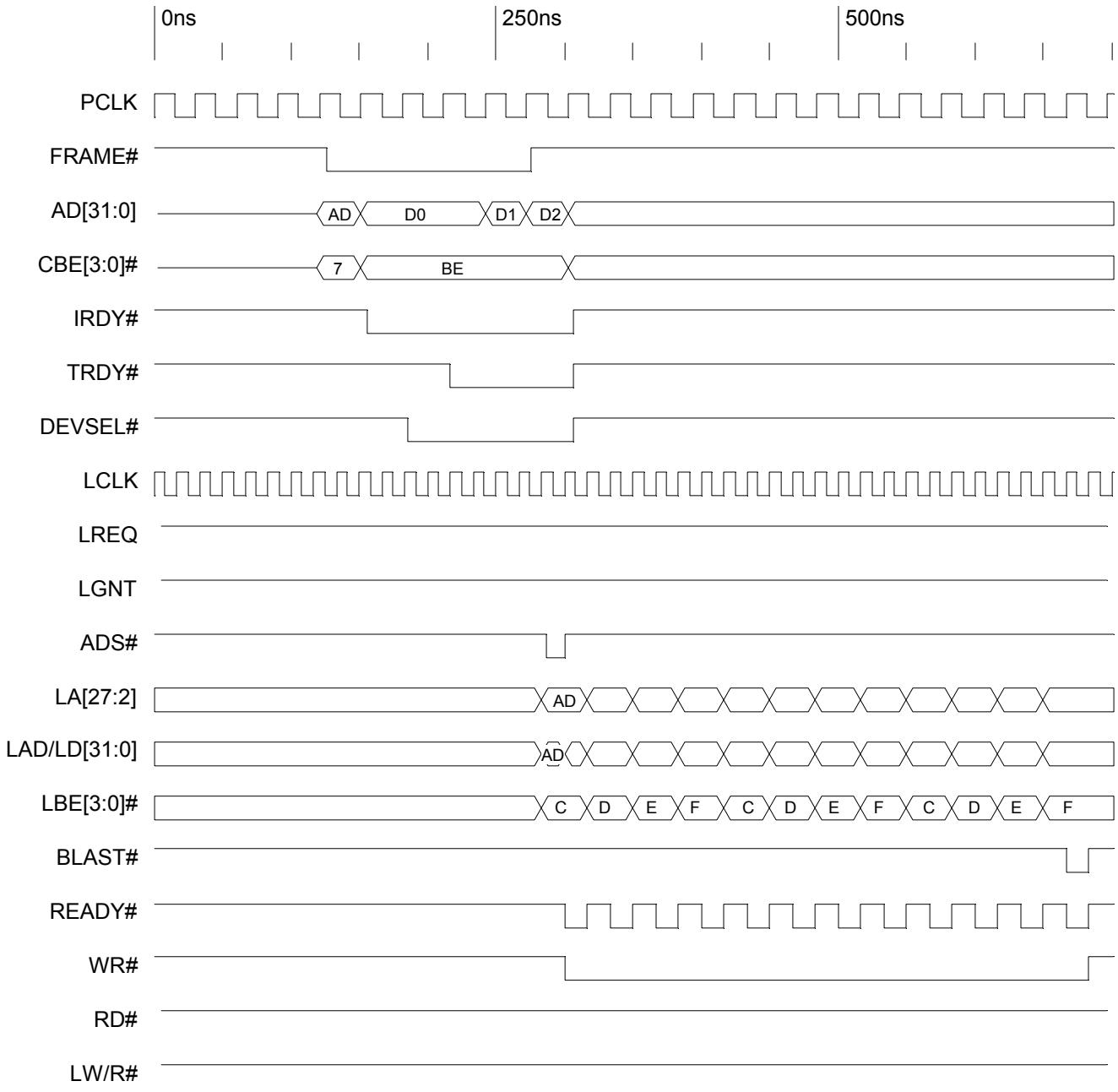
Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-11. PCI Target Burst Write (16-Bit Local Bus), No Wait States



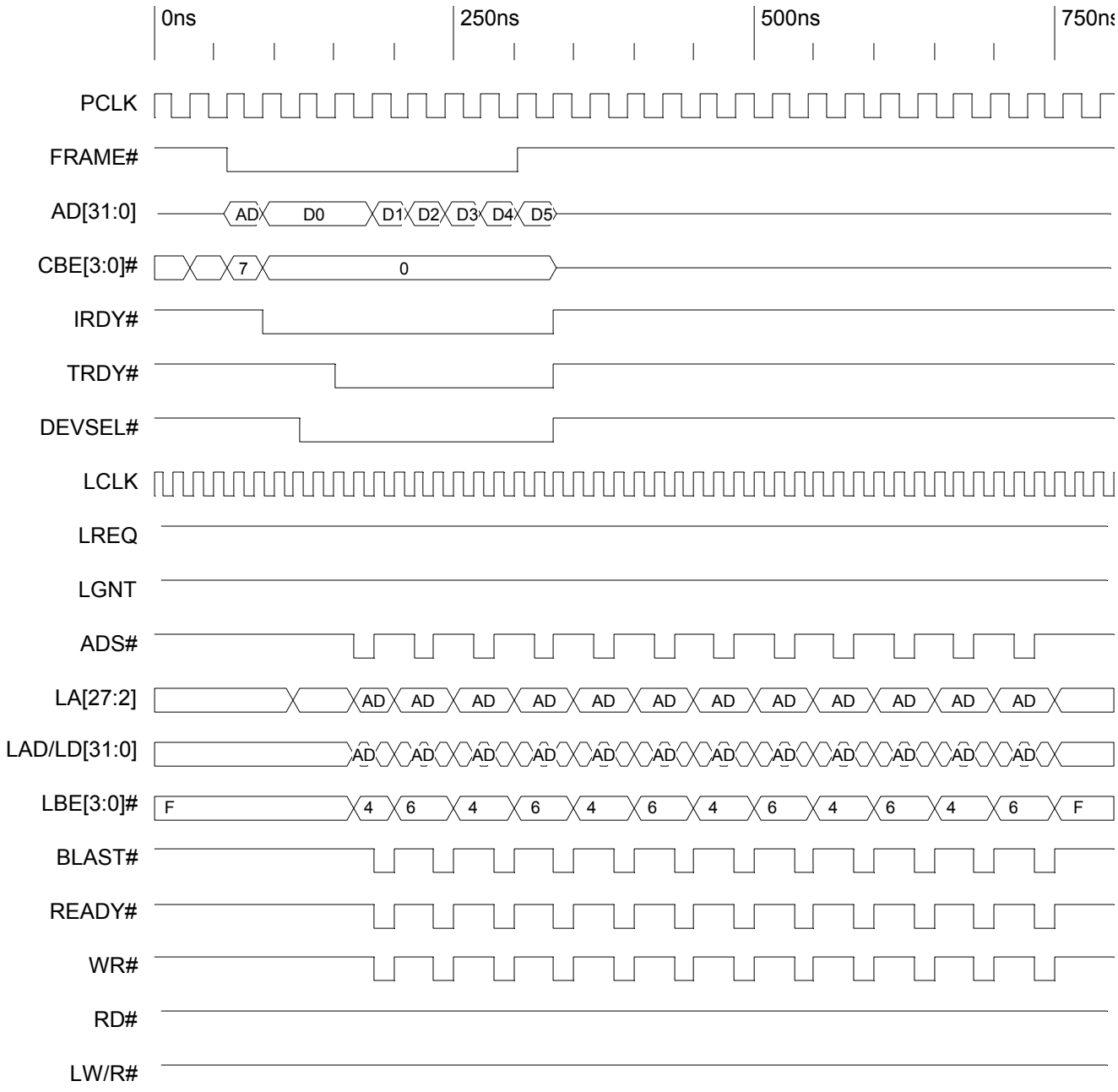
Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-12. PCI Target Burst Write (16-Bit Local Bus), One Data-to-Data Wait State



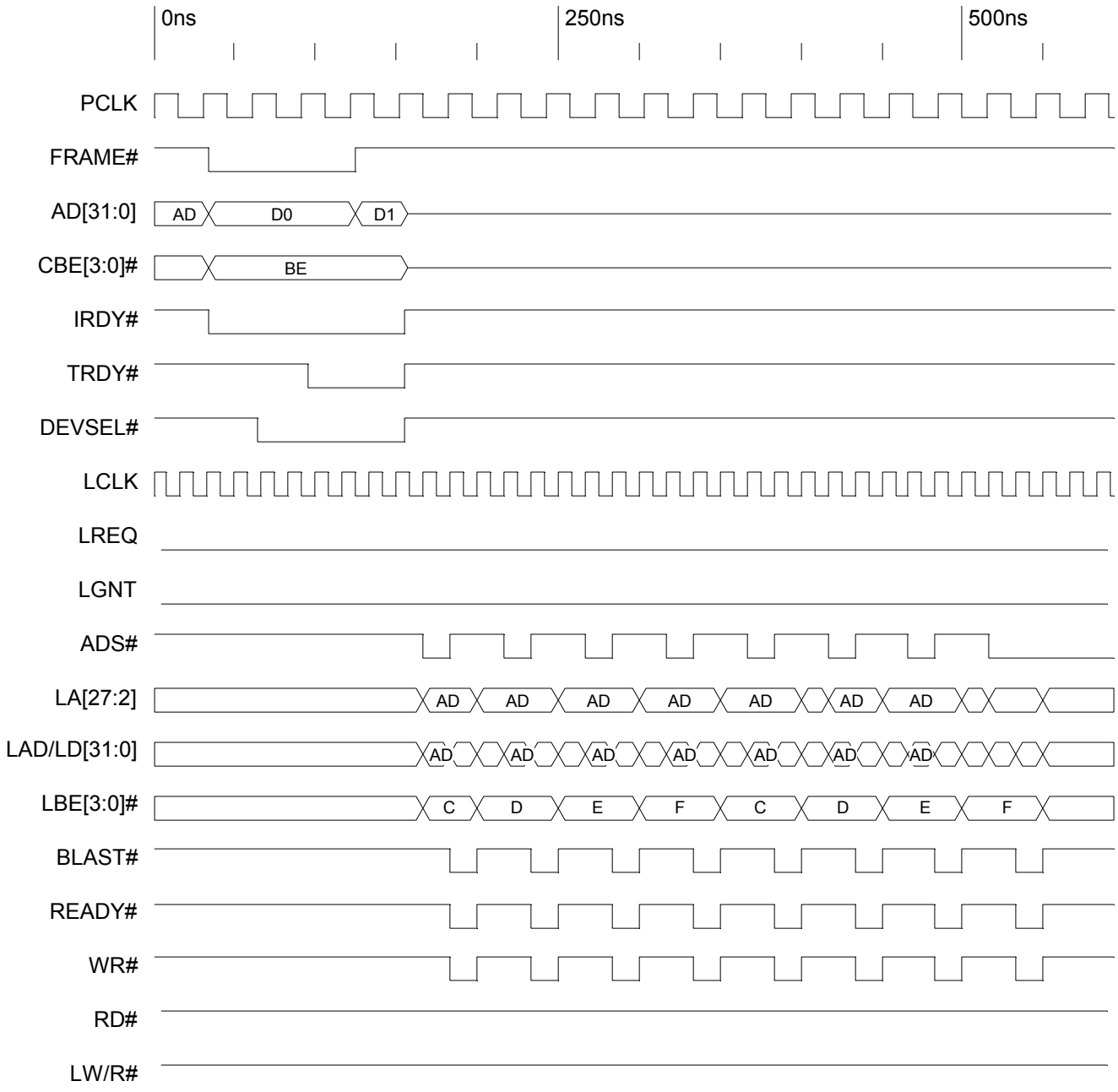
Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-13. PCI Target Burst Writes (8-Bit Local Bus), One Data-to-Data Wait State



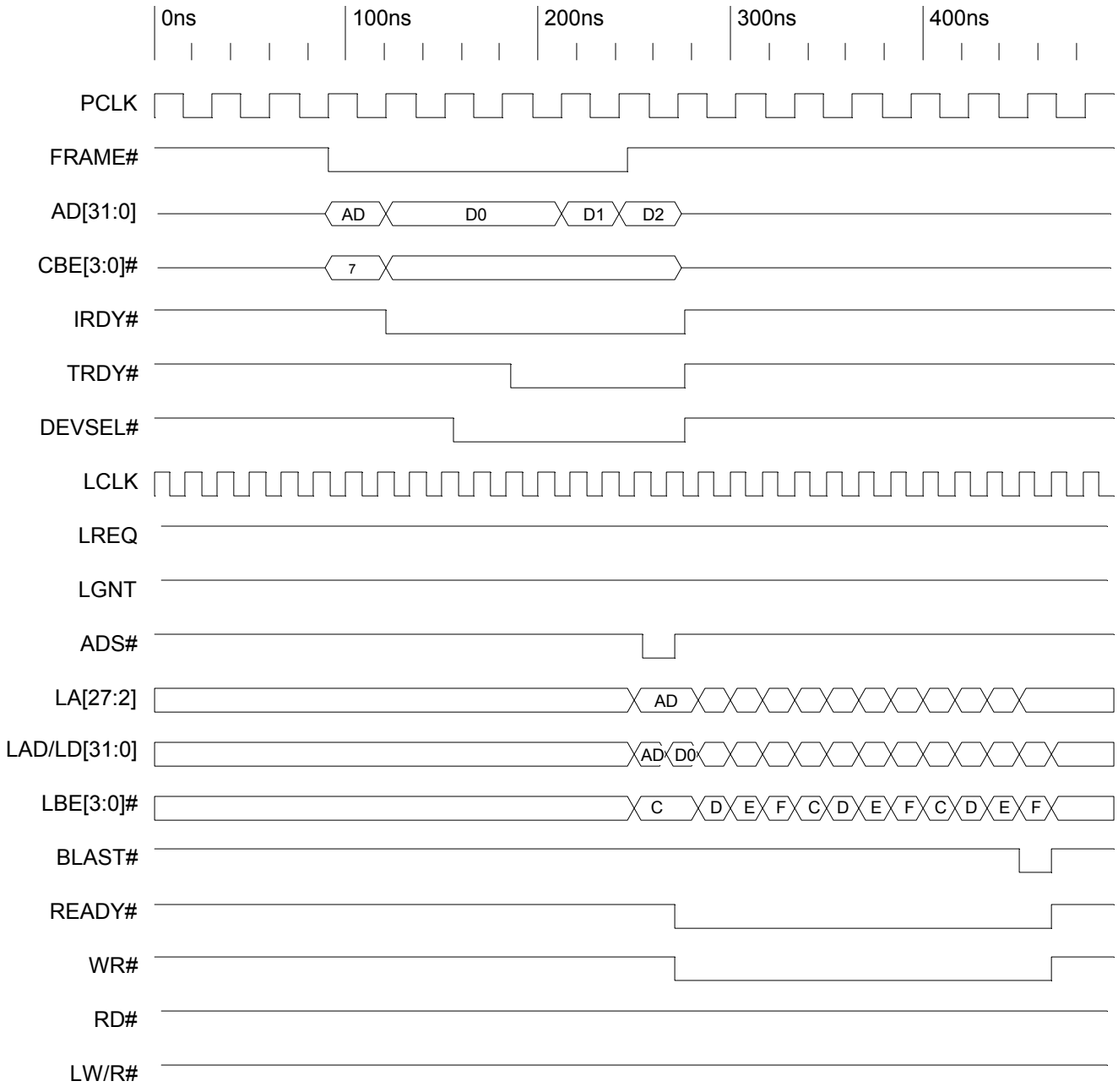
Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-14. PCI Target Single Writes (16-Bit Local Bus)



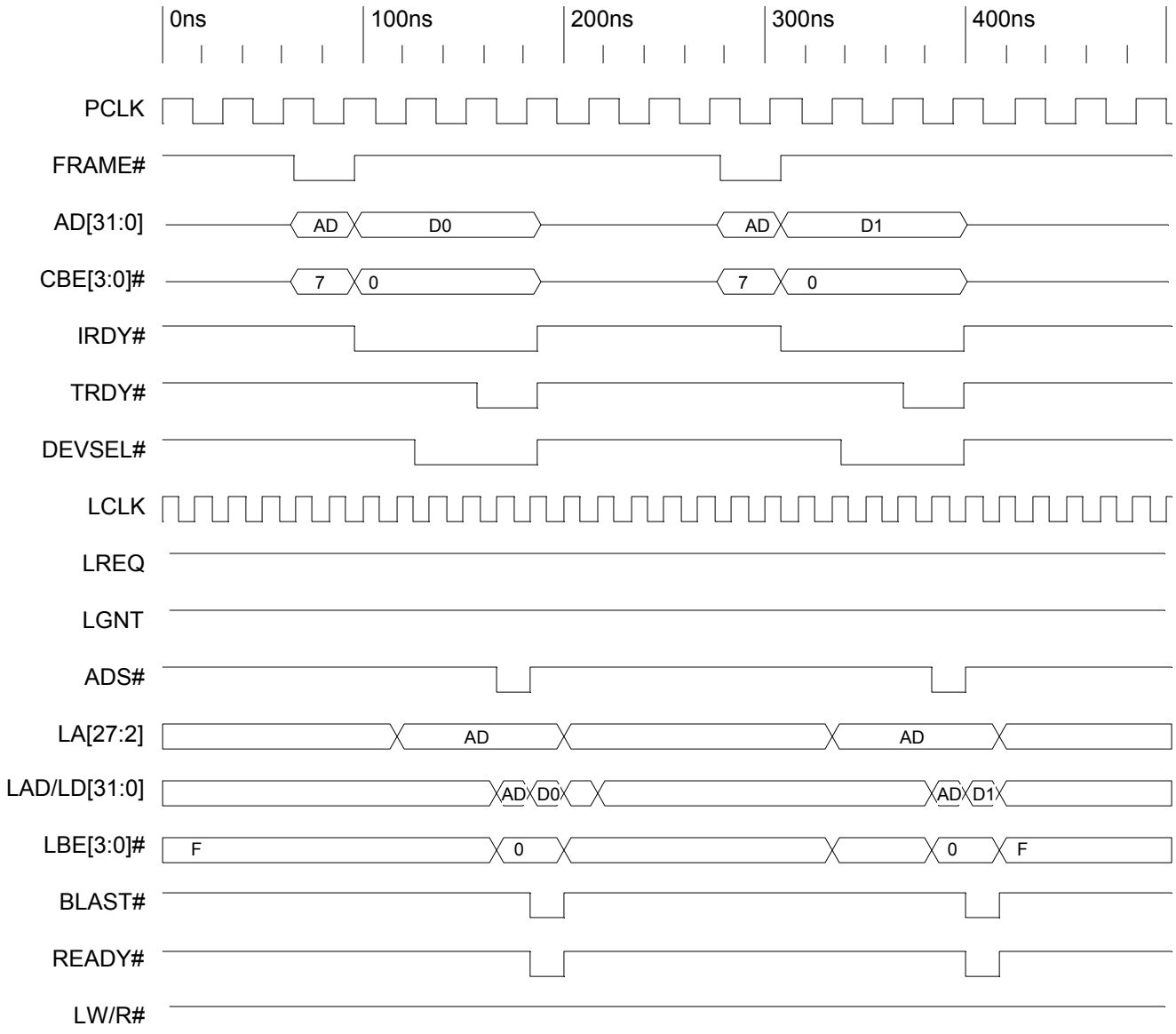
Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-15. PCI Target Single Writes (8-Bit Local Bus)



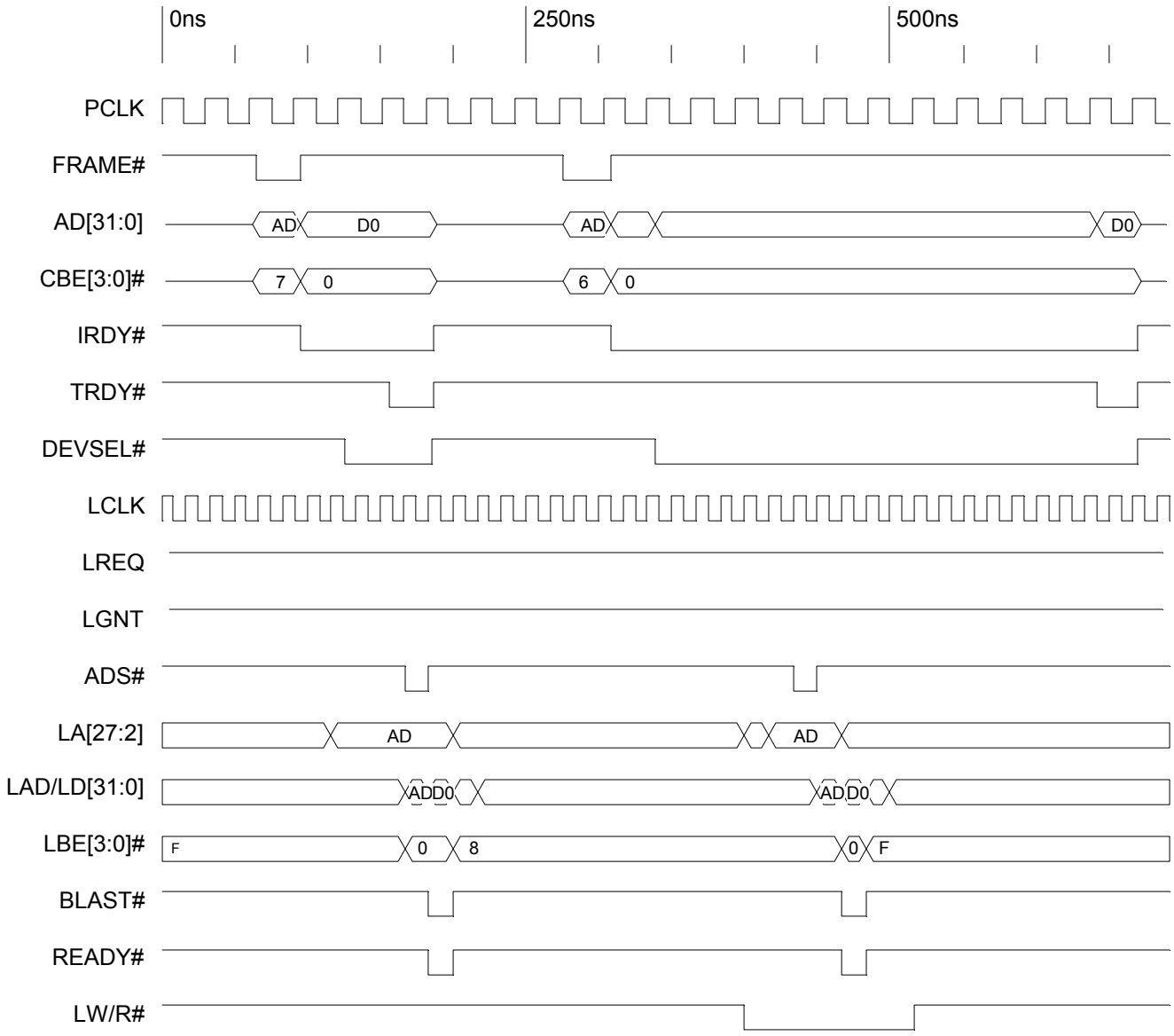
Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-16. PCI Target Single Writes (8-Bit Local Bus), No Wait States



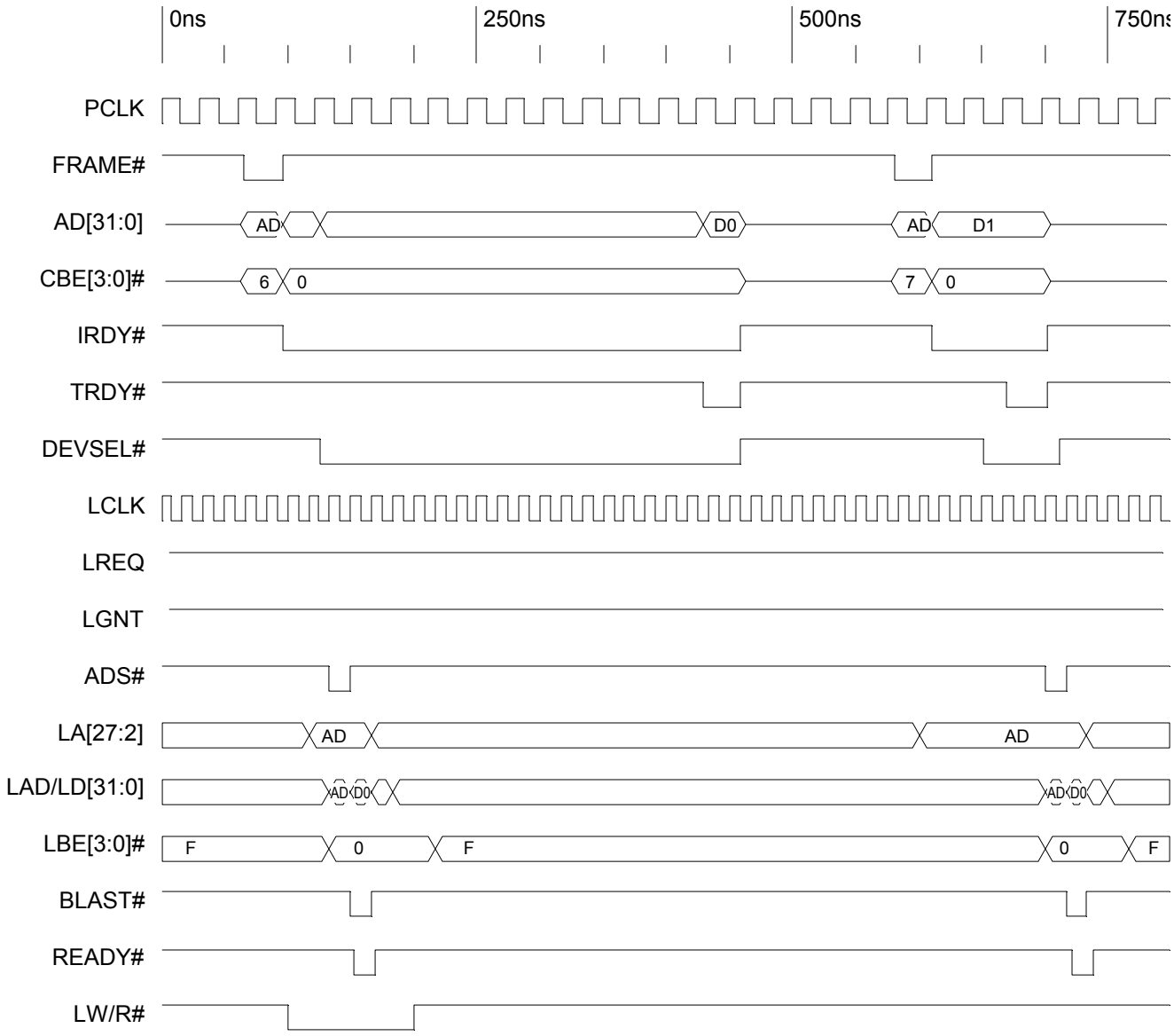
Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-17. PCI Target Back-to-Back Single Writes



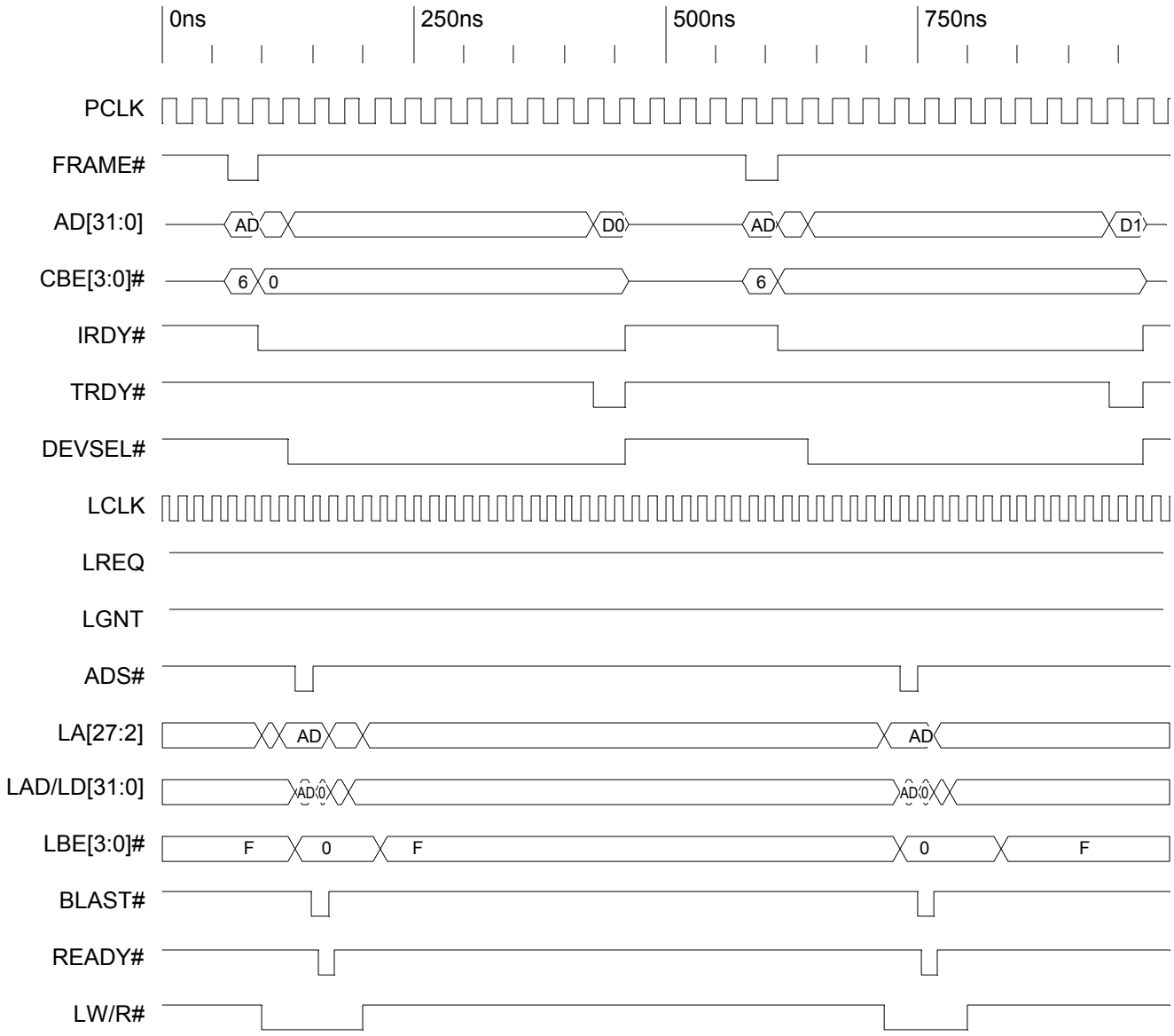
Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-18. PCI Target Back-to-Back Write Followed by a Read



Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

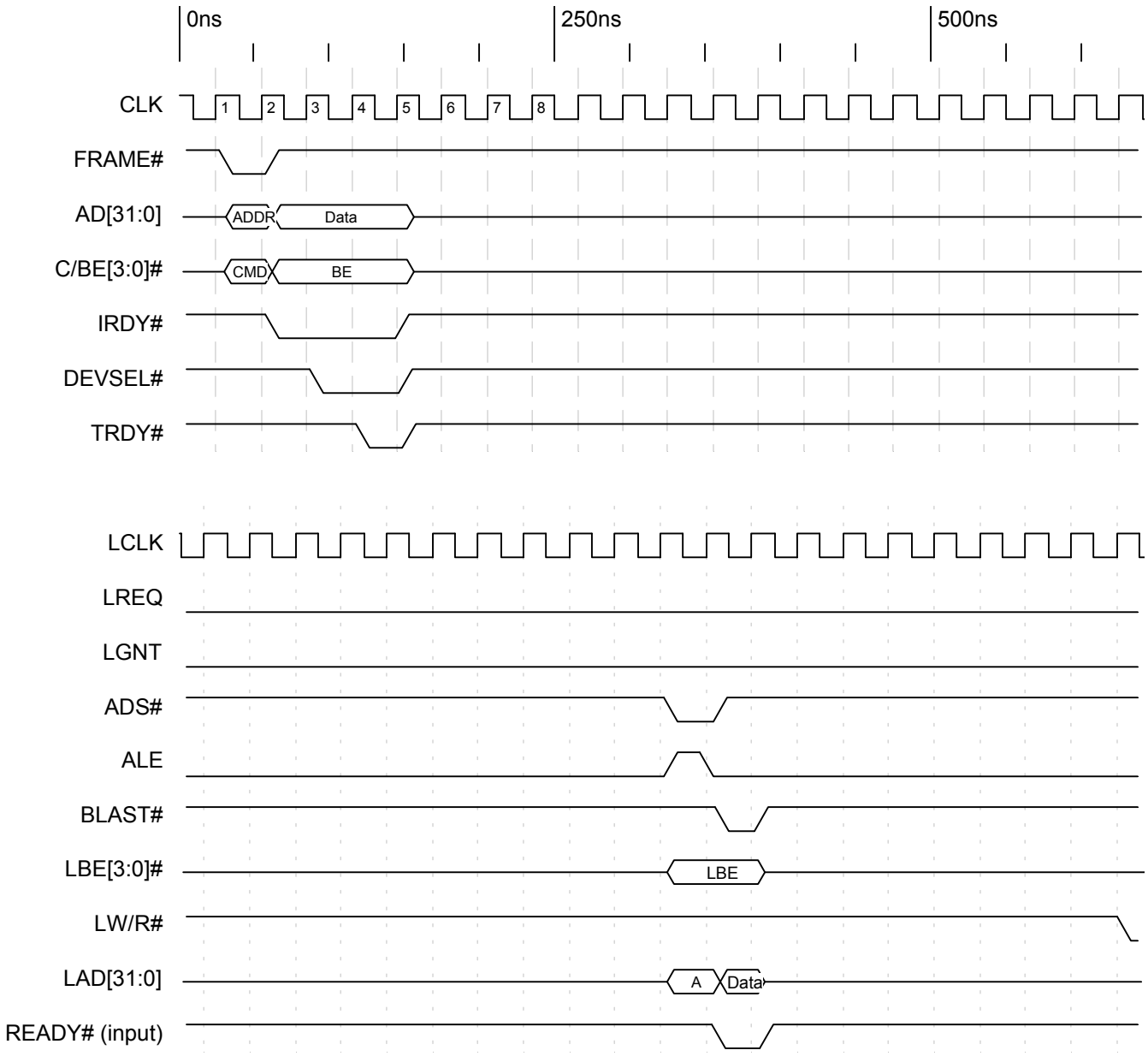
Timing Diagram 4-19. PCI Target Back-to-Back Read Followed by a Write



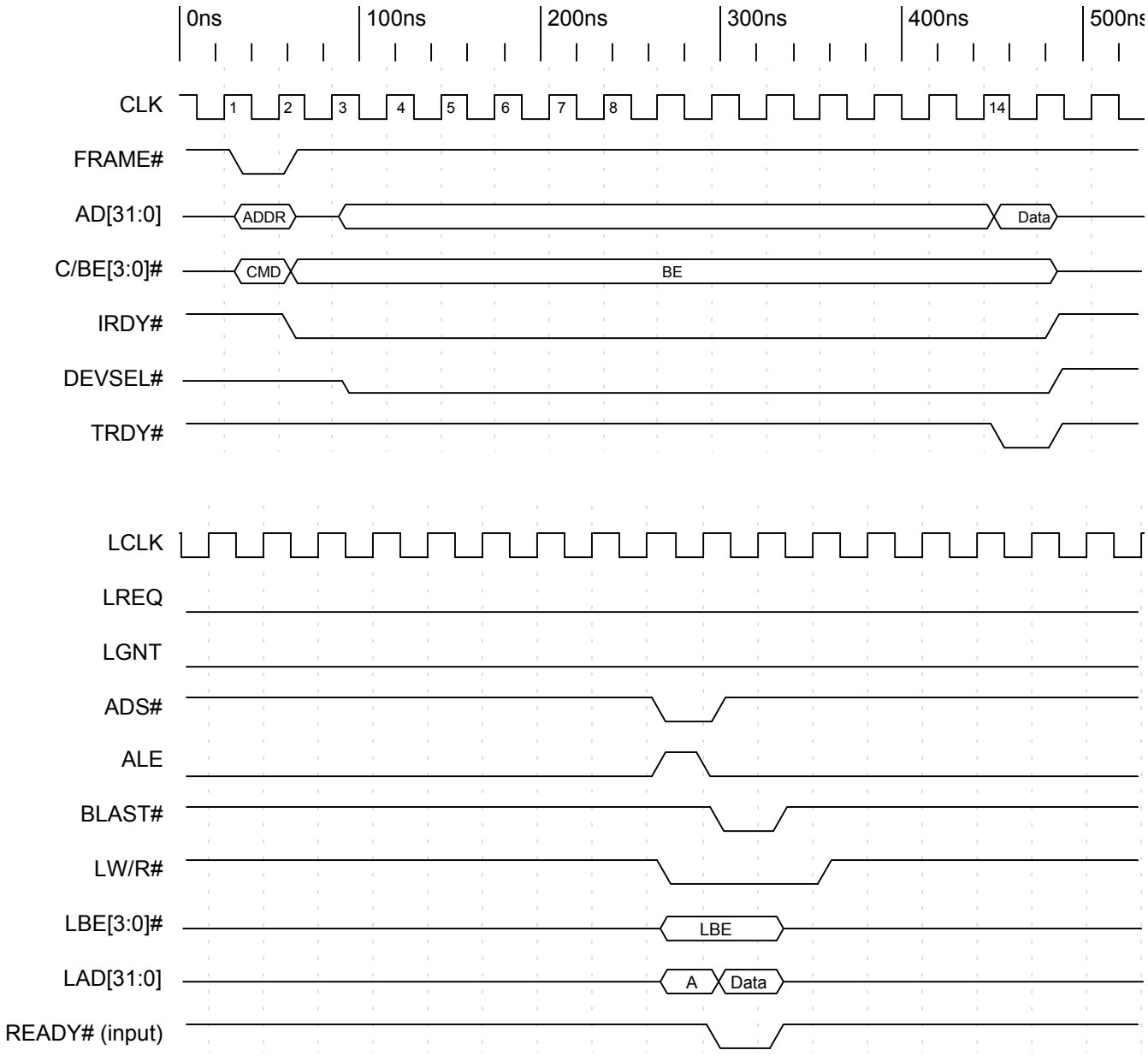
Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-20. PCI Target Back-to-Back Reads

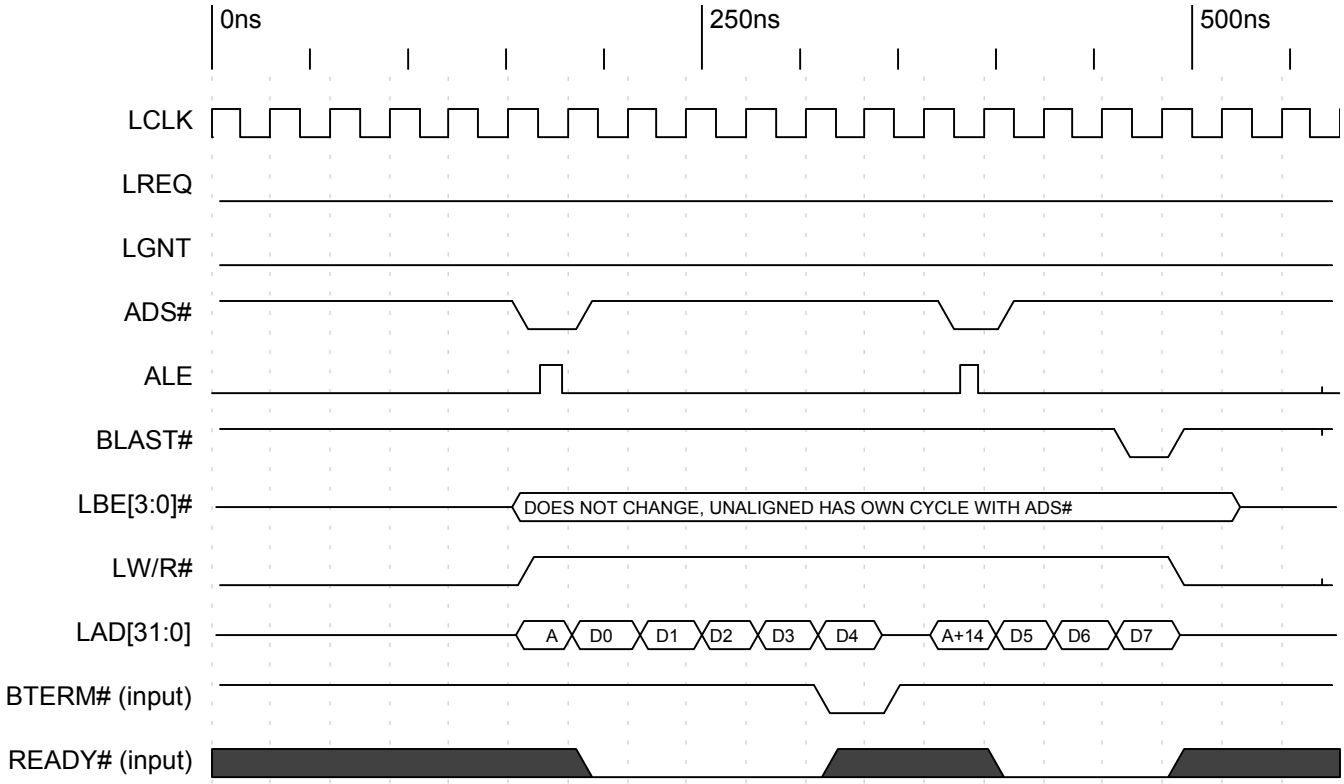
4.4.2.1 PCI Target, Multiplexed Mode Only



Timing Diagram 4-21. PCI Target Single Write (32-Bit Local Bus), Multiplexed Mode Only



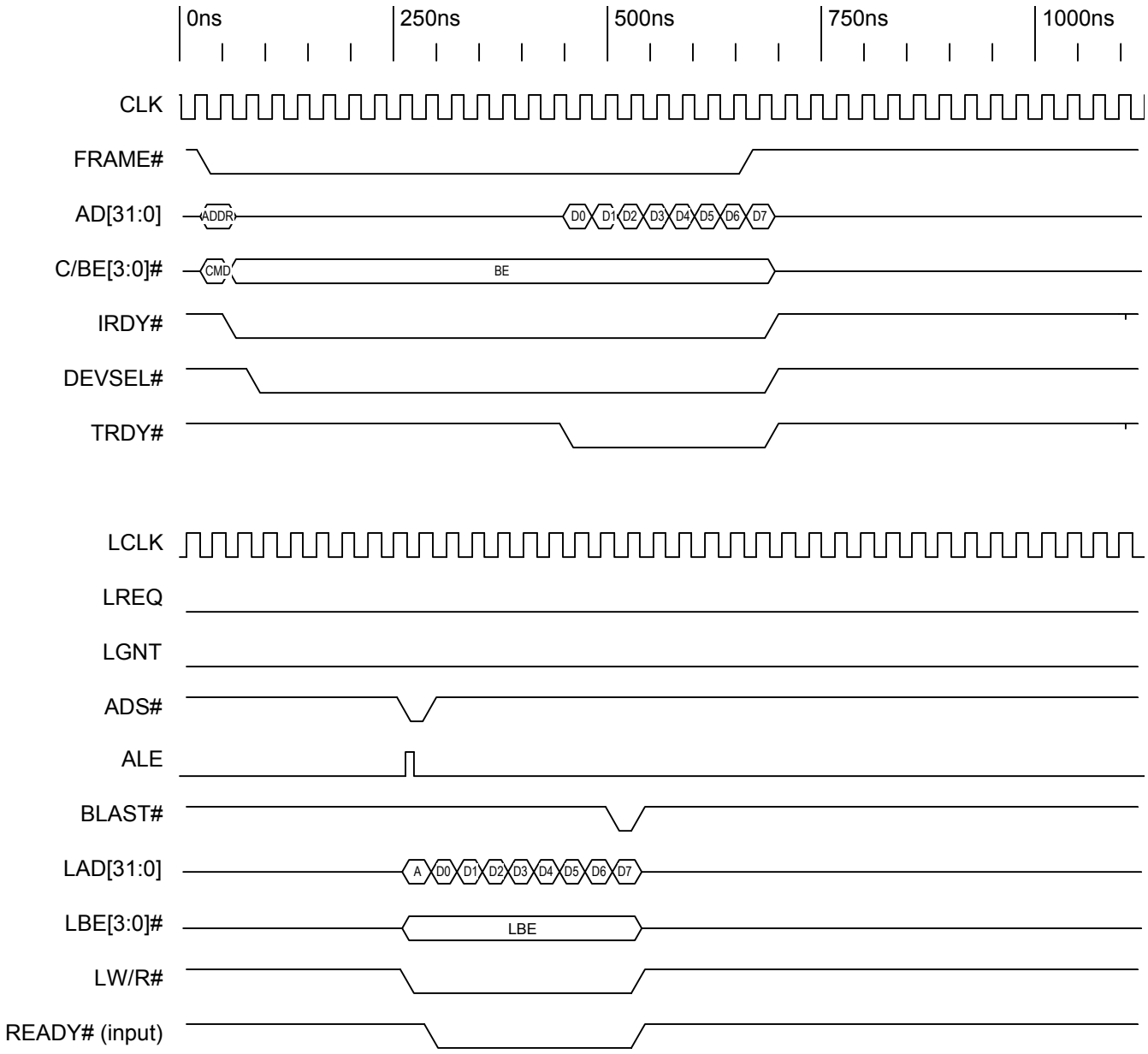
Timing Diagram 4-22. PCI Target Single Read (32-Bit Local Bus), Multiplexed Mode Only



Eight Lword Burst, no wait states, BTERM# (input) enabled, Burst enabled, 32-bit Local Bus.

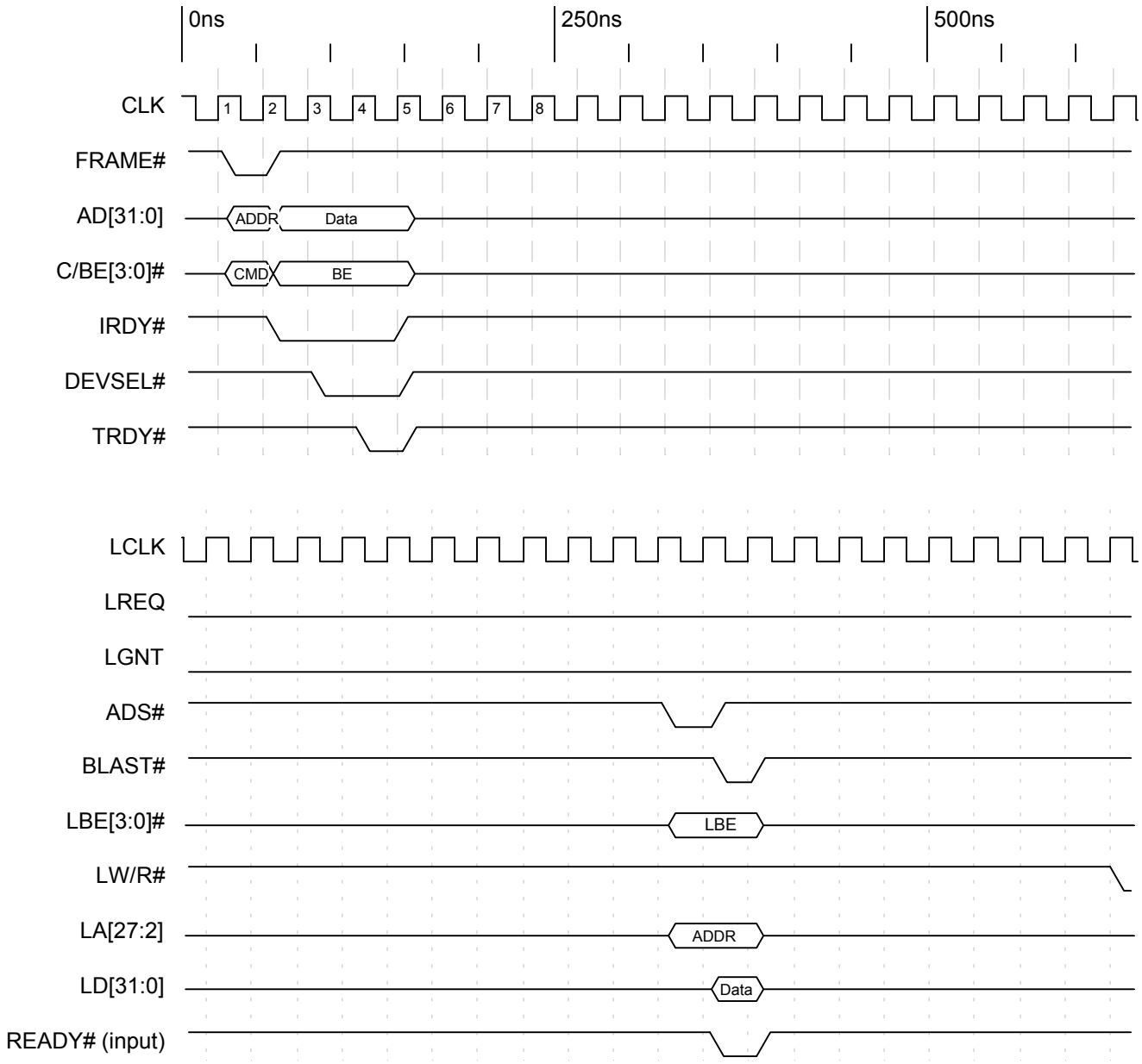
Note: If BTERM# (input) is disabled, a new ADS# cycle starts every quad-Lword boundary. BTERM# (input) replaces READY# (input) when asserted.

Timing Diagram 4-23. PCI Target Burst Write with Bterm Enabled (32-Bit Local Bus), Multiplexed Mode Only

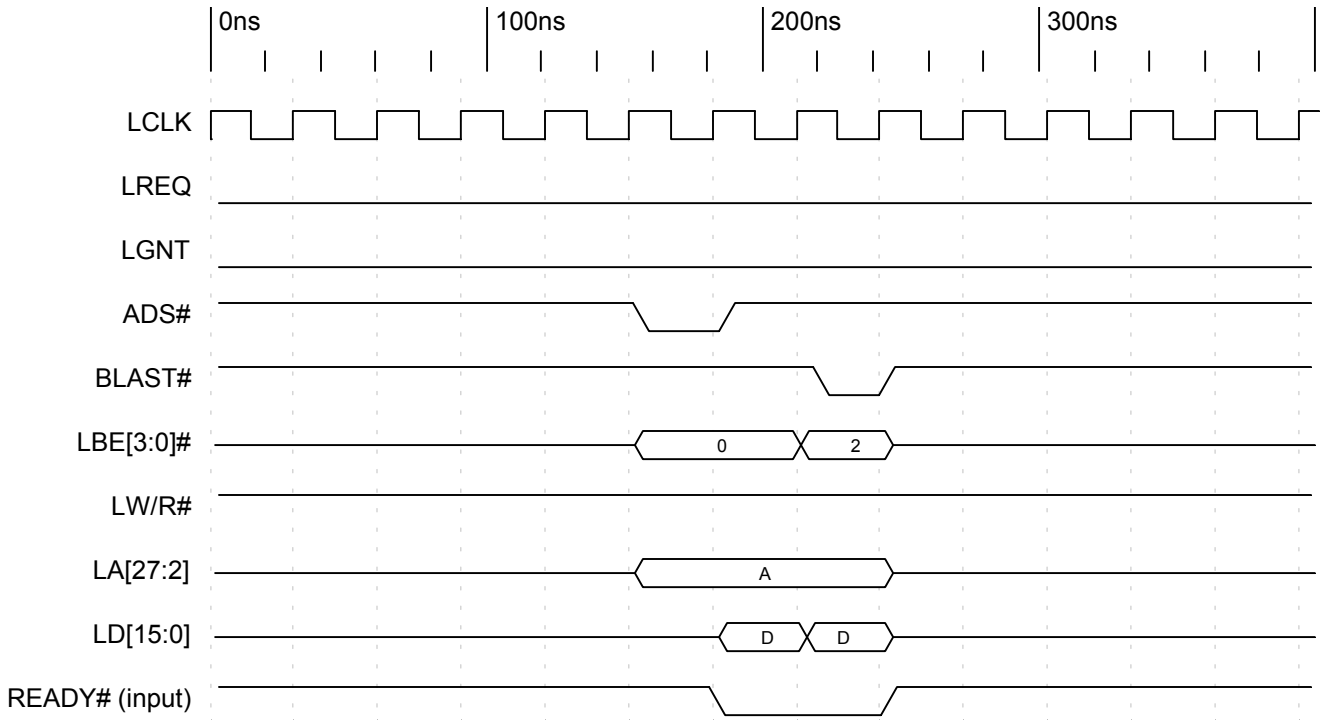


Timing Diagram 4-24. PCI Target Burst Read with Prefetch Enabled (32-Bit Local Bus), Prefetch Counter Set to 8, Multiplexed Mode Only

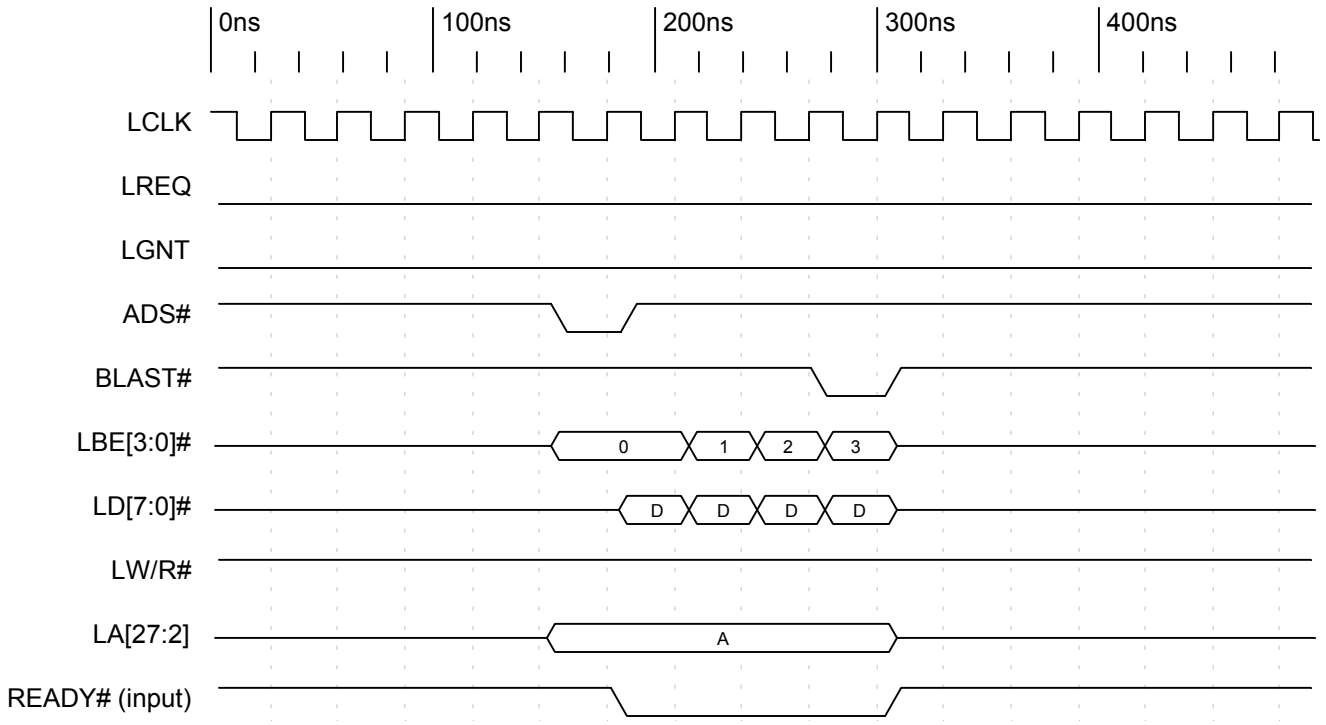
4.4.2.2 PCI Target, Non-Multiplexed Mode Only



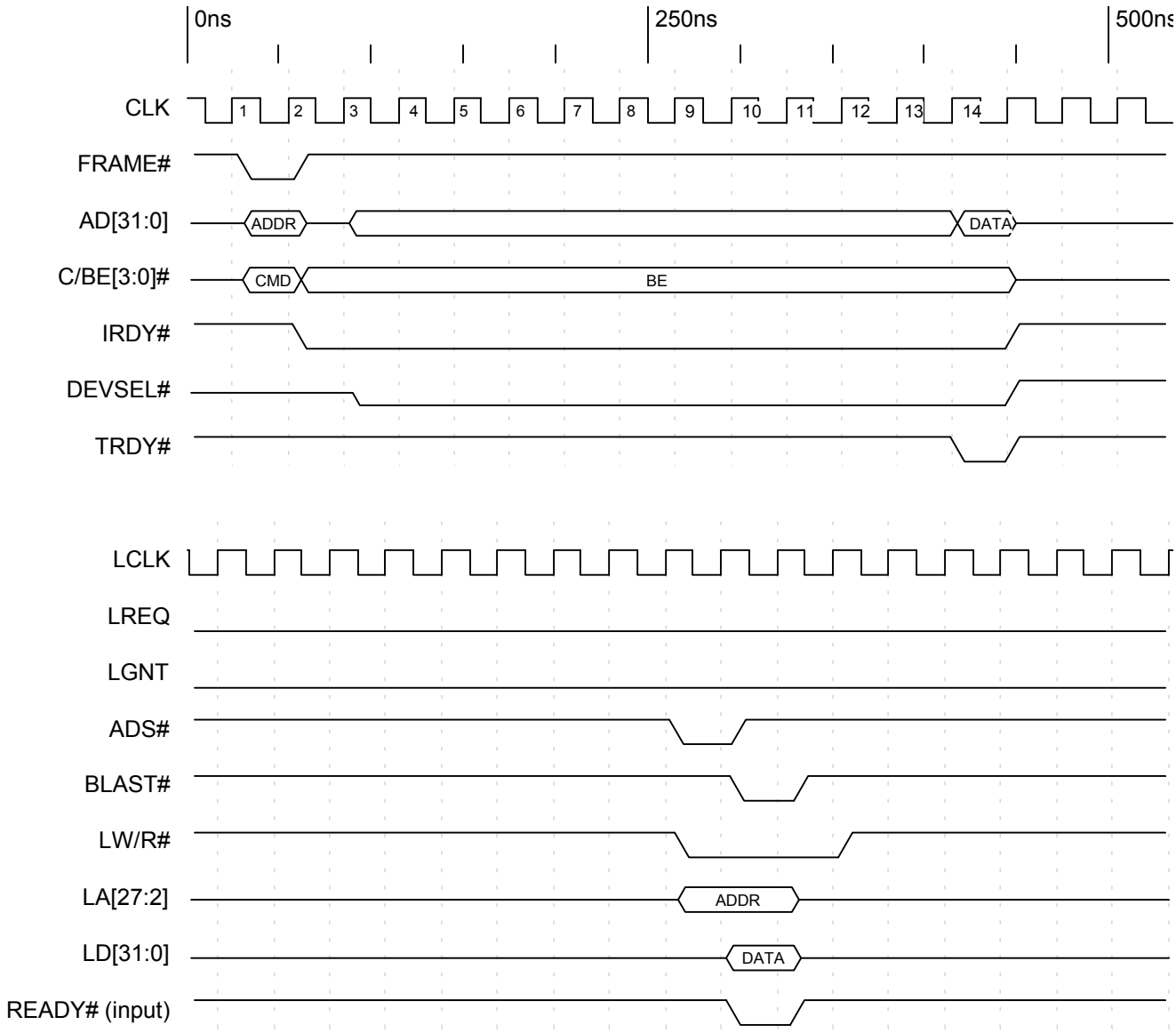
Timing Diagram 4-25. PCI Target Single Write (32-Bit Local Bus), Non-Multiplexed Mode Only



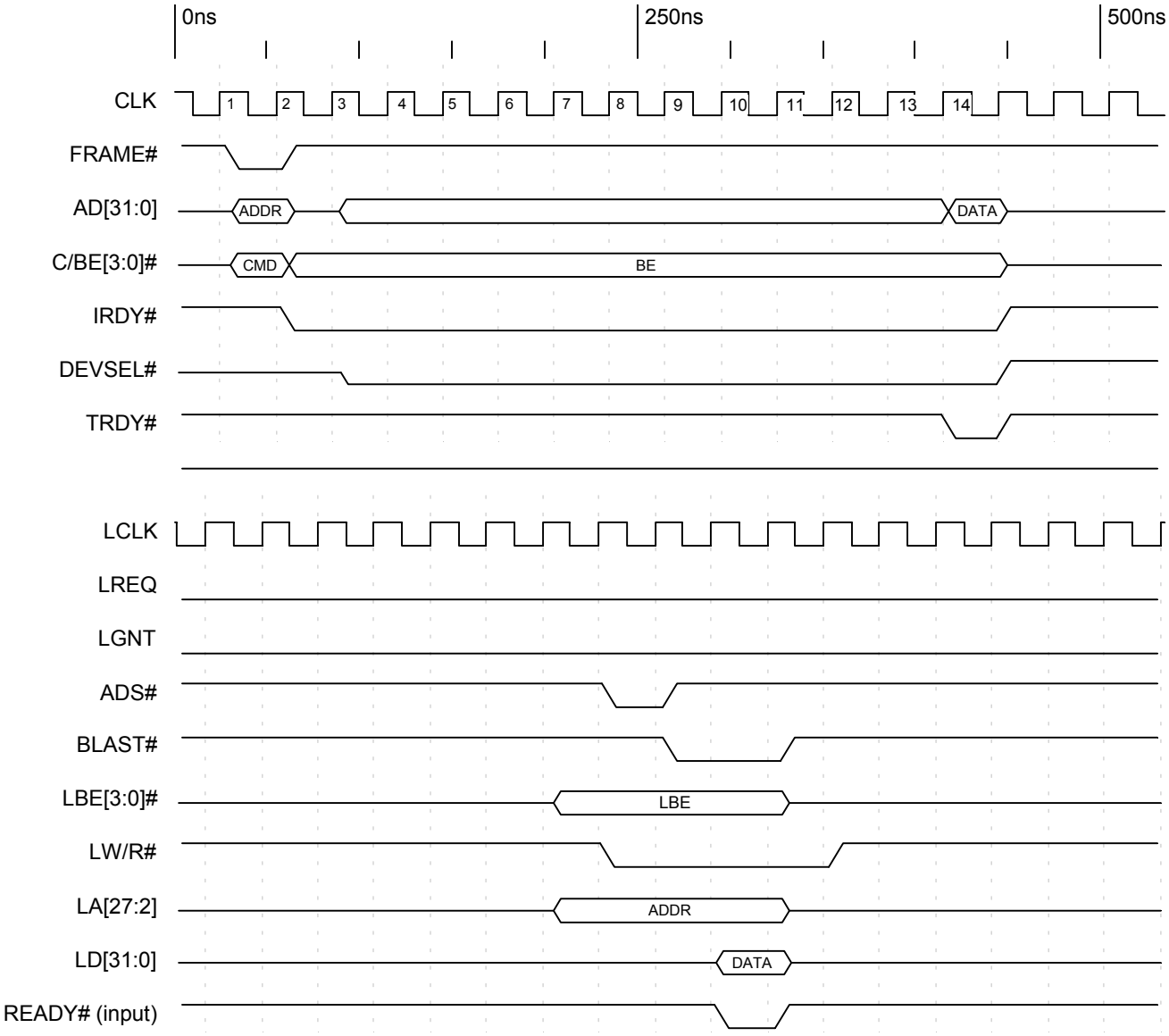
Timing Diagram 4-26. PCI Target Single Write (16-Bit Local Bus), Non-Multiplexed Mode Only



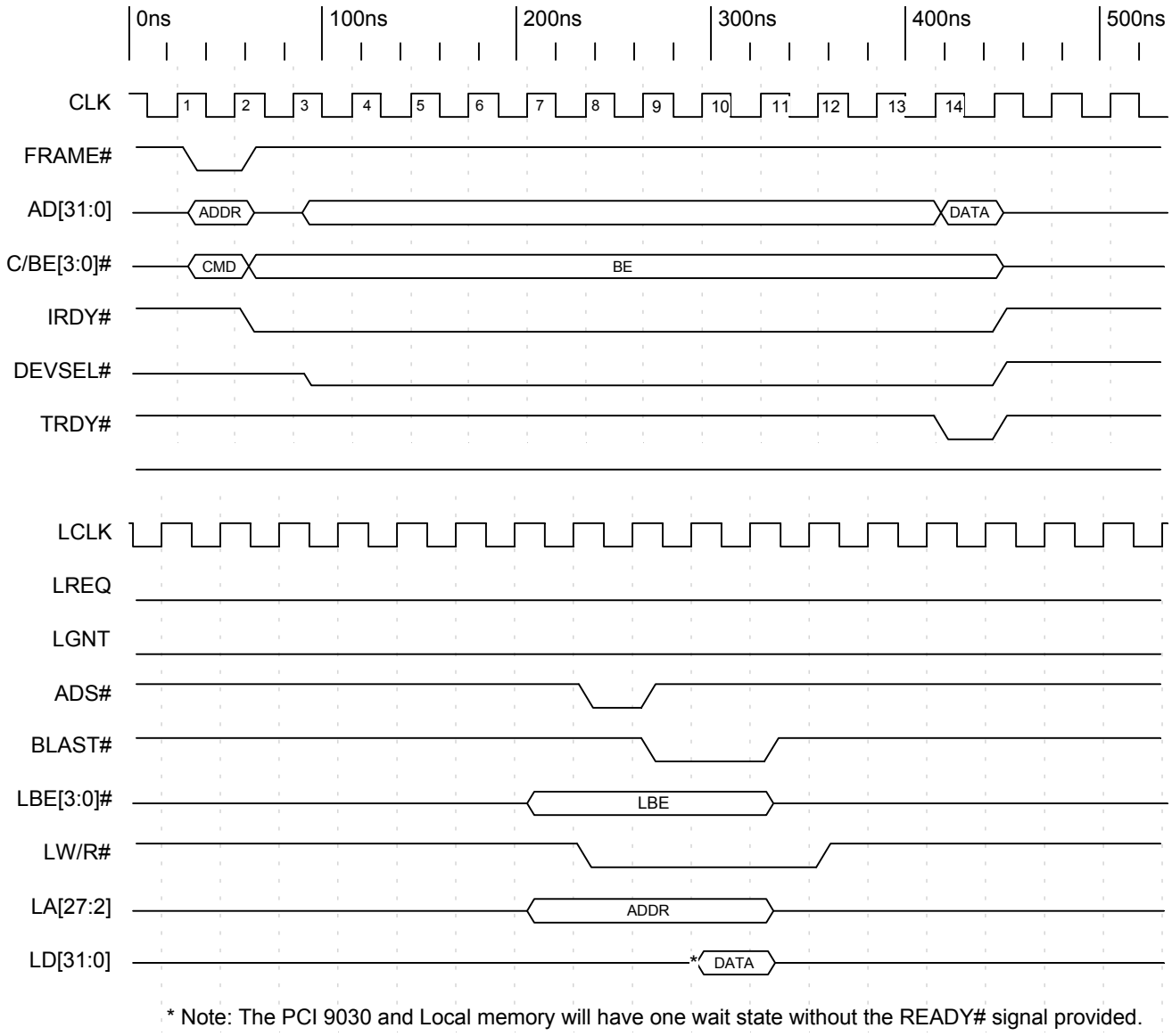
Timing Diagram 4-27. PCI Target Single Write (8-Bit Local Bus), Non-Multiplexed Mode Only



Timing Diagram 4-28. PCI Target Single Read (32-Bit Local Bus), Non-Multiplexed Mode Only

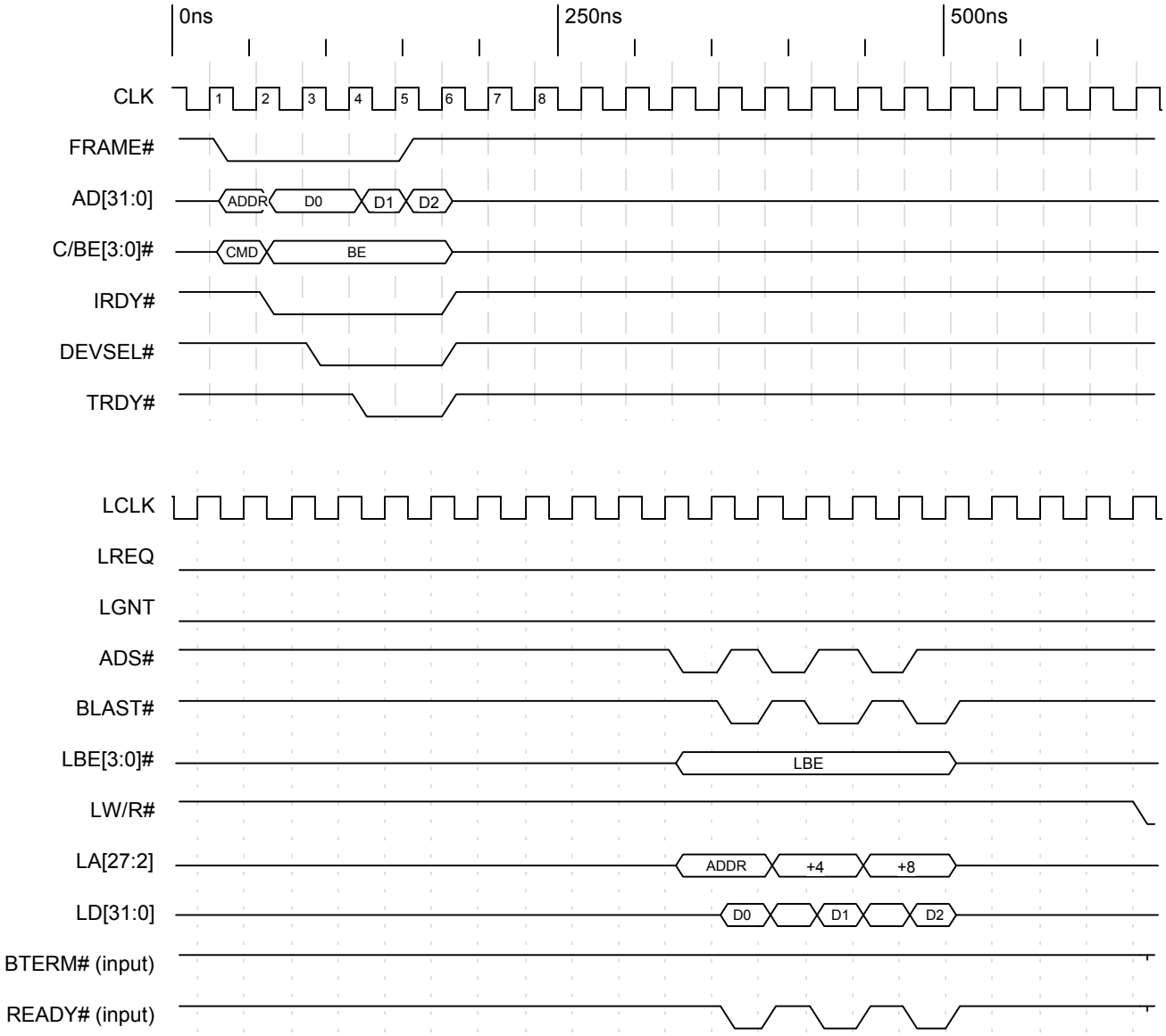


Timing Diagram 4-29. PCI Target Single Read with One Wait State Using READY# Input (32-Bit Local Bus), Non-Multiplexed Mode Only

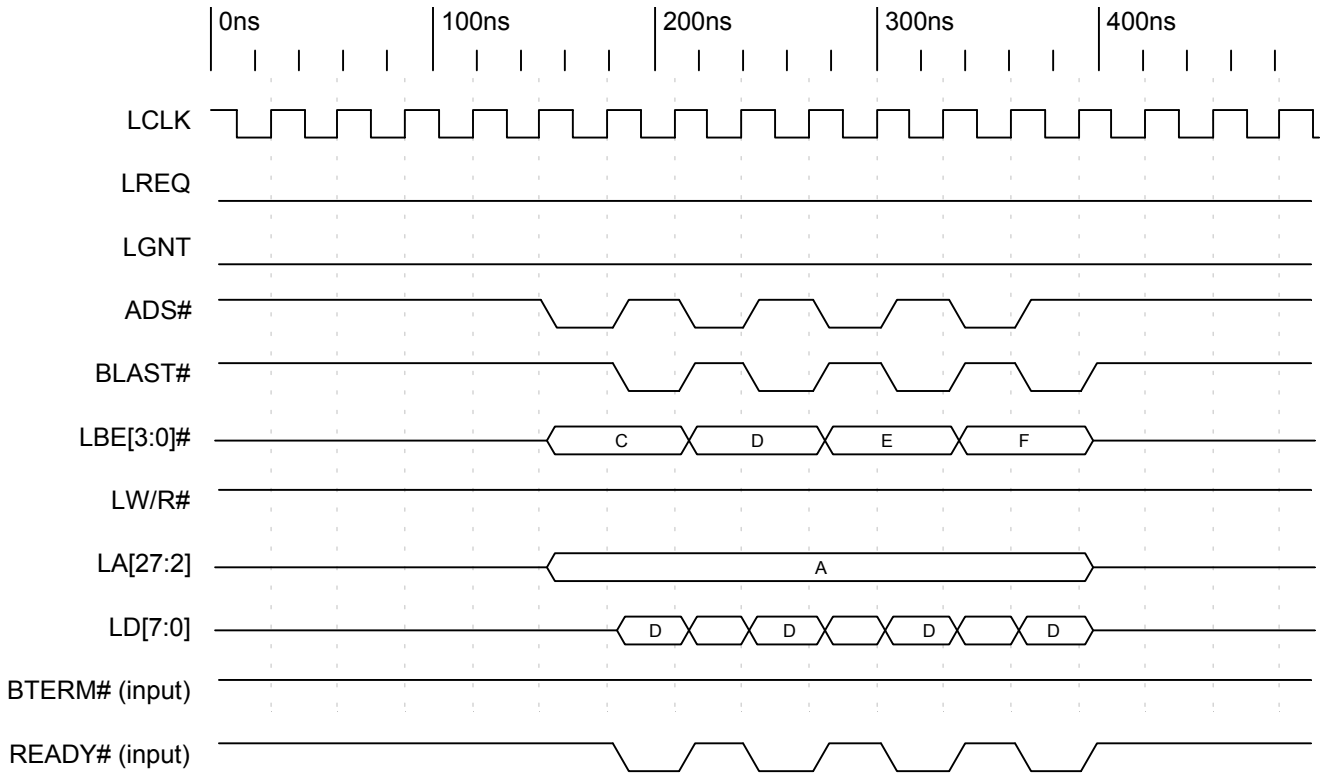


* Note: The PCI 9030 and Local memory will have one wait state without the READY# signal provided.

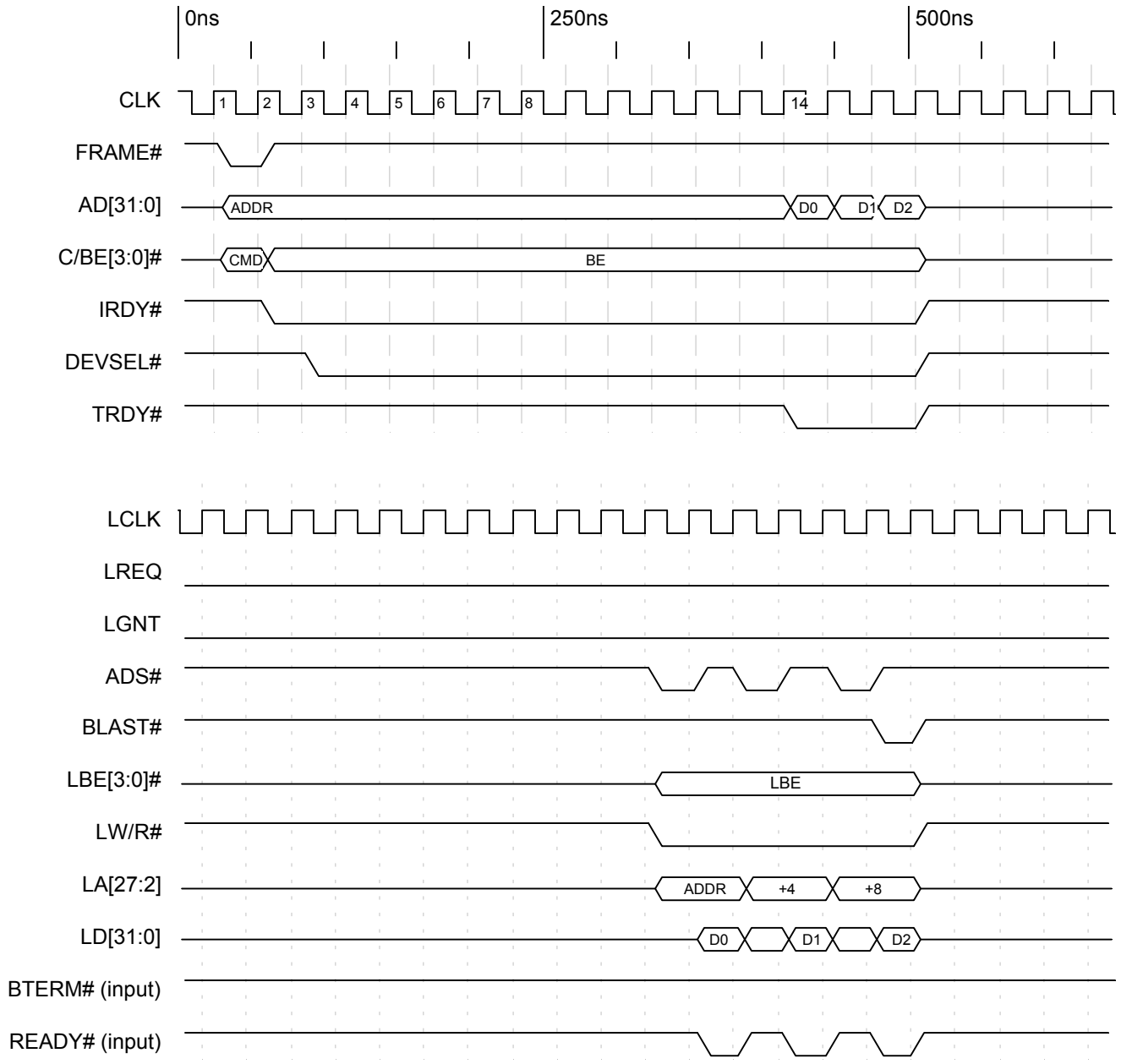
Timing Diagram 4-30. PCI Target Single Read with One Wait State Using Internal Wait State (32-Bit Local Bus), Non-Multiplexed Mode Only



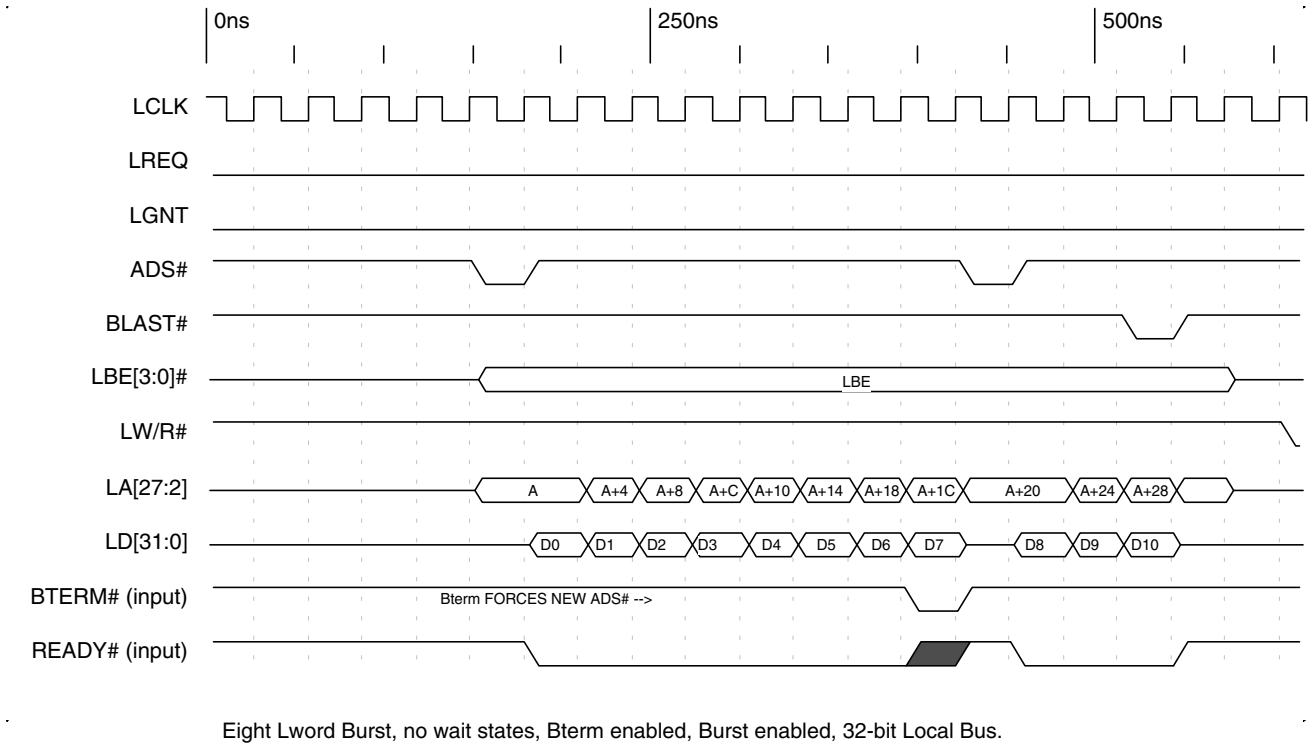
Timing Diagram 4-31. PCI Target Non-Burst Write (32-Bit Local Bus), Non-Multiplexed Mode Only



Timing Diagram 4-32. PCI Target Non-Burst Write (8-Bit Local Bus), Non-Multiplexed Mode Only



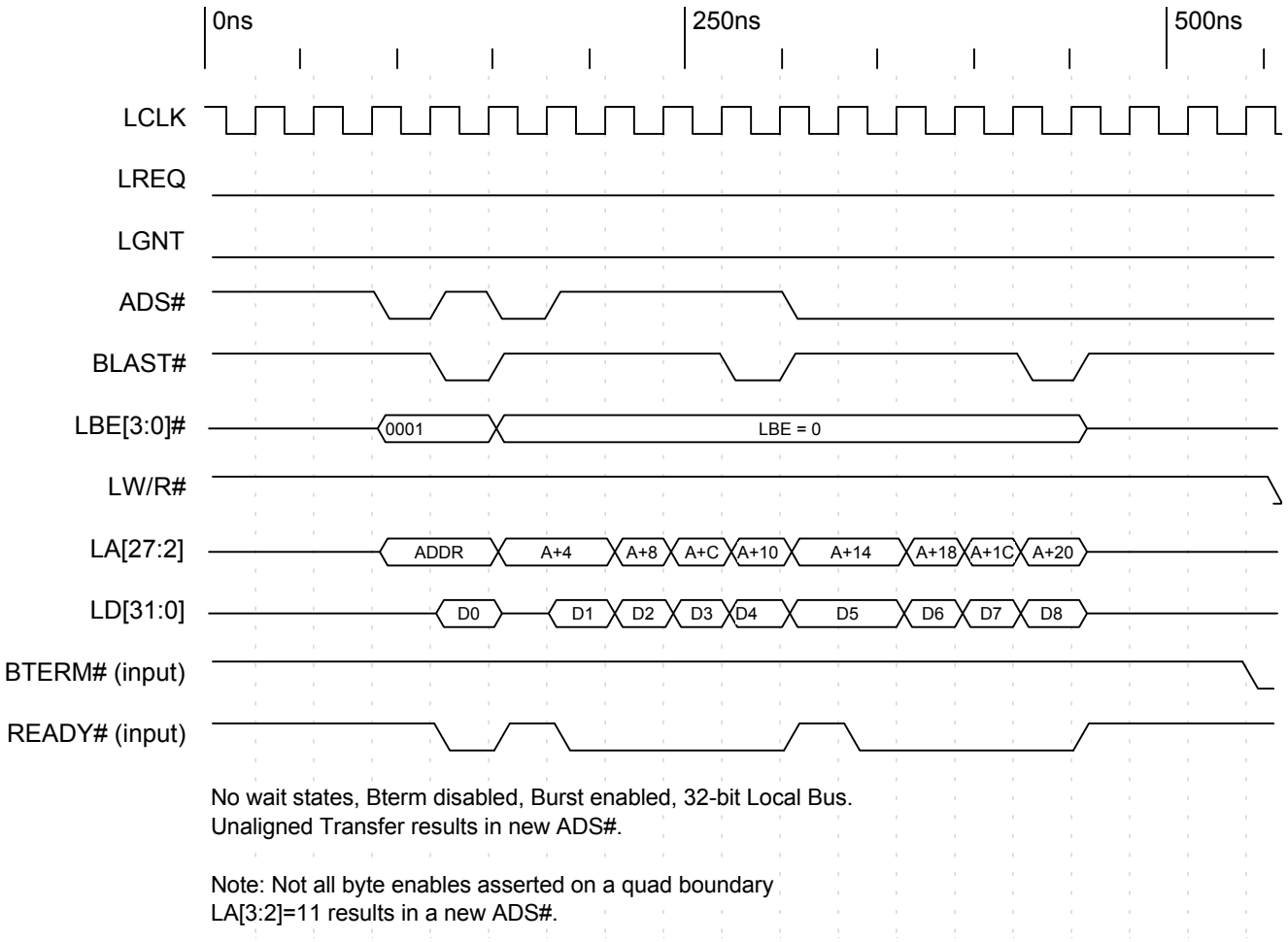
Timing Diagram 4-33. PCI Target Non-Burst Read, Non-Multiplexed Mode Only



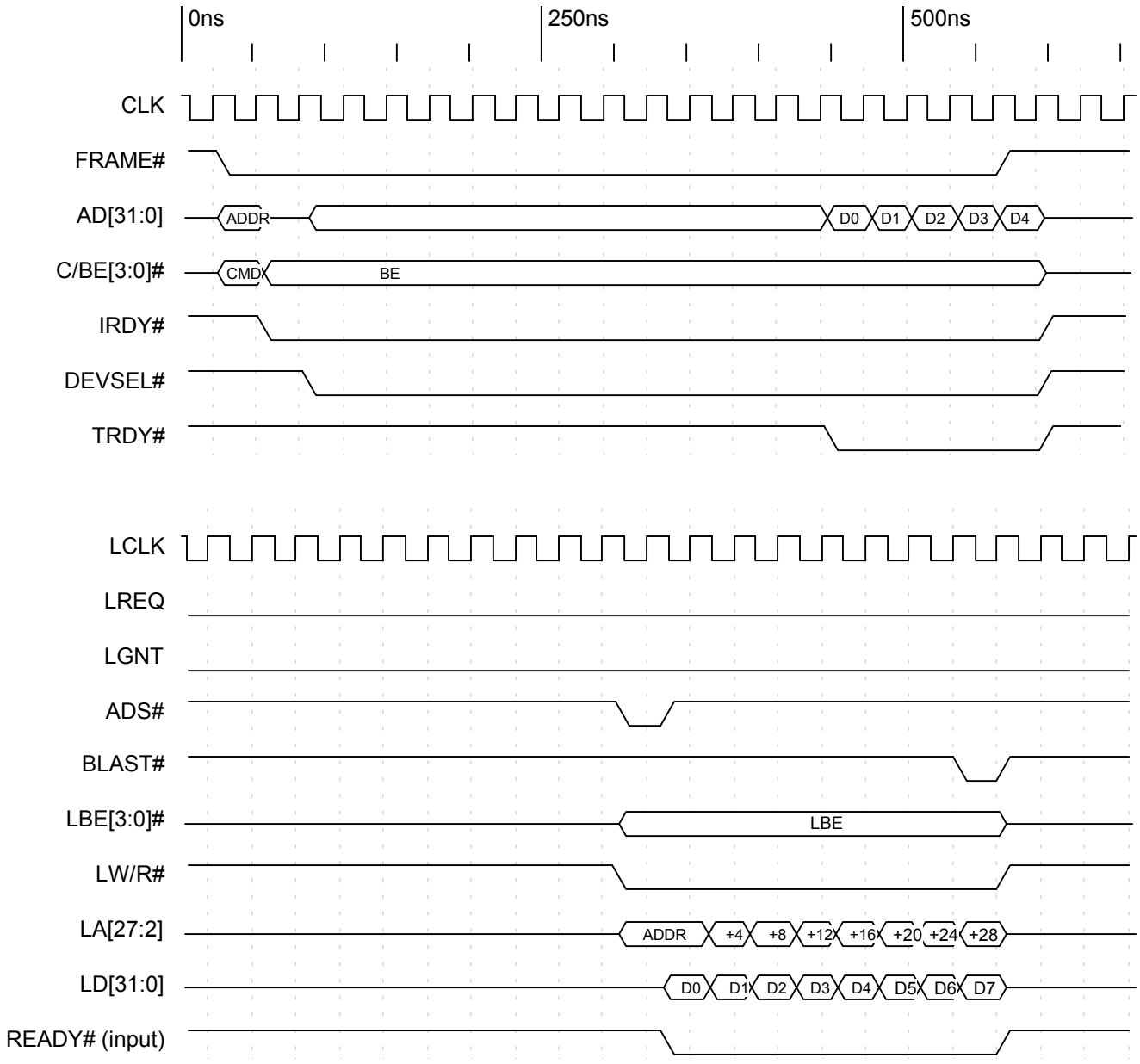
Eight Lword Burst, no wait states, Bterm enabled, Burst enabled, 32-bit Local Bus.

Note: If Bterm is disabled, a new ADS# cycle starts every quad-Lword boundary.

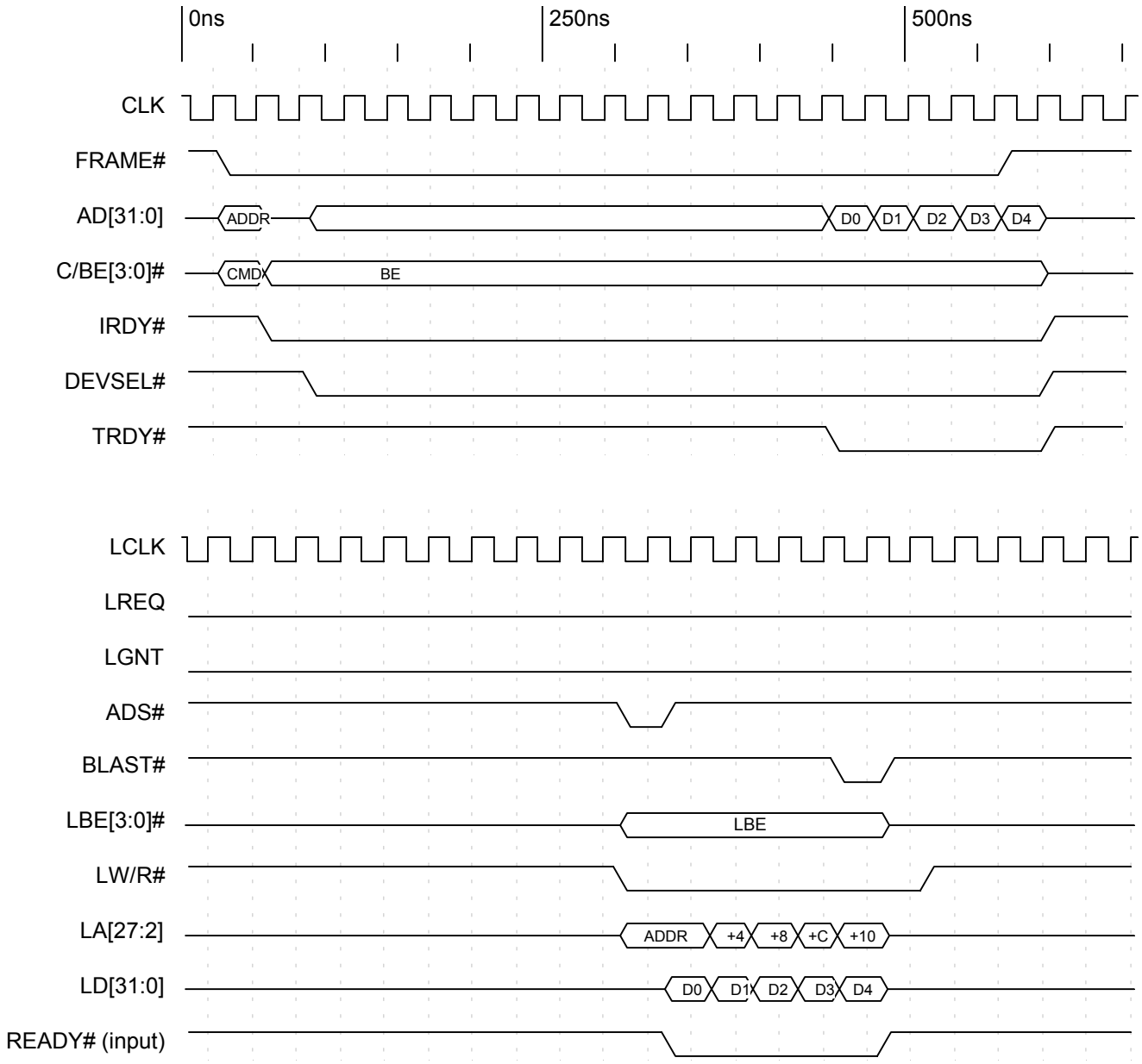
Timing Diagram 4-34. PCI Target Burst Write with Bterm Enabled (32-Bit Local Bus), Non-Multiplexed Mode Only



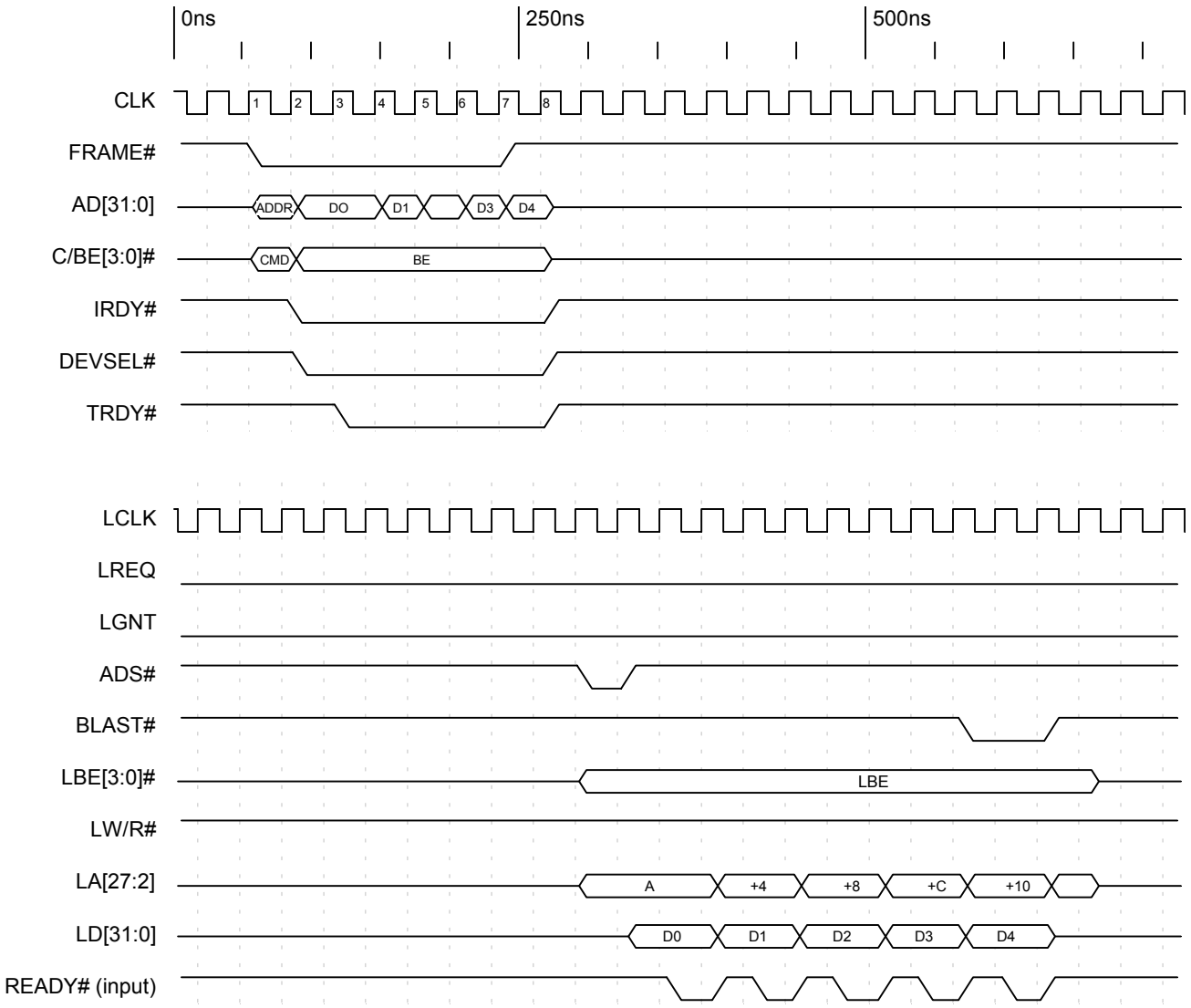
Timing Diagram 4-35. PCI Target Burst Write with Bterm Disabled (32-Bit Local Bus), Non-Multiplexed Mode Only



Timing Diagram 4-36. PCI Target Burst Read with Prefetch Counter Set to 8 (32-Bit Local Bus), Non-Multiplexed Mode Only

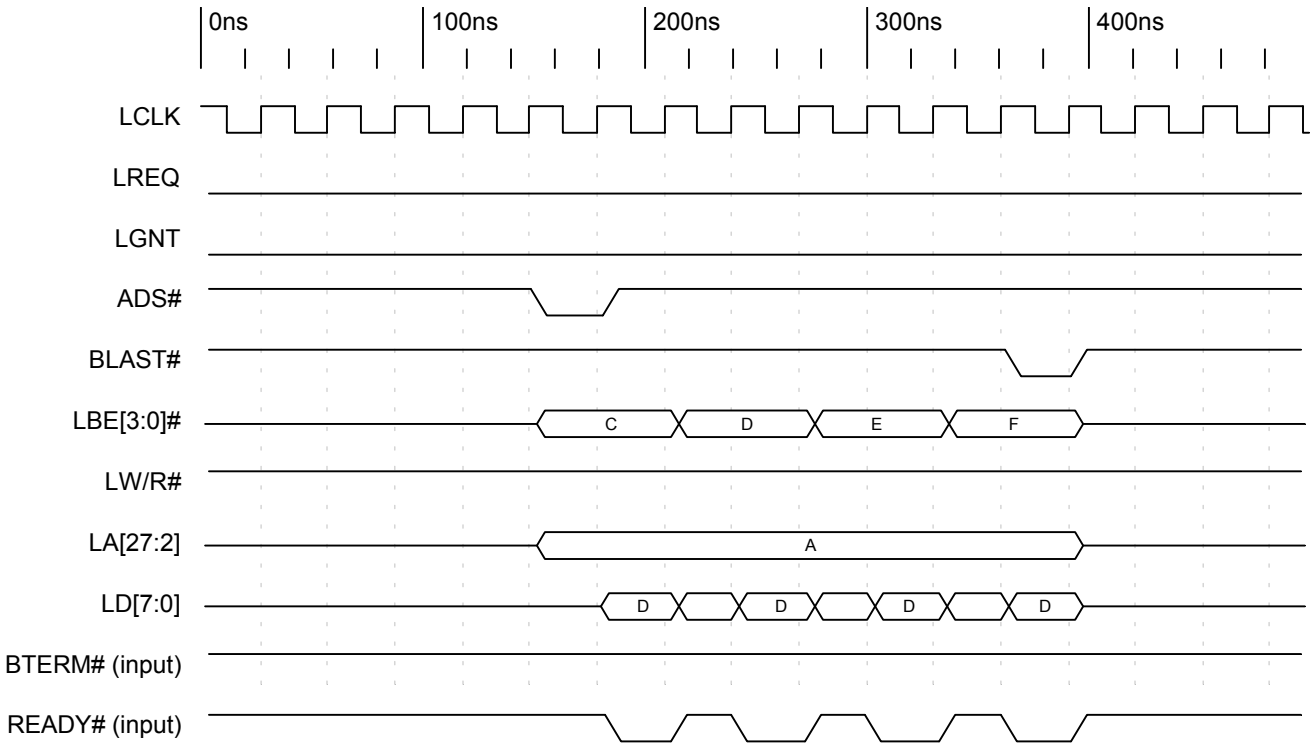


Timing Diagram 4-37. PCI Target Burst Read with Prefetch Counter Set to 5 (32-Bit Local Bus), Non-Multiplexed Mode Only

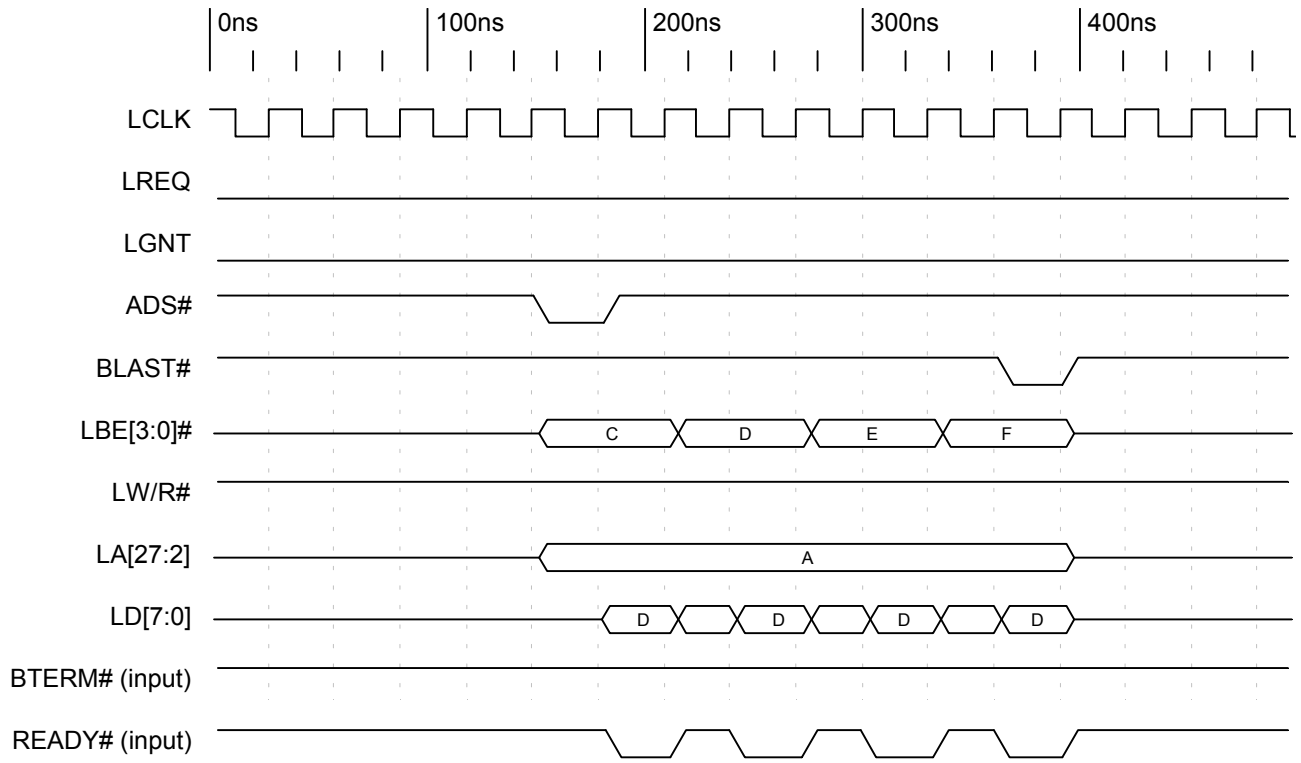


Five Lwords, one external wait state, Bterm enabled, Burst enabled.

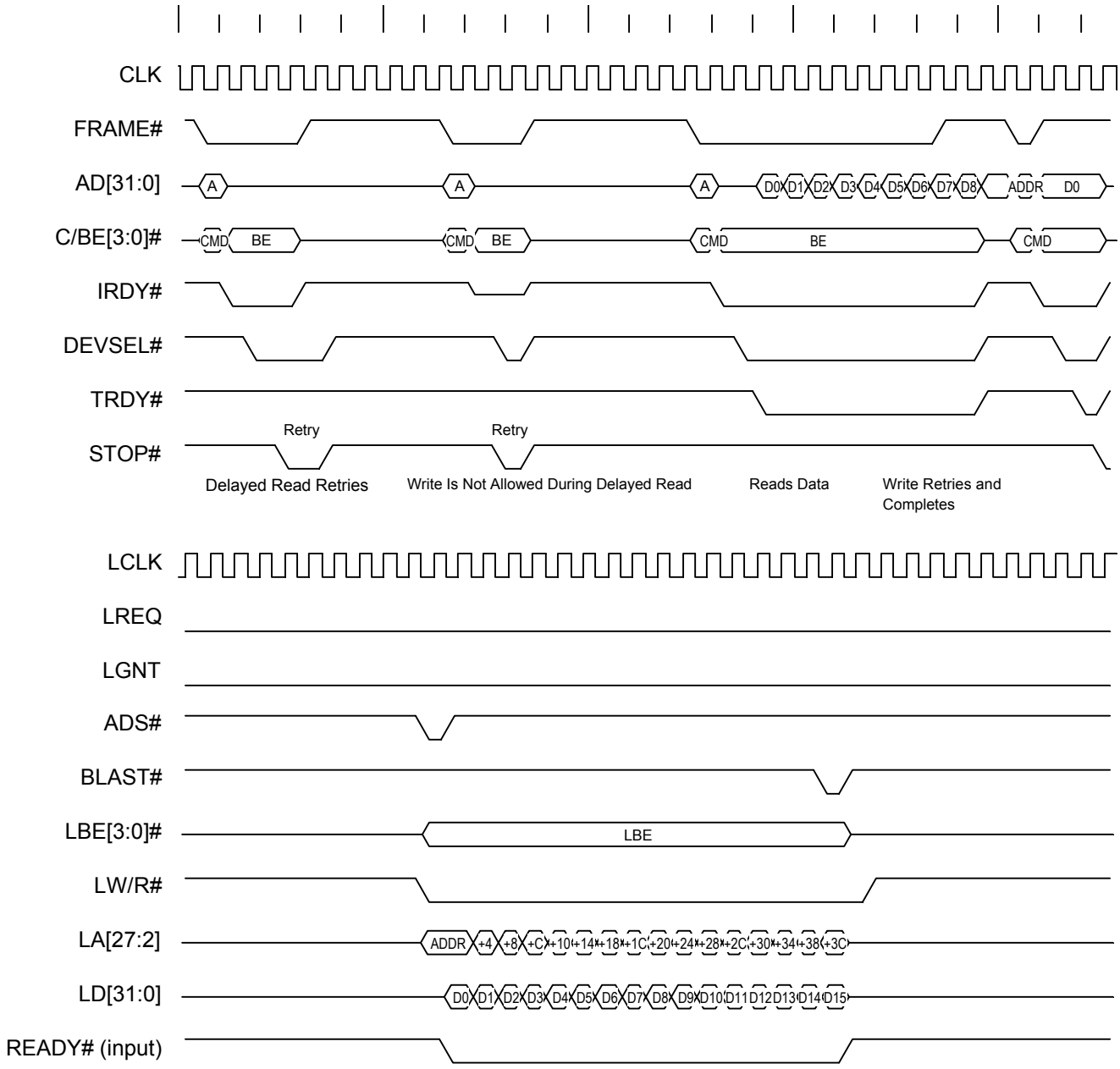
Timing Diagram 4-38. PCI Target Burst Write (32-Bit Local Bus), Non-Multiplexed Mode Only



Timing Diagram 4-39. PCI Target Burst Write (16-Bit Local Bus), Non-Multiplexed Mode Only



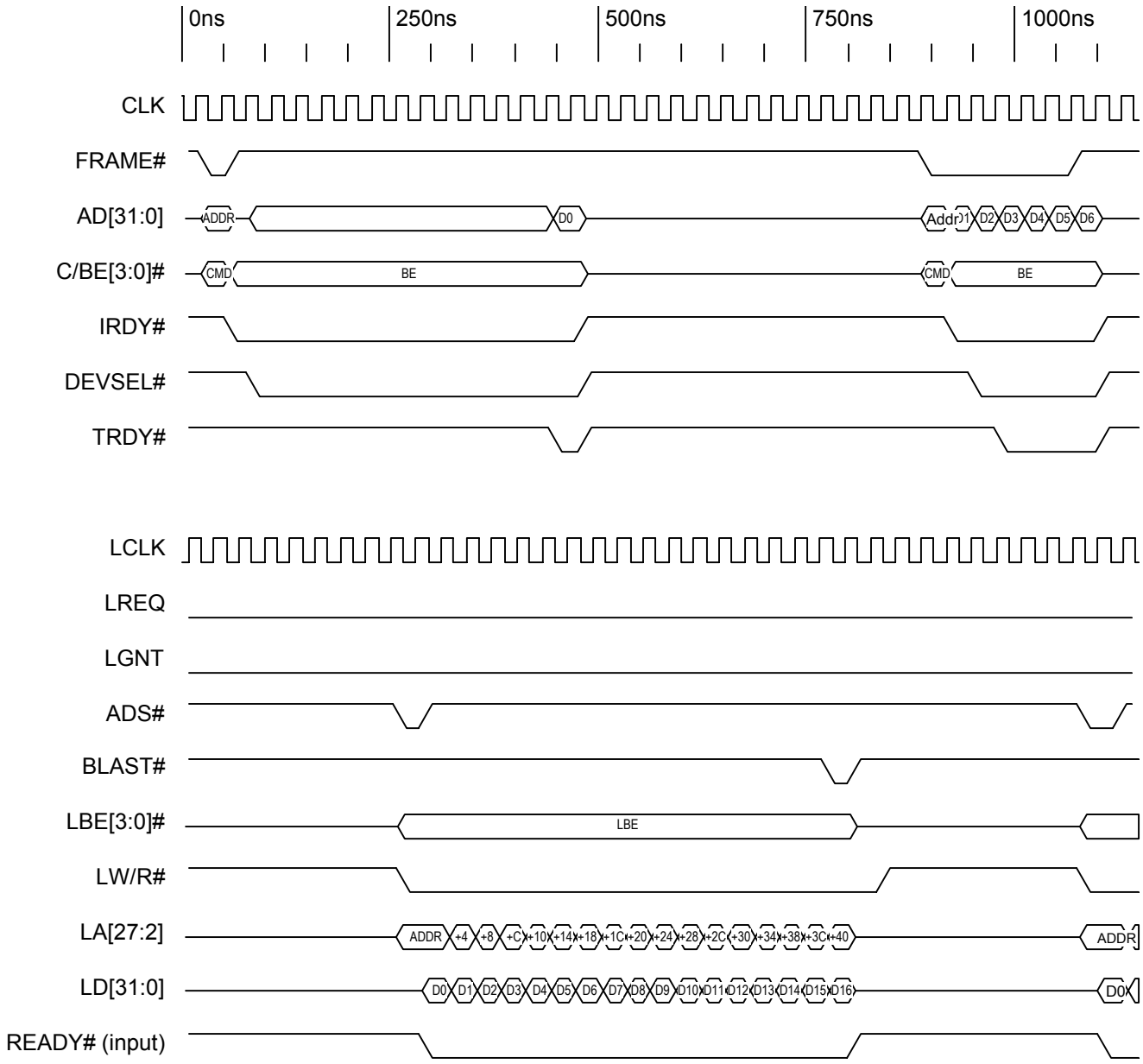
Timing Diagram 4-40. PCI Target Burst Write with External Wait States (8-Bit Local Bus), Non-Multiplexed Mode Only



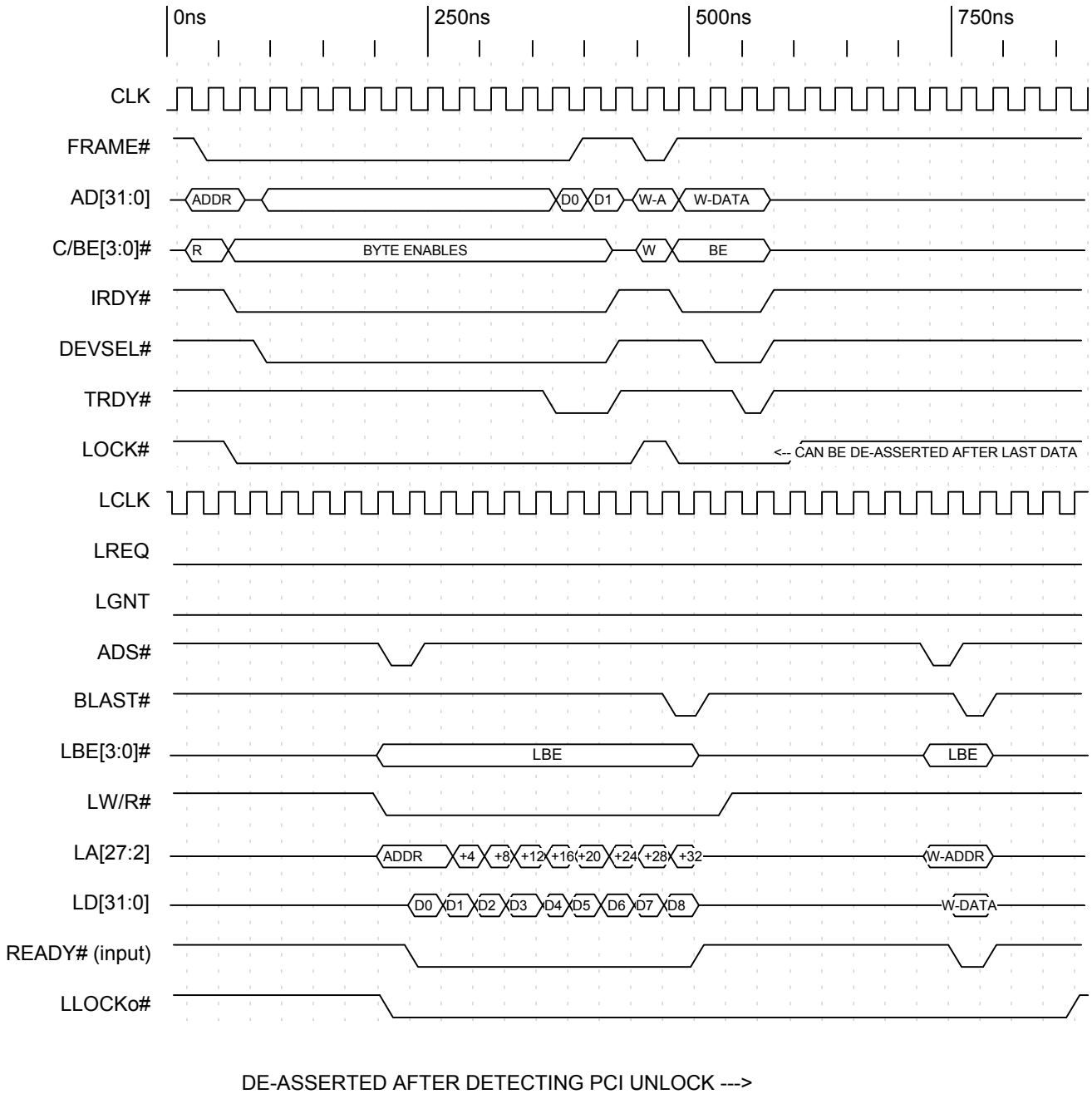
Disconnect immediately for a read. Does not effect pending reads when a Write cycle occurs, nor flush the Read FIFO if the PCI Read cycle completes.

When a read is pending, force Retry on a write. De-assert TRDY# until space is available in the PCI Target Write FIFO.

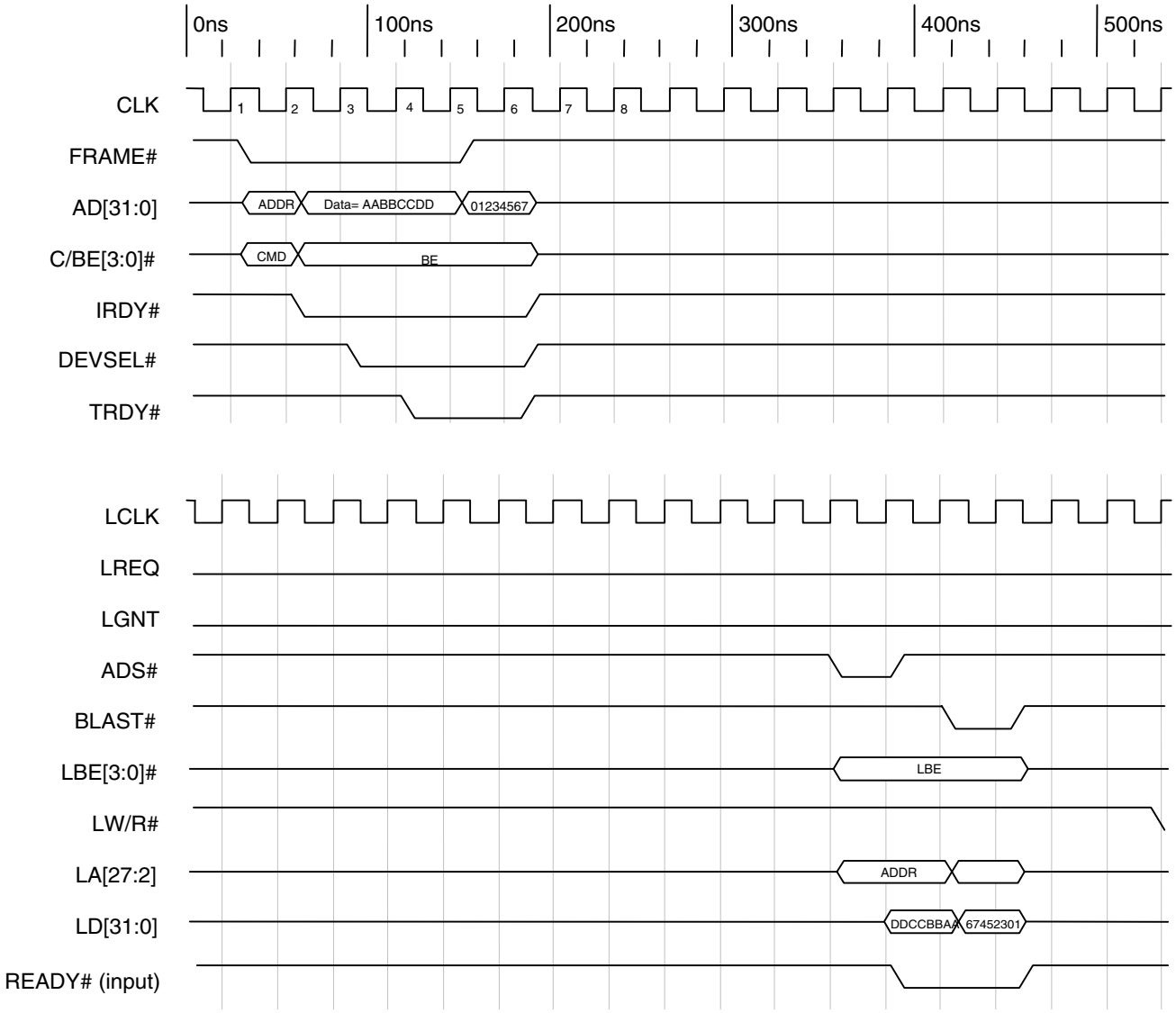
Timing Diagram 4-41. Delayed Read Transaction PCI Specification v2.2, Non-Multiplexed Mode Only



Timing Diagram 4-42. PCI Target Read No Flush Mode (Read Ahead Mode), Prefetch Enabled, Prefetch Count Disabled, Non-Multiplexed Mode Only



Timing Diagram 4-43. Locked PCI Target Read Followed by Write and Release (LLOCKo#), Non-Multiplexed Mode Only



Timing Diagram 4-44. PCI Target Write to Local Target in BIGEND Mode, Non-Multiplexed Mode Only

5 LOCAL CHIP SELECTS

5.1 OVERVIEW

The PCI 9030 supports four different chip selects. Each chip select is programmable and independent of Address Space. The PCI 9030 includes the ability to directly provide Chip Select control signals to four devices on the PCI 9030 Local Bus. Without this feature, it is necessary to add address-decoding logic for each required Chip Select.

5.2 CHIP SELECT BASE ADDRESS REGISTERS

There are four Chip Select Base Address registers. These registers control the four chip select pins on the PCI 9030. *For example*, Chip Select 0 Base Address Register controls CS0# (PQFP—pin 147; µBGA—pin C9), Chip Select 1 Base Address Register controls CS1# (PQFP—pin 148; µBGA—pin B9), and so forth.

The Chip Select Base Address registers serve three purposes:

1. To enable or disable chip select functions within the PCI 9030. If enabled, the Chip Select signal is active if the address on the address line falls within the address specified by the range and base address. If disabled, the Chip Select signal is not active.
2. To set the range of addresses for which the Chip Select signal(s) are active.
3. To set the base address at which the range starts.

To program the Chip Select Base Address registers, there are three rules:

1. Range must be a power of 2.
2. Base address must be a multiple of the range.
3. Multiple Chip Select Base Address registers, if used, are programmed to not overlap one another.

Each 28-bit Chip Select Base Address register is programmed as listed in the following table.

Table 5-1. Chip Select Base Address Register Signal Programming

MSB=27						LSB=0
XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXY

The Y bit (bit 0) enables or disables the chip select signal. X bits are used to determine the range and base address of where the CS# pin is asserted. To program the base and range, the X bits are set as follows:

- Device length or range is equal to the first bit set above the Y bit. Determined by setting a bit in the register equal to the exponent in the exponential representation of the range. Bit is counted up, starting at the Y bit, where the Y bit is counted as 1.
- Base address is determined by the bit or bits set above the range bit (range multiple). Number uses all bits in register above the range bits.

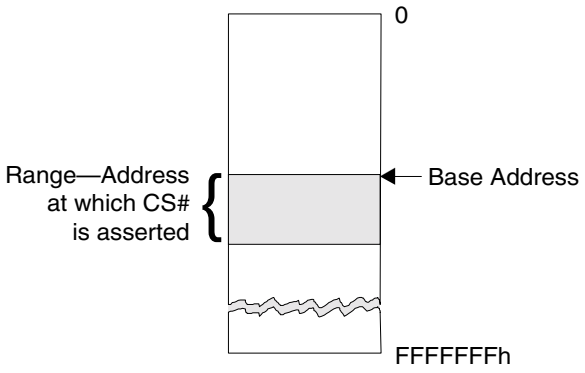


Figure 5-1. Chip Select Base Address and Range

5.3 PROCEDURE FOR USING CHIP SELECT BASE ADDRESS REGISTERS

The following procedure describes how to use the Chip Select Base Address registers.

1. Determine the range in hex. Convert this number to a power of 2. Range must be a power of 2 (*for example*, 2^1, 2^2, 2^3, 2^{16}, and so forth).
2. Set a bit in the Chip Select Base Address register to determine the range. Use the range exponent to set the bit in the Chip Select Base Address register. In a binary representation of the Chip Select Base Address register, count left, starting at the Y bit, where Y is one. Only one bit may be set.
3. Determine the base address. It is recommended to use hex numbers for the base address. Base address must be a multiple of the range.
4. Determine the base address multiplier. Divide range into the base address in hex:

   (base address)/(range)=(base address multiplier)
5. Convert the base address multiplier to binary.
6. Set the base address multiplier bits directly above the range bit in the Chip Select Base Address register.

Example: A 16K SRAM device is attached to the Local Bus and a chip select is provided. The base address is specified to be 24000h. The following figure illustrates this example.

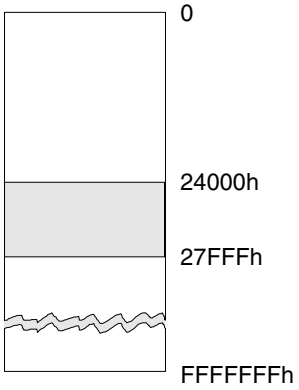


Figure 5-2. Memory Map Example

1. Determine the range in hex and convert the number to a power of 2 (*for example*, 16K is equivalent to 4000h, or 2^{14} bits).
2. Set the bit in the Chip Select Base Address register to specify the range. Set the 14th bit to 1.

MSB=27						LSB=0
0000	0000	0000	0010	0000	0000	0000

3. Determine the base address (*for example*, 24000h).
4. Determine the base address multiplier. Divide the range into the base address in hex (*for example*, 24000h/4000h=9h).
5. Convert the base address multiplier to binary (*for example*, 1001b).
6. Set the base address multiplier bits directly above the range bit in the Chip Select Base Address register.

			Base Address Multiplier		Range			
MSB=27								LSB=0
0000	0000	00	10	01	10	0000	0000	0000

The following is a complete example of setting the Chip Select Base Address register with a range of 4000h, a base address of 24000h, and enabled:

MSB=27						LSB=0
0000	0000	0010	0110	0000	0000	0001

6 PCI AND LOCAL INTERRUPTS AND GENERAL PURPOSE I/O

6.1 OVERVIEW

There are two local interrupt pins which can trigger PCI interrupt INTA#. Each pin has a global Enable or Disable bit. In addition, each pin is programmable to a different polarity, and can be triggered by an edge or level. Each interrupt has a status bit indicating which interrupt source is active.

6.2 INTERRUPTS

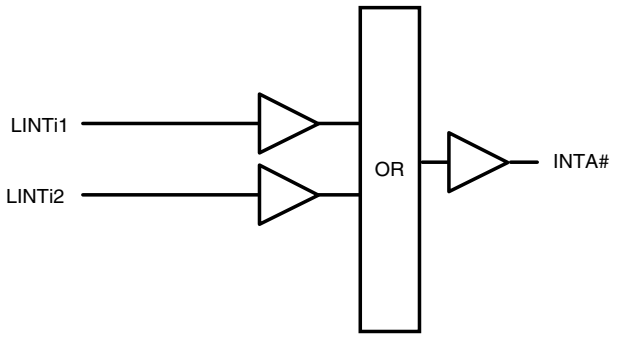


Figure 6-1. Interrupt and Error Sources

6.2.1 PCI Interrupts (INTA#)

A PCI 9030 PCI Interrupt (INTA#) can be asserted by Local Interrupt Input 2 or 1 (LINTi[2:1]), which are described in the next section.

INTA#, or individual sources of an interrupt, can be enabled or disabled with the PCI 9030 Interrupt Control/Status register (INTCSR). This register also provides the interrupt status of each interrupt source.

The PCI 9030 PCI Bus interrupt is a level output. Disabling an interrupt enable bit or clearing the cause(s) of the interrupt can clear an interrupt.

6.2.2 Local Interrupt Input (LINTi[2:1])

The PCI 9030 provides two Local interrupts (LINTi[2:1]). The Local interrupts can be used to generate a PCI interrupt. LINTi[2:1] supports different polarity, edge or level trigger, programmable through the Interrupt Control/Status register (INTCSR; 4Ch).

6.2.3 Local Power Management Interrupt (LPMINT#)

The PCI 9030 is a PCI Target device only; therefore, there is no access to the internal registers from the Local Bus. The Local Power Management Interrupt output (LPMINT#) is included to accommodate the PCI Bus Power Management interface to a Local Bus.

The PCI 9030 asserts LPMINT# to request a Power State change to the Local Bus when the Power Management Control/Status register (PMCSR[1:0]) changes. The LPMINT# interrupt is synchronous to the Local clock. When asserted, it is a one clock-wide pulse.

External glue logic is needed to latch the Power State change and to retain the previous Power State history for further evaluation by the external Local Bus Initiator.

6.2.4 Local Power Management Enumerator Set

The Local Power Management Enumerator Set Interrupt input (LPMESET) is included to accommodate the PCI Bus Power Management interface to a Local Bus.

The external Local Bus Initiator can assert LPMESET to the PCI 9030 Power Management Control/Status register (PMCSR[15]) to set the PME# status and assert the PME# signal to the PCI Bus in case of a Wake-up Request event.

6.2.5 All Modes PCI SERR# (PCINMI)

The PCI 9030 asserts an SERR# pulse if parity checking is enabled (PCICR[6]=1) and it detects an address or parity error.

The SERR# output can be enabled or disabled with the SERR# Enable bit (PCICR[8]).

6.3 GENERAL PURPOSE I/O

The PCI 9030 supports nine general purpose input and output pins, multiplexed GPIO0/WAITo#, GPIO1/LLOCKo#, GPIO2/CS2#, GPIO3/CS3#, GPIO4/LA27, GPIO5/LA26, GPIO6/LA25, and GPIO7/LA24, and GPIO8. The PCI 9030 default condition is the General Purpose Input for GPIO[3:0], with Local Address LA[27:24] for GPIO[7:4], and General Purpose Input for GPIO8. The general purpose input and output pins and functionality can be enabled and selected in the General Purpose I/O Control register (GPIOC[31:0]).

7 PCI POWER MANAGEMENT

7.1 OVERVIEW

The *PCI Bus Power Management Interface Specification* v1.1 provides a standard mechanism for operating systems to control add-in boards for power management. The Specification defines four PCI functional power states—D_0, D_1, D_2, and D_3. States D_0 and D_3 are required, while states D_1 and D_2 are optional. State D_0 represents the highest power consumption and state D_3 the least.

- **D_0 (Uninitialized)**—Enters this state from Power-On Reset or from state D_{3hot} or D_{3cold}. Supports PCI Target transactions only.
- **D_0 (Active)**—All functions active.
- **D_1**—Uses less power than State D_0, and more than state D_2. Light Sleep State. ***Not supported by the PCI 9030.***
- **D_2**—Uses very little power.

  Supports PCI Configuration cycles to function if clock is running (Memory, I/O, Bus Mastering, and Interrupts are disabled). It also supports the Wake-up Event from function, but not standard PCI interrupts. ***Not supported by the PCI 9030.***
- **D_{3hot}**—Uses lower power than any other state. Supports PCI Configuration cycles to function if clock is running. Supports Wake-up Event from function, but not standard PCI interrupts. When programmed for state D_0, an internal soft reset occurs. The PCI Bus drivers must be disabled. PME# context must be retained during this soft reset.
- **D_{3cold}**—No power. Supports Bus reset only. All context is lost in this state.

From a power management perspective, the PCI Bus can be characterized at any point in time by one of four power management states—B_0, B_1, B_2, and B_3:

- **B_0 (Fully On)**—Bus is fully usable with full power and clock frequency, PCI v2.2 compliant. Fully operational bus activity. This is the only Power Management state in which data transactions can occur.
- **B_1**—Intermediate power management state. Full power with clock frequency, PCI v2.2 compliant. PME Event driven bus activity. Vcc is applied to all devices on the bus, and no transactions are allowed to occur on the bus.
- **B_2**—Intermediate power management state. Full power clock frequency stopped, *PCI* v2.2 compliant (in the low state). PME Event-driven bus activity. Vcc is applied to all devices on the bus; however, the clock is stopped and held in the Low state.
- **B_3 (Off)**—Power to the bus is switched off. PME Event-driven bus activity.Vcc is removed from all devices on the PCI Bus.

All system PCI Buses have an originating device, which can support one or more power states. In most cases, this creates a bridge (*such as*, a Host-to-PCI-Bus or a PCI-to-PCI bridge).

Function States must be at the same or lower energy state than the bus on which they reside.

7.2 PCI POWER MANAGEMENT FUNCTIONAL DESCRIPTION

The PCI 9030 passes power management information and has no inherent power-saving feature. The PCI 9030 supports D_0, D_{3hot}, and D_{3cold} states.

The PCI Status register (PCISR) and the New Capability Pointer register (CAP_PTR) indicate whether a new capability (the Power Management function) is available. The New Capability Functions Support bit (PCISR[4]) enables a PCI BIOS to identify a New Capability function support. This bit is executable for writes from the serial EEPROM and reads from the PCI Bus. CAP_PTR provides an offset into PCI Configuration Space, the start location of the first item in a New Capabilities Linked List.

The Power Management Capability ID register (PMCAPID) specifies the Power Management Capability ID, 01h, assigned by the PCI SIG. The Power Management Next Capability Pointer register (PMNEXT) points to the first location of the next item in the capabilities linked list. If Power Management is the last item in the list, then this register should be set to 0. The default value for the PCI 9030 is 48h (Hot Swap).

For the PCI 9030 to change the power state and assert PME#, the serial EEPROM or PCI Host should set the PME#_En bit (PMCSR[8]=1). The Local Host then determines to which power state the backplane should change by monitoring the Power_State bits (PMCSR[1:0]), by way of the LPMINT# interrupt signal.

The PCI 9030 is a PCI Target device only; therefore, there is no access to the internal registers from the Local Bus. The Local Power Management Interrupt output (LPMINT#) is included to accommodate the PCI Power Management interface to a Local Bus.

The PCI 9030 asserts LPMINT# to request a Power State change to an external Local Bus Initiator when the Power Management Control/Status register (PMCSR[1:0]) changes. The LPMINT# interrupt is synchronous to the Local clock. When asserted, it is one clock-wide pulse.

External Local glue logic is needed to latch the Power State change and to retain the previous Power State history for further evaluation by the external Local Bus Initiator.

The PCI 9030 uses the PME#_Support bits (PMC[14:11]) to identify the PME# Support corresponding to a specific power state (PMCSR[1:0]). (PMC[14:11]) are configured by way of the serial EEPROM.

The Local Host then sets the PME#_Status bit (PMCSR[15]=1), by way of LPMESET, and the PCI 9030 asserts PME#. To clear the PME#_Status bit, the PCI Host must write a 1 to the PME# Status bit (PMCSR[15]=1). To disable the PME# Interrupt signal, either the PCI Host or serial EEPROM can write a 0 to the PME#_En bit (PMCSR[8]=0).

The Local Power Management Enumerator Set Interrupt input (LPMESET) is included to accommodate the PCI Power Management interface to a Local Bus.

The external Local Bus Initiator can assert LPMESET to the PCI 9030 Power Management Control/Status register (PMCSR[15]) to set the PME# status and assert the PME# signal in the case of a Wake-up Request event to the PCI Bus.

LPMINT# output is asserted every time the power state in the PMCSR register changes. Transition from state 11 (D_{3hot}) to state 00 (D_0) causes a soft reset and serial EEPROM reload. During a soft reset, the Local Bus interface is in Reset mode. The PCI 9030 issues LRESETo# and resets the Local Bus and all its Local Internal registers to their default values.

In state D_{3hot}, PCI Memory and I/O accesses are disabled, as well as PCI interrupts, and only configuration is allowed.

7.2.1 Power Management Data_Select, Data_Scale, and Power Data Utilization

The Data_Scale bits (PMCSR[14:13]) indicate the scaling factor to use when interpreting the value of the Power Management Data bits (PMDATA[7:0]). The value and meaning of the bits depend upon the data value specified in the Data_Select bits (PMCSR[12:9]). The Data_Scale bit value is unique for each Data_Select bit. For Data_Select values from 8 to 15, the Data_Scale bits always return a zero (PMCSR[14:13]=0).

To accommodate the PCI Power Management interface to a local bus, two hidden registers (loadable by the serial EEPROM) are available to store all necessary information for the Power Management Data and Data_Scale register bits—(PMDATASEL; PCI:70h) for PMDATA[7:0] and (PMDATASCALE; PCI:74h) for PMCSR[14:13], respectively.

The PCI 9030 supports only D_0, D_{3hot}, and D_{3cold}. Power Management States. Therefore, the PMDATA[7:0] register, which provides operating data (such as power consumption and/or heat dissipation), retains only four possible power data combinations:

1. D_0 Power Consumed
2. D_3 Power Consumed
3. D_0 Power Dissipated
4. D_{3hot} Power Dissipated

Each power combination field requires an 8-bit register in which to store the data. The PCI 9030 provides a 32-bit hidden register, PMDATASEL, to store such information. The PMDATASEL register can be written only from the serial EEPROM and read from the PMDATA[7:0] with the corresponding Data_Select value in the Power Management Control/Status register bits (PMCSR [12:9]).

The PMDATASEL register loading sequence from the serial EEPROM is as follows:

- Bits [31:24]—Data Select for D_{3hot} Power Dissipated
- Bits [23:16]—Data Select for D_0 Power Dissipated
- Bits [15:8]—Data Select for D_{3hot} Power Consumed
- Bits [7:0]—Data Select for D_0 Power Consumed

The Data_Scale register bits (PMCSR[14:13]) that provide a scale factor value for the Data_Select value retains four possible scale factors—0, 1, 2, and 3 (refer to *PCI Bus Power Management Interface Specification* v1.1 for the scale factor derivative values). Each Data_Scale field requires a 2-bit register in which to store the data. The PCI 9030 provides an 8-bit hidden register, PMDATASCALE, to store such information. The PMDATASCALE register can be written only from the serial EEPROM and read from the PMCSR[14:13] with the corresponding Data_Select value in the Power Management Control/ Status register bits (PMCSR [12:9]).

The loading sequence of the PMDATASCALE register from the serial EEPROM is as follows:

- Bits [7:6]—Data_Scale for D_{3hot} Power Dissipated
- Bits [5:4]—Data_Scale for D_0 Power Dissipated
- Bits [3:2]—Data_Scale for D_{3hot} Power Consumed
- Bits [1:0]—Data_Scale for D_0 Power Consumed

7.2.2 Reading Hidden Data Example

An example of reading hidden data follows:

1. PMCSR[12:9] Data_Select retains a value of 0h.

   PMCSR[14:13] provides a scale factor for the D_0 Power Consumed from the Data_Scale 0 bits (PMDATASCALE[1:0]).

   PMDATA[7:0] provides the D_0 Power Consumed value from the D_0 Power Consumed bits (PMDATASEL[7:0]).

2. PMCSR[12:9] Data_Select retains a value of 7h.

   PMCSR[14:13] provides a scale factor for the D_{3hot} Power Dissipated from the Data_Scale 7 bits (PMDATASCALE[7:6]).

   PMDATA[7:0] provides the D_{3hot} Power Dissipated value, from the D_3 Power Dissipated bits (PMDATASEL[31:24]).

7.3 SYSTEM CHANGES POWER MODE EXAMPLE

An example of system changes power mode follows:

1. The Host writes to the PCI 9030 PMCSR register to change the power states.
2. The PCI 9030 sends a Local Power Management Interrupt (LPMINT# output) to a Local CPU (LCPU).
3. The LCPU has 200 µs to respond to the power management information change (LPMINT#) from the PCI 9030 PMCSR register to implement the power saving function.
4. After the LCPU implements the power saving function, the PCI 9030 disables all PCI Target accesses and PCI Interrupt output (INTA#).

Notes: *In Power Saving mode, all PCI and Local Configuration cycles are granted.*

The PCI 9030 automatically performs a soft reset to a Local Bus on D_3-to-D_0 transitions.

7.4 WAKE-UP REQUEST EXAMPLE

An example of a wake-up request follows:

1. The add-in board (with a PCI 9030 chip installed) is in a powered-down state.
2. The Local CPU performs a LPMESET interrupt assertion (PCI 9030 PMCSR[15] register bit) to request a wake-up procedure.
3. As soon as the request is detected, the PCI 9030 drives PME# out to the PCI Bus.
4. The PCI Host accesses the PCI 9030 PMCSR register to disable the PME# output signal and restores the PCI 9030 to the D_0 power state.
5. The PCI 9030 completes the power management task by issuing the Local Power Management Interrupt (LPMINT# output) to the Local CPU, indicating that the power mode has changed.

8 COMPACTPCI HOT SWAP

The PCI 9030 is a CompactPCI Hot Swap *Ready*-compliant device.

8.1 OVERVIEW

Hot Swap is used for many CompactPCI applications. Hot Swap functionality allows the orderly insertion and removal of boards without adversely affecting system operation. This is done for repair of faulty boards or system reconfiguration. Additionally, Hot Swap provides access to Hot Swap services, allowing system reconfiguration and fault recovery to occur with no system down time and minimum operator interaction. Adapter insertion/removal logic control resides on the individual adapters. The PCI 9030 uses four pins—ENUM#, BD_SEL#, LEDon#, and CPCISW—to implement the hardware aspects of Hot Swap functionality. The PCI 9030 uses the Hot Swap Capabilities register to implement the software aspects of Hot Swap.

To avoid confusion in the industry, Hot Swap defines three levels of compatibility:

- Hot Swap-*Capable* devices contain the minimum requirements to operate in a Hot Swap environment
- Hot Swap-*Friendly* devices contain additional functions to ease the designer's job
- Hot Swap-*Ready* devices contain all necessary functions for Hot Swap

Hot Swap-*Capable* requirements are mandatory for a device to be used in a Hot Swap environment. These requirements are attributes for which a system user must compensate using external circuitry, as follows:

- *PCI Local Bus Specification* v2.1 compliance
- Tolerate Vcc from early power
- Tolerate asynchronous reset
- Tolerate precharge voltage
- I/O Buffers must meet modified V/I requirements
- Limited I/O pin leakage at precharge voltage

Hot Swap-*Friendly* silicon includes all required *Capable* functions and adds others from the following list. The PCI 9030 integrated these functions into the PCI silicon, thereby reducing the amount and cost of required external circuitry.

- **Incorporates Hot Swap Control/Status register (HS_CSR)**—Contained within the configuration space.
- **Incorporates an Extended Capability Pointer (ECP) mechanism**—It is required that Software retain a standard method of determining if a specific function is designed in accordance with the specification. The Capabilities Pointer is located within standard CSR space, using a bit in the PCI Status register (offset 04h).
- Incorporates remaining software connection control resources. Provides ENUM#, Hot Swap switch, and the blue LED.

Hot Swap-*Ready* silicon includes all required *Friendly* functions and adds others from the following list. The PCI 9030 integrated these functions into the PCI silicon, thereby reducing the amount and cost of external circuitry required.

- Early Power Support.
- **Incorporates a 1V BIAS precharge voltage to the PCI I/O pins**—All PCI Bus signals are required to be precharged to a 1V BIAS through a 10K ohm resistor during the Hot Swap process. The PCI 9030 provides an internal voltage regulator to supply 1V, with a built-in 10K ohm resistor, to all required PCI I/O buffers. Other PCI signals can be precharged to V_{IO}.

The PCI 9030 is a Hot Swap-*Ready* PCI silicon device. The PCI 9030 incorporates all compliant functions defined by the CompactPCI Hot Swap specification. The PCI 9030 incorporates LEDon#, CPCISW, BD_SEL#, and ENUM#, as well as Hot Swap Capabilities registers—HS_CNTL, HS_NEXT, and HS_CSR.

8.2 CONTROLLING CONNECTION PROCESSES

The following sections are excerpts from the *CompactPCI Hot Swap Specification*. Refer to the specification for more details.

8.2.1 Connection Control

Hardware Control provides a means for the platform to control the hardware connection process. The signals listed in the following sections must be

supported on all Hot Swap boards for interoperability. Implementations on different platforms may vary.

8.2.1.1 Board Slot Control

BD_SEL#, one of the shortest pins from the CompactPCI backplane, is driven low to enable power-on. For systems not implementing hardware control, it is grounded on the backplane.

Systems implementing hardware control radially connect BD_SEL# to a Hot Swap Controller (HSC). The controller terminates the signal with a weak pull-down, and can detect board present when the board pull-up overrides the pull-down. HSC can then control the power-on process by driving BD_SEL# low.

The PCI 9030 uses the BD_SEL# signal to tri-state all local output buffers during the insertion and extraction process. In addition, the PCI 9030 uses BD_SEL# as a qualifier to dynamically connect 1V and $V_{I/O}$ BIAS precharge resistors to all required PCI I/O buffers. A pull-up resistor must be provided to the BD_SEL# pin or add-in card, where the pull-up resistor is connected to an early power Power Supply, which provides for proper PCI 9030 operation. (Refer to Section 11, “Pin Description,” for precharge connections.)

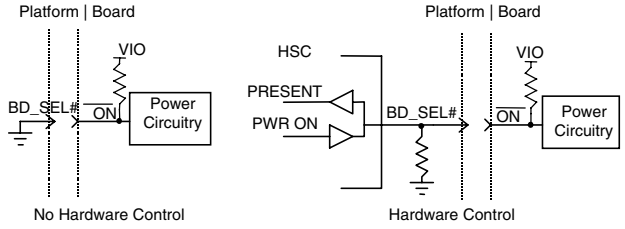


Figure 8-1. Redirection of BD_SEL#

8.2.1.2 Board Healthy

A second radial signal is used to acknowledge board health. It signals that a board is suitable to be released from reset and allowed onto the PCI Bus.

Minimally, this signal must be connected to the board’s power controller “power good” status line. Use of HEALTHY# can be expanded for applications requiring additional conditions to be met for the board to be considered healthy.

On platforms that do not use Hardware Connection Control, this line is not monitored. Platforms implementing this signaling, route these signals radially to a Hot Swap Controller.

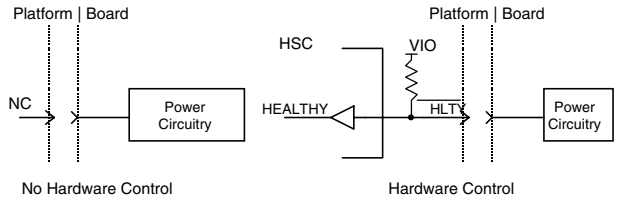


Figure 8-2. Board Healthy

8.2.1.3 Platform Reset

Reset (PCI_RST#), as defined by the *CompactPCI Specification*, is a bus signal on the backplane, driven by the Host. Platforms may implement this signal as a radial signal from the Hot Swap Controller to further control the electrical connection process. Platforms that maintain function of the bus signal, must *OR* the Host reset signal with the slot-specific signal.

Locally, boards must not exit reset until the H1 State is reached (healthy), and they must honor the backplane reset. The Local board reset (Local_PCI_RST#) must be the logical *OR* of these two conditions. Local_PCI_RST# is connected to the PCI 9030 RST# input pin.

During a BIAS voltage precharge and platform reset, in insertion and extraction procedures, all PCI I/O buffers must be in a high-impedance state. The PCI 9030 supports this condition when the Host RST# is asserted (PCI v2.1). To protect the Local board components from early power, the PCI 9030 floats the Local Bus I/Os. The BD_SEL# pin is used to perform the high-impedance condition on the Local Bus. With full contact of the add-in card to the backplane, BD_SEL# is asserted which ensures that the PCI 9030 asserts the LRESETo# signal to complete a Local Board Reset task.

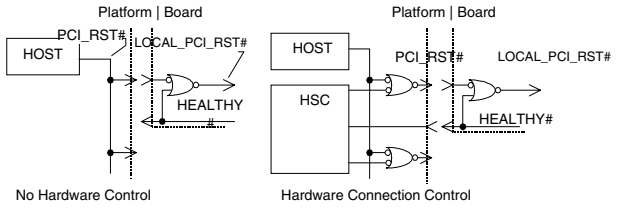


Figure 8-3. PCI Reset

8.2.2 Software Connection Control

Software Connection Control provides a means to control the Software Connection Process. Hot Swap board resources facilitate software Connection Control. Access to these resources occurs by way of the bus, using PCI protocol transfers (in-band).

These resources consist of four elements:

- ENUM# driven active indicates the need to change the Hot Swap Board state
- A switch, tied to the ejector, indicates the intent to remove a board
- LED indicates the software connection process status
- Control/Status register allows the software to interact with these resources

8.2.2.1 Ejector Switch and Blue LED

A microswitch (switch), located in the Hot Swap CompactPCI board card-ejector mechanism, is used to signal impending board removal. This signal asserts ENUM#. The operator normally activates the switch, waits for the LED illumination to indicate it may remove the board, and then removes the board. The PCI 9030 implements separate control logic for the microswitch and blue LED in two different pins (CPCISW and LEDon#, respectively).

When the ejector is opened or closed, the switch bounces for a time. The PCI 9030 uses internal debounce circuitry to clean the signal before the remainder of Hot Swap logic acknowledges it. The switch state is sampled six times, at 1 ms intervals, before it is determined to be closed or open.

The Blue “Status” LED, located on the front of the Hot Swap CompactPCI board, is illuminated when it is permissible to remove a board. The hardware connection layer provides protection for the system during all insertions and extractions. This LED indicates the system software is in a state that tolerates board extraction.

Upon insertion, the LED is automatically illuminated by the hardware until the hardware connection process completes. The LED remains *OFF* until the software uses it to indicate extraction is once again permitted.

The PCI 9030 uses an open-drain output pin to sink the external LED. The LED state is driven from the LED Software On/Off Switch bit (HS_CSR[3]).

The CPCISW input signal acknowledges the state ejector handle change to identify when a board is inserted or removed. The appropriate status bits are set (HS_CSR[7:6]).

8.2.2.2 ENUM#

ENUM# is provided to notify the Host CPU that a board was recently inserted or is about to be removed. This signal informs the CPU that system configuration changed, at which time the CPU performs necessary maintenance such as installing a device driver upon board insertion, or quiescing a device driver prior to board extraction.

ENUM# is an open collector bused signal with a pull-up on the Host bus. It may drive an interrupt (preferred) or be polled by the system software at regular intervals. The CompactPCI Hot-Plug System Driver on the system Host manages the ENUM# sensing. Full Hot Swap Boards assert ENUM# until serviced by the Hot-Plug system driver.

When a board is inserted into the system and comes out of reset, the PCI 9030 acknowledges the ejector switch state. If this switch is open (ejector handle closed), the PCI 9030 asserts the ENUM# interrupt and sets the ENUM# Status Indicator for Board Insertion bit (HS_CSR[7]). Once the Host CPU installs the proper drivers, it can logically include this board by clearing the interrupt.

When a board is about to be removed, the PCI 9030 acknowledges the ejector handle is open, asserts the ENUM# interrupt, and sets the ENUM# Status Indicator for the Board Removal bit (HS_CSR[6]). The Host then logically removes the board and turns on the LED, at which time the board can be removed from the system.

8.2.2.3 Hot Swap Control/Status Register (HS_CSR)

The PCI 9030 supports Hot Swap directly, as a control/status register is provided in Configuration space. This register is accessed through the PCI Extended Capabilities Pointer (ECP) mechanism.

The Hot Swap Control/Status register (HS_CSR) provides status read-back for the Hot-Plug System Driver to determine which board is driving ENUM#. This register is also used to control the Hot Swap Status LED on the board front panel, and to de-assert ENUM#.

8.2.2.4 Hot Swap Capabilities Register Bit Definition

31 24	23 16	15 8	7 0
Reserved	Control	Next_Cap Pointer	Hot Swap ID

Figure 8-4. Hot Swap Capabilities Register Bit Definition

Hot Swap ID. Bits [7:0] (HS_CNTL[7:0]; PCI:48h). These bits are set to a default value of 0x06.

Next_Cap Pointer. Bits [15:8] (HS_NEXT[7:0]; PCI:49h). These bits either point to the next New Capability structure, or are set to 0 if this is the last capability in the structure.

Control. Bits [23:16] (HS_CSR[7:0]; PCI:4Ah). This 8-bit control register is defined in the following table.

Table 8-1. Hot Swap Control

Bit	Description
23	ENUM# status—Insertion (1 = board is inserted).
22	ENUM# status—Removal (1 = board is being removed).
21	Not used.
20	Not used.
19	LED state (1 = LED on, 0 = LED off).
18	Not used.
17	ENUM# interrupt enable (1 = de-assert, 0 = enable interrupt).
16	Not used.

9 PCI VITAL PRODUCT DATA (VPD)

9.1 OVERVIEW

The *PCI Specification* v2.2 Vital Product Data (VPD) function defines a new location and access method. It also defines the Read Only and Read/Write bits. Currently Device ID, Vendor ID, Revision ID, Class Code, Subsystem ID, and Subsystem Vendor ID are required in the Configuration Space Header and for basic device identification and configuration. Although this information allows a device to be configured, it is not sufficient to allow a device to be uniquely identified. With the addition of VPD, optional information is provided that allows a device to be uniquely identified and tracked. These additional bits enable current and/or future support tools and reduces the total cost of ownership of PCs and systems.

This provides an alternate access method other than Expansion ROM for VPD. VPD is stored in an external serial EEPROM, which is accessed using the Configuration Space New Capabilities function.

The VPD registers—PVPDCNTL, PVPD_NEXT, PVPDAD, and PVPDATA—are not accessible for reads from the Local Bus. The VPD function can be exercised only from the PCI Bus.

9.2 VPD CAPABILITIES REGISTER

VPD ID. Bits [7:0] (PVPDCNTL[7:0]; PCI:4Ch). The PCI SIG assigned a value of 03h to these bits. The VPD ID is hardcoded.

Next_Cap Pointer. Bits [15:8] (PVPD_NEXT[7:0]; PCI:4Dh). These bits either point to the next New Capability structure, or are set to 0 if this is the last capability in the structure. The PCI 9030 defaults to 0x00. This value can be overwritten from the serial EEPROM.

VPD Address. Bits [24:16] (PVPAD[14:0]; PCI:4Eh). These bits specify the VPD byte address to be accessed. All accesses are 32-bit wide; bits [17:16] must be 0, with the maximum serial EEPROM size being 4K bits. Bits [30:25] are ignored.

F. Bit 31 (PVPDAD[15]; PCI:4Eh). This bit sets a flag to indicate when a serial EEPROM data operation is complete. For Write cycles, the four bytes of data are first written into the VPD Data bits, after which the VPD Address is written at the same time the F flag is set to 1. The F flag clears when the serial EEPROM Data transfer completes. For Read cycles, the VPD Address is written at the same time the F flag is cleared to 0. The F flag is set when four bytes of data are read from the serial EEPROM.

VPD Data. Bits [31:0] (PVPDATA[31:0]; PCI:50h). The VPDDATA register is not a pure read/write register. The data read from the register depends upon the last Read operation performed in PVPDAD[15]. VPD data is written or read through this register. Least-significant byte corresponding to VPD Byte at the address specified by the VPD Address register. Four bytes are always transferred between the register and the serial EEPROM.

31	30 16	15 8	7 0
F	VPD Address	Next_Cap Pointer (0X00)	VPD ID (0x03)
VPD Data			

Figure 9-1. VPD Capabilities Register Bit Definition

9.3 VPD SERIAL EEPROM PARTITIONING

To support VPD, the serial EEPROM is partitioned into read only and read/write sections.

9.4 SEQUENTIAL READ ONLY

The first 1024 bits, (128 bytes) of the serial EEPROM contain read-only information. The serial EEPROM read-only portion is loaded into the PCI 9030, using a sequential Read command to the serial EEPROM and occurs once after power-on or Hot Swap insertion.

9.5 RANDOM ACCESS READ AND WRITE

The PCI 9030 has full access to the read/write portion of the serial EEPROM. The serial EEPROM, starting at Lword Boundary for VPD Accesses bits (PROT_AREA[6:0]), designates this portion. This register is loaded upon power-on and can be written with a desired value, starting at location 0. This provides the capability of writing the entire serial EEPROM. Writes to the serial EEPROM are comprised of the following commands:

- Write Enable
- Write command, followed by the upper 16-bit Write data
- Write command, followed by the lower 16-bit Write data
- Write Disable

This is done to ensure against accidental write of the serial EEPROM. Randomly occurring cycles allow VPD information to be written and read at any time.

To perform a simple VPD write to the serial EEPROM, the following steps are necessary:

1. Change the write-protected serial EEPROM address in PROT_AREA[6:0], if required. 0x0000000 makes the serial EEPROM writable from the beginning.
2. Write the desired data into the VPDDATA register.
3. Write the destination serial EEPROM address and flag of operation to a value of 1.
4. Probe the flag of operation until it changes to a 0 to ensure the write is complete.

To perform a simple VPD read from the serial EEPROM, the following steps are necessary:

1. Write a destination serial EEPROM address and flag of operation to a value of 0.
2. Probe the flag of operation until it changes to a 1 to ensure the Read data is available.
3. Read back the VPDDATA register to see the requested data.

10 REGISTERS

10.1 NEW REGISTER DEFINITIONS SUMMARY (AS COMPARED TO THE PCI 9050 AND PCI 9052)

Refer to the description column in the following tables for a full explanation.

Table 10-1. New Registers Definitions Summary (As Compared to the PCI 9050 and PCI 9052)

PCI Register Address	Local Offset from Base Address	Register	Bits	Description
34h	—	New Capability Pointer	7:0	Provides offset into PCI Configuration space for the location of the first item in the New Capability Linked List.
40h	—	Power Management	31:0	Provides Power Management ID, Power Management Next Capability Pointer, and Power Management Capabilities.
44h	—	Power Management	31:0	Provides Power Management Status, PMCSR Bridge Support Extensions, and Power Management Data.
48h	—	CompactPCI Hot Swap	31:0	Hot Swap Control, Hot Swap Next Capability Pointer, and Hot Swap Control/Status Register.
4Ch	—	PCI Vital Product Data	31:0	VPD ID, VPD Next Capability Pointer, and VPD Address Pointer.
50h	—	PCI Vital Product Data	31:0	VPD Data.
—	4Eh	Serial EEPROM Write-Protected Address Boundary	6:0 15:7	Serial EEPROM Write-Protected Address Boundary. ***Reserved***.
—	50h	PCI Target Response, Serial EEPROM, and Initialization Control	5:0 6 7 8 9 11:10 31	***Reserved***. PCI Target Write FIFO Full Condition. Local Arbiter LGNT Select Enable. Local Ready Timeout Enable. Local Ready Timeout Select. PCI Target Write Delay Access Select. Disconnect with Flush Read FIFO.
—	54h	General Purpose I/O Control	26:0 31:27	GPIO[7:0] Control Select bits. ***Reserved.***
—	70h	Hidden 1 Power Management Data Select	31:0	Data Select register for Power Consumed and Dissipated. Written only by the serial EEPROM.
—	74h	Hidden 2 Power Management Data Scale	7:0 31:8	Data Scale Factor Values for Power Consumed and Dissipated. Written only by the serial EEPROM. ***Reserved.***

10.2 REGISTER ADDRESS MAPPING

Table 10-2. PCI Configuration Register Address Mapping

PCI Configuration Register Address	To ensure software compatibility with other versions of the PCI 9030 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 30 24 23 16 15 8 7 0	PCI Writable	Serial EEPROM Writable
00h	Device ID / Vendor ID	N	Y
04h	Status / Command	Y	Y [20]
08h	Class Code / Revision ID	N	Y
0Ch	BIST / Header Type / PCI Bus Latency Timer ***(Not supported)*** / Cache Line Size	Y [7:0]	N
10h	PCI Base Address 0; used for Memory-Mapped Configuration Registers (PCIBAR0)	Y	N
14h	PCI Base Address 1; used for I/O-Mapped Configuration Registers (PCIBAR1)	Y	N
18h	PCI Base Address 2; used for Local Address Space 0 (PCIBAR2)	Y	N
1Ch	PCI Base Address 3; used for Local Address Space 1 (PCIBAR3)	Y	N
20h	PCI Base Address 4; used for Local Address Space 2 (PCIBAR4)	Y	N
24h	PCI Base Address 5; used for Local Address Space 3 (PCIBAR5)	Y	N
28h	Cardbus CIS Pointer (***Not supported***)	N	N
2Ch	Subsystem ID / Subsystem Vendor ID	N	Y
30h	PCI Base Address for Local Expansion ROM	Y	N
34h	***Reserved*** / Next_Cap Pointer	N	Y [7:0]
38h	***Reserved***	N	N
3Ch	Max_Lat / Min_Gnt / Interrupt Pin / Interrupt Line	Y [7:0]	Y [15:8]
40h	Power Management Capabilities / Next_Cap Pointer / Capability ID	N	Y [30:27, 21, 19:16, 15:8]
44h	Data / PMCSR Bridge Support Extensions / Power Management Control/Status	Y [15, 12:8, 1:0]	Y [12:8]
48h	***Reserved*** / Control/Status / Next_Cap Pointer / Capability ID	Y [23:16]	Y [15:0]
4Ch	F / VPD Address / Next_Cap Pointer / Capability ID	Y [31:16]	Y [15:8]
50h	VPD Data	Y	N

Note: *Refer to PCI Specification* v2.2 *for definitions of these registers.*

Table 10-3. Local Configuration Register Address Mapping

PCI (Offset from Base Address)	To ensure software compatibility with other versions of the PCI 9030 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 0	PCI Writable	Serial EEPROM Writable
00h	Range for PCI-to-Local Address Space 0	Y	Y
04h	Range for PCI-to-Local Address Space 1	Y	Y
08h	Range for PCI-to-Local Address Space 2	Y	Y
0Ch	Range for PCI-to-Local Address Space 3	Y	Y
10h	Range for PCI-to-Local Expansion ROM	Y	Y
14h	Local Base Address (Remap) for PCI-to-Local Space 0	Y	Y
18h	Local Base Address (Remap) for PCI-to-Local Space 1	Y	Y
1Ch	Local Base Address (Remap) for PCI-to-Local Space 2	Y	Y
20h	Local Base Address (Remap) for PCI-to-Local Space 3	Y	Y
24h	Local Base Address (Remap) for PCI-to-Local Expansion ROM	Y	Y
28h	Local Bus Region Descriptor (Space 0) for PCI-to-Local Accesses	Y	Y
2Ch	Local Bus Region Descriptor (Space 1) for PCI-to-Local Accesses	Y	Y
30h	Local Bus Region Descriptor (Space 2) for PCI-to-Local Accesses	Y	Y
34h	Local Bus Region Descriptor (Space 3) for PCI-to-Local Accesses	Y	Y
38h	Local Bus Region Descriptor (Expansion ROM) for PCI-to-Local Accesses	Y	Y

Table 10-4. Chip Select Register Address Mapping

PCI (Offset from Base Address)	To ensure software compatibility with other versions of the PCI 9030 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 0	PCI Writable	Serial EEPROM Writable
3Ch	Local Chip Select 0 Base Address	Y	Y
40h	Local Chip Select 1 Base Address	Y	Y
44h	Local Chip Select 2 Base Address	Y	Y
48h	Local Chip Select 3 Base Address	Y	Y

Table 10-5. Runtime Register Address Mapping

PCI (Offset from Base Address)	To ensure software compatibility with other versions of the PCI 9030 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 28 27 24 23 16 15 0	PCI Writable	Serial EEPROM Writable
4Ch	***Reserved*** | Serial EEPROM Write-Protected Address Boundary | Interrupt Control/Status	Y [31:8]	Y
50h	PCI Target Response, Serial EEPROM Control, and Initialization Control	Y	Y
54h	***Reserved*** | General Purpose I/O Control	Y	Y
70h	Hidden 1 Register for Power Management Data Select, Power Consumed and Dissipated Values	N	Y
74h	Hidden 2 Register for Power Management Data Scale, Power Consumed and Dissipated Values	N	Y

10.3 PCI CONFIGURATION REGISTERS

All registers may be written to or read from in Byte, Word, or Lword accesses.

Register 10-1. (PCIIDR; PCI:00h) PCI Configuration ID

Bit	Description	Read	Write	Value after Reset
15:0	**Vendor ID.** Identifies manufacturer of device. Defaults to the PCI SIG-issued Vendor ID of PLX (10B5h) if blank or if no serial EEPROM is present.	Yes	Serial EEPROM	10B5h
31:16	**Device ID.** Identifies particular device. Defaults to PLX part number for PCI interface chip (9030h) if blank or no serial EEPROM is present.	Yes	Serial EEPROM	9030h

Register 10-2. (PCICR; PCI:04h) PCI Command

Bit	Description	Read	Write	Value after Reset
0	**I/O Space.** Writing a 1 allows the device to respond to I/O space accesses. Writing a 0 disables the device from responding to I/O space accesses.	Yes	Yes	0
1	**Memory Space.** Writing a 1 allows the device to respond to Memory Space accesses. Writing a 0 disables the device from responding to Memory Space accesses.	Yes	Yes	0
2	**Master Enable.** ***Not supported.***	Yes	No	0
3	**Special Cycle.** ***Not supported.***	Yes	No	0
4	**Memory Write and Invalidate Enable.** ***Not supported.***	Yes	No	0
5	**VGA Palette Snoop.** ***Not supported.***	Yes	No	0
6	**Parity Error Response.** Writing a 0 indicates parity error is ignored and the operation continues. Writing a 1 indicates parity checking is enabled.	Yes	Yes	0
7	**Wait Cycle Control.** Controls whether a device does address/data stepping. Writing a 0 indicates the device never does stepping. Writing a 1 indicates the device always does stepping. ***Note:*** *Hardcoded to 0.*	Yes	No	0
8	**SERR# Enable.** Writing a 1 enables SERR# driver. Writing a 0 disables SERR# driver.	Yes	Yes	0
9	**Fast Back-to-Back Enable.** Indicates what type of fast back-to-back transfers a Master can perform on the bus. Writing a 1 indicates fast back-to-back transfers can occur to any agent on the bus. Writing a 0 indicates fast back-to-back transfers can only occur to the same agent as in the previous cycle. ***Note:*** *Hardcoded to 0.*	Yes	No	0
15:10	***Reserved***.	Yes	No	0h

Register 10-3. (PCISR; PCI:06h) PCI Status

Bit	Description	Read	Write	Value after Reset
3:0	***Reserved.***	Yes	No	0h
4	**New Capability Functions Support.** Writing a 1 supports New Capabilities Functions. If enabled, the first New Capability Function ID is located at PCI Configuration offset [40h]. Can only be written from the serial EEPROM. Read-only from the PCI Bus.	Yes	Serial EEPROM	1
6:5	***Reserved.***	Yes	No	0
7	**Fast Back-to-Back Capable.** Writing a 1 indicates an adapter can accept fast back-to-back transactions. ***Note:*** *Hardcoded to 1.*	Yes	No	1
8	**Master Data Parity Error Detected.** ***Not supported.***	Yes	No	0
10:9	**DEVSEL# Timing.** Indicates timing for DEVSEL# assertion. Writing a 01 sets this bit to medium. ***Note:*** *Hardcoded to 01.*	Yes	No	01
11	**Target Abort.** When set to 1, indicates the PCI 9030 signaled a Target Abort. Writing a 1 clears this bit to 0.	Yes	Yes/Clr	0
12	**Received Target Abort.** When set to 1, indicates the PCI 9030 received a Target Abort signal. ***Not supported.***	Yes	No	0
13	**Received Master Abort.** When set to 1, indicates the PCI 9030 received a Master abort signal. ***Not supported.***	Yes	No	0
14	**Signaled System Error.** When set to 1, indicates the PCI 9030 reported a system error on SERR#. Writing a 1 clears this bit to 0.	Yes	Yes/Clr	0
15	**Detected Parity Error.** When set to 1, indicates the PCI 9030 detected a PCI Bus parity error, even if parity error handling is disabled (the Parity Error Response bit in the Command register is clear). One of three conditions can cause this bit to be set when the PCI 9030 detects a parity error: 1) During PCI Address phase; 2) When it was the Target of a write; 3) When performing Master Read operation. Writing a 1 clears this bit to 0.	Yes	Yes/Clr	0

Register 10-4. (PCIREV; PCI:08h) PCI Revision ID

Bit	Description	Read	Write	Value after Reset
7:0	**Revision ID.** PCI 9030 Silicon revision.	Yes	Serial EEPROM	Current Rev #

Register 10-5. (PCICCR; PCI:09-0Bh) PCI Class Code

Bit	Description	Read	Write	Value after Reset
7:0	**Register Level Programming Interface.** None defined.	Yes	Serial EEPROM	0h
15:8	**Subclass Code (Other Bridge Device).**	Yes	Serial EEPROM	80h
23:16	**Base Class Code (Bridge Device).**	Yes	Serial EEPROM	06h

Register 10-6. (PCICLSR; PCI:0Ch) PCI Cache Line Size

Bit	Description	Read	Write	Value after Reset
7:0	**System Cache Line Size.** Specified in units of 32-bit words (8 or 16 Lwords). Can be written and read; however, the value has no effect on chip operation.	Yes	Yes	0h

Register 10-7. (PCILTR; PCI:0Dh) PCI Bus Latency Timer

Bit	Description	Read	Write	Value after Reset
7:0	**PCI Bus Latency Timer.** ***Not supported***.	Yes	No	0h

Register 10-8. (PCIHTR; PCI:0Eh) PCI Header Type

Bit	Description	Read	Write	Value after Reset
6:0	**Configuration Layout Type.** Specifies layout of bits 10h through 3Fh in configuration space. Only one encoding, 0h, is defined. All other encodings are ***reserved***.	Yes	No	0h
7	**Header Type.** Writing a 1 indicates multiple functions. Writing a 0 indicates single function.	Yes	No	0

Register 10-9. (PCIBISTR; PCI:0Fh) PCI Built-In Self Test (BIST)

Bit	Description	Read	Write	Value after Reset
7:0	**Built-In Test.** Value of 0 indicates device passed its test. ***Not supported***.	Yes	No	0h

Register 10-10. (PCIBAR0; PCI:10h) PCI Base Address Register for Memory Accesses to Local Registers

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing a 0 indicates the register maps into Memory space. Writing a 1 indicates the register maps into I/O space. ***Note:*** *Hardcoded to 0.*	Yes	No	0
2:1	**Location of Register.** Values: 00—Locate anywhere in 32-bit Memory Address space 01—Locate below 1-MB Memory Address space 10—Locate anywhere in 64-bit Memory Address space 11—***Reserved*** ***Note:*** *Hardcoded to 00.*	Yes	No	00
3	**Prefetchable.** Writing a 1 indicates there are no side effects on reads. Does not affect the PCI 9030 operation. ***Note:*** *Hardcoded to 0.*	Yes	No	0
6:4	**Memory Base Address.** Memory base address for access to Local registers (requires 128 bytes). ***Note:*** *Hardcoded to 0h.*	Yes	No	0h
31:7	**Memory Base Address.** Memory base address for access to Local registers.	Yes	Yes	0h

Register 10-11. (PCIBAR1; PCI:14h) PCI Base Address Register for I/O Accesses to Local Registers

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing a 0 indicates the register maps into Memory space. Writing a 1 indicates the register maps into I/O space. ***Note:*** *Hardcoded to 1.*	Yes	No	1
1	***Reserved.***	Yes	No	0
6:2	**I/O Base Address.** Base Address for I/O access to Local registers (requires 128 bytes). ***Note:*** *Hardcoded to 0h.*	Yes	No	0h
31:7	**I/O Base Address.** Base Address for I/O access to Local registers.	Yes	Yes	0h

Register 10-12. (PCIBAR2; PCI:18h) PCI Base Address Register for Memory Accesses to Local Address Space 0

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing a 0 indicates the register maps into Memory space. Writing a 1 indicates the register maps into I/O space. (Specified in the LAS0RR register.)	Yes	No	0
2:1	**Location of Register (If Memory Space).** Values: 00—Locate anywhere in 32-bit Memory Address space 01—Locate below 1-MB Memory Address space 10—Locate anywhere in 64-bit Memory Address space 11—***Reserved*** (Specified in the LAS0RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: bit 1 no, bit 2 yes	00
3	**Prefetchable (If Memory Space).** Writing a 1 indicates there are no side effects on reads. Reflects value of LAS0RR[3] and provides only status to the system. Does not affect PCI 9030 operation. The associated Bus Region Descriptor register controls prefetching functions of this address space. (Specified in the LAS0RR register.) If I/O Space, bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	**Memory Base Address.** Memory base address for access to Local Address Space 0. PCIBAR2 can be enabled or disabled by setting or clearing the Space 0 Enable bit (LAS0BA[0]).	Yes	Yes	0h

Note: *PCIBAR2 can be enabled or disabled by setting or clearing LAS0BA[0].*

Register 10-13. (PCIBAR3; PCI:1Ch) PCI Base Address Register for Memory Accesses to Local Address Space 1

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing a 0 indicates the register maps into Memory space. Writing a 1 indicates the register maps into I/O space. (Specified in the LAS1RR register.)	Yes	No	0
2:1	**Location of Register.** Values: 00—Locate anywhere in 32-bit Memory Address space 01—Locate below 1-MB Memory Address space 10—Locate anywhere in 64-bit Memory Address space 11—***Reserved*** (Specified in the LAS1RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 No, Bit 2 Yes	00
3	**Prefetchable (If Memory Space).** Writing a 1 indicates there are no side effects on reads. Reflects value of LAS1RR[3] and provides only status to the system. Does not affect PCI 9030 operation. The associated Bus Region Descriptor register controls prefetching functions of this address space. (Specified in the LAS1RR register.) If I/O Space, bit 3 is included in base address.	Yes	Mem: No I/O: Yes	0
31:4	**Memory Base Address.** Memory base address for access to Local Address Space 1. PCIBAR3 can be enabled or disabled by setting or clearing the Space 1 Enable bit (LAS1BA[0]).	Yes	Yes	0h

Note: *PCIBAR3 can be enabled or disabled by setting or clearing LAS1BA[0].*

Register 10-14. (PCIBAR4; PCI:20h) PCI Base Address Register for Memory Accesses to Local Address Space 2

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing a 0 indicates the register maps into Memory space. Writing a 1 indicates the register maps into I/O space. (Specified in the LAS2RR register.)	Yes	No	0
2:1	**Location of Register.** Values: 00—Locate anywhere in 32-bit Memory Address space 01—Locate below 1-MB Memory Address space 10—Locate anywhere in 64-bit Memory Address space 11—***Reserved*** (Specified in the LAS2RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 No, Bit 2 Yes	00
3	**Prefetchable (If Memory Space).** Writing a 1 indicates there are no side effects on reads. Reflects value of LAS2RR[3] and provides only status to the system. Does not affect the PCI 9030 operation. The associated Bus Region Descriptor register controls prefetching functions of this address space. (Specified in the LAS2RR register.) If I/O Space, bit 3 is included in base address.	Yes	Mem: No I/O: Yes	0
31:4	**Memory Base Address.** Memory base address for access to Local Address Space 2. PCIBAR4 can be enabled or disabled by setting or clearing the Space 2 Enable bit (LAS2BA[0]).	Yes	Yes	0h

Note: *PCIBAR4 can be enabled or disabled by setting or clearing LAS2BA[0].*

Register 10-15. (PCIBAR5; PCI:24h) PCI Base Address Register for Memory Accesses to Local Address Space 3

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing a 0 indicates the register maps into Memory space. Writing a 1 indicates the register maps into I/O space. (Specified in the LAS3RR register.)	Yes	No	0
2:1	**Location of Register.** Values: 00—Locate anywhere in 32-bit Memory Address space 01—Locate below 1-MB Memory Address space 10—Locate anywhere in 64-bit Memory Address space 11—***Reserved*** (Specified in the LAS3RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 No, Bit 2 Yes	00
3	**Prefetchable (If Memory Space).** Writing a 1 indicates there are no side effects on reads. Reflects value of LAS3RR[3] and provides only status to the system. Does not affect the PCI 9030 operation. The associated Bus Region Descriptor register controls prefetching functions of this address space. (Specified in the LAS3RR register.) If I/O Space, bit 3 is included in base address.	Yes	Mem: No I/O: Yes	0
31:4	**Memory Base Address.** Memory base address for access to Local Address Space 3. PCIBAR5 can be enabled or disabled by setting or clearing the Space 3 Enable bit (LAS3BA[0]).	Yes	Yes	0h

Note: *PCIBAR5 can be enabled or disabled by setting or clearing LAS3BA[0].*

Register 10-16. (PCICIS; PCI:28h) PCI Cardbus CIS Pointer

Bit	Description	Read	Write	Value after Reset
31:0	**Cardbus Information Structure Pointer for PCMCIA. *Not supported*.**	Yes	No	0h

Register 10-17. (PCISVID; PCI:2Ch) PCI Subsystem Vendor ID

Bit	Description	Read	Write	Value after Reset
15:0	**Subsystem Vendor ID (Unique Add-in Board Vendor ID).**	Yes	Serial EEPROM	0h

Register 10-18. (PCISID; PCI:2Eh) PCI Subsystem ID

Bit	Description	Read	Write	Value after Reset
15:0	**Subsystem ID (Unique Add-in Board Device ID).**	Yes	Serial EEPROM	0h

Register 10-19. (PCIERBAR; PCI:30h) PCI Expansion ROM Base

Bit	Description	Read	Write	Value after Reset
0	**Address Decode Enable.** Writing a 1 indicates a device accepts accesses to the Expansion ROM space. Writing a 0 indicates a device does not accept accesses to Expansion ROM space. Should be set to 0 if there is no Expansion ROM. Works in conjunction with EROMRR[0].	Yes	Yes	0
10:1	***Reserved***.	Yes	No	0h
31:11	**Expansion ROM Base Address (upper 21 bits).**	Yes	Yes	0h

Register 10-20. (CAP_PTR; PCI:34h) New Capability Pointer

Bit	Description	Read	Write	Value after Reset
7:0	**New Capability Pointer.** Provides an offset into PCI Configuration Space for location of the first item in the New Capabilities Linked List.	Yes	Serial EEPROM	40h
31:8	***Reserved.***	Yes	No	0h

Register 10-21. (PCIILR; PCI:3Ch) PCI Interrupt Line

Bit	Description	Read	Write	Value after Reset
7:0	**Interrupt Line Routing Value.** Value indicates which input of the system interrupt controller(s) is connected to each device interrupt line.	Yes	Yes	0h

Register 10-22. (PCIIPR; PCI:3Dh) PCI Interrupt Pin

Bit	Description	Read	Write	Value after Reset
7:0	**Interrupt Pin Register.** Indicates which interrupt pin the device uses. The following values are decoded (the PCI 9030 supports only INTA#): 0 = No Interrupt Pin 1 = INTA# 2 = INTB# 3 = INTC# 4 = INTD#	Yes	Serial EEPROM	1h

Register 10-23. (PCIMGR; PCI:3Eh) PCI Min_Gnt

Bit	Description	Read	Write	Value after Reset
7:0	**Min_Gnt.** Specifies how long a Burst period device needs, assuming a clock rate of 33 MHz. Value is a multiple of 1/4 µs increments. ***Not Supported.***	Yes	No	0h

Register 10-24. (PCIMLR; PCI:3Fh) PCI Max_Lat

Bit	Description	Read	Write	Value after Reset
7:0	**Max_Lat.** Specifies how often the device must gain access to the PCI Bus. Value is a multiple of 1/4 µs increments. ***Not Supported.***	Yes	No	0h

Register 10-25. (PMCAPID; PCI:40h) Power Management Capability ID

Bit	Description	Read	Write	Value after Reset
7:0	**Power Management Capability ID.**	Yes	No	1h

Register 10-26. (PMNEXT; PCI:41h) Power Management Next Capability Pointer

Bit	Description	Read	Write	Value after Reset
7:0	**Next_Cap Pointer.** Points to the first location of the next item in the capabilities linked list. If power management is the last item in the list, set this register to 0.	Yes	Serial EEPROM	48h

Register 10-27. (PMC; PCI:42h) Power Management Capabilities

Bit	Description	Read	Write	Value after Reset
2:0	**Version.** Writing a 1 indicates this function complies with *PCI Bus Power Management Interface Specification* v1.1.	Yes	Serial EEPROM	001
3	**PCI Clock Required for PME# Signal.** When set to 1, indicates a function relies on PCI clock presence for PME# operation. The PCI 9030 does not require the PCI clock for PME#, so this bit should set to 0.	Yes	Serial EEPROM	0
4	**Auxiliary Power Source.** Because the PCI 9030 does not support PME# while in a D_{3cold} state, this bit is always set to 0. ***Not supported.***	Yes	No	0
5	**DSI.** When set to 1, the PCI 9030 requires special initialization following a transition to a D_0 uninitialized state before a generic class device driver is able to use it.	Yes	Serial EEPROM	0
8:6	***Reserved.***	Yes	No	000
9	**D_1_Support.** When set to 1, the PCI 9030 supports the D_1 power state. ***Not supported.***	Yes	No	0
10	**D_2_Support.** When set to 1, the PCI 9030 supports the D_2 power state. ***Not supported.***	Yes	No	0
14:11	**PME#_Support.** Indicates power states in which the PCI 9030 may assert PME#. Value Description XXX1 PME# can be asserted from D_0 1XXX PME# can be asserted from D_{3hot}	Yes	Serial EEPROM	9h
15	***Reserved.***	Yes	No	0

Register 10-28. (PMCSR; PCI:44h) Power Management Control/Status

Bit	Description	Read	Write	Value after Reset
1:0	**Power State.** Determines or changes the current power state. Value State 00 D_0 11 D_{3hot} Transition from a D_{3hot} state to a D_0 state causes a soft reset. Should only be initiated from the PCI Bus because the Local Bus interface is reset during a soft reset. In a D_{3hot} state, PCI Memory and I/O accesses are disabled, as well as PCI interrupts, and only configuration is allowed.	Yes	Yes	00
7:2	***Reserved.***	Yes	No	0h
8	**PME#_En.** Writing a 1 enables PME# to be asserted.	Yes	Yes/ Serial EEPROM	0
12:9	**Data_Select.** Selects which data to report through the Data register and Data_Scale bits.	Yes	Yes/ Serial EEPROM	0h
14:13	**Data_Scale.** Indicates the scaling factor to use when interpreting the Data register value. Value and meaning of this bit depends on the data value selected by the Data_Select bit. When the Local CPU initializes the Data_Scale values, it must use the Data_Select bit to determine which Data_Scale value it is writing. For Power Consumed and Power Dissipated data, the following scale factors are used. Unit values are in watts. Value Scale 0 Unknown 1 0.1x 2 0.01x 3 0.001x ***Note:*** *Information regarding hidden register use is provided in Section 7.2.1.*	Yes	Serial EEPROM by way of PMDATASCALE	00
15	**PME#_Status.** Indicates PME# is being driven if the PME#_En bit is set (PMCSR[8]=1). Writing a 1 from the Local Bus sets this bit; writing a 1 from the PCI Bus clears this bit to 0. Depending on the current power state, set only if the appropriate PME#_Support bit(s) is set (PMC[15:11]=1).	Yes	Local Interrupt/Set, PCI/Clr	0

Register 10-29. (PMCSR_BSE; PCI:46h) PMCSR Bridge Support Extensions

Bit	Description	Read	Write	Value after Reset
7:0	***Reserved.***	Yes	No	0h

Register 10-30. (PMDATA; PCI:47h) Power Management Data

Bit	Description	Read	Write	Value after Reset
7:0	**Power Management Data.** Provides operating data, such as power consumed or heat dissipation. Data returned is selected by the Data_Select bit(s) (PMCSR[12:9]) and scaled by the Data_Scale bit(s) (PMCSR[14:13]). Data_Select — Description 0 — D_0 Power Consumed 1 — ***Reserved*** 2 — ***Reserved*** 3 — D_3 Power Consumed 4 — D_0 Power Dissipated 5 — ***Reserved*** 6 — ***Reserved*** 7 — D_{3hot} Power Dissipated ***Note:*** *Information regarding hidden register use is provided in Section 7.2.1.*	Yes	Serial EEPROM by way of PMDATASEL	0h

Register 10-31. (HS_CNTL; PCI:48h) Hot Swap Control

Bit	Description	Read	Write	Value after Reset
7:0	**Hot Swap ID.**	Yes	Serial EEPROM	06h

Register 10-32. (HS_NEXT; PCI:49h) Hot Swap Next Capability Pointer

Bit	Description	Read	Write	Value after Reset
7:0	**Next_Cap Pointer.** Points to the first location of the next item in the capabilities linked list. If Hot Swap is the last item in the list, this register should be set to zero.	Yes	Serial EEPROM	4Ch

Register 10-33. (HS_CSR; PCI:4Ah) Hot Swap Control/Status

Bit	Description	Read	Write	Value after Reset
0	***Reserved.***	Yes	No	0
1	**ENUM# Interrupt Mask.** Writing a 0 enables the interrupt. Writing a 1 masks the interrupt.	Yes	PCI	0
2	***Reserved.***	Yes	No	0
3	**LED Software On/Off Switch.** Writing a 1 turns on the LED. Writing a 0 turns off the LED.	Yes	PCI	0
5:4	***Reserved.***	Yes	No	00
6	**ENUM# Status Indicator for Board Removal.** Value of 1 reports the ENUM# assertion for removal process. Writing a 1 clears the ENUM# Interrupt and Status bit.	Yes	PCI/Clr	0
7	**ENUM# Status Indicator for Board Insertion.** Value of 1 reports the ENUM# assertion for the insertion process. Writing a 1 clears the ENUM# Interrupt and Status bit.	Yes	PCI/Clr	0
15:8	***Reserved.***	Yes	No	0h

Register 10-34. (PVPDCNTL; PCI:4Ch) PCI Vital Product Data Control

Bit	Description	Read	Write	Value after Reset
7:0	**VPD ID.** Capability ID = 03h for VPD.	PCI	No	03h

Register 10-35. (PVPD_NEXT; PCI:4Dh) PCI Vital Product Data Next Capability Pointer

Bit	Description	Read	Write	Value after Reset
7:0	**Next_Cap Pointer.** Points to first location of next item in the capabilities linked list. VPD is the last item in the New Capabilities Linked List. This register is set to 0h.	PCI	Serial EEPROM	0h

Register 10-36. (PVPDAD; PCI:4Eh) PCI Vital Product Data Address

Bit	Description	Read	Write	Value after Reset
14:0	**VPD Address.** Byte address of the VPD address to be accessed. Supports 2K- or 4K-bit serial EEPROM.	PCI	Yes	0h
15	**F.** Flag used to indicate when the transfer of data between PVPDATA and the storage component is complete. Writing a 0 along with the VPD address causes a read of VPD information into PVPDATA. The hardware sets this bit to 1 when the VPD Data transfer is complete. Writing a 1 along with the VPD address causes a write of VPD information from PVPDATA into a storage component. The hardware sets this bit to 0 after the Write operation is complete.	PCI	Yes	0

Register 10-37. (PVPDATA; PCI:50h) PCI VPD Data

Bit	Description	Read	Write	Value after Reset
31:0	**VPD Data Register.**	PCI	Yes	0h

10.4 LOCAL CONFIGURATION REGISTERS

Register 10-38. (LAS0RR; 00h) Local Address Space 0 Range Register for PCI-to-Local Bus

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing a 0 indicates Local Address Space 0 maps into PCI Memory space. Writing a 1 indicates address Space 0 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 2/1 Meaning 0 0 Locate anywhere in 32-bit PCI Address space 0 1 Locate below 1 MB in PCI Address space 1 0 Locate anywhere in 64-bit PCI Address space 1 1 ***Reserved*** When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [27:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing a 1 indicates reads are prefetchable (does not affect the PCI 9030 operation, but is used for system status). When mapped into I/O space, it is included with bits [27:2] to indicate the decoding range.	Yes	Yes	0
27:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Bus Space 0. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIBAR2). Default is 1 MB. ***Notes:*** *Range (**not** Range register) must be power of 2. "Range register value" is inverse of range.* *User should limit all I/O spaces to 256 bytes per "PCI Specification v2.2."*	Yes	Yes	FF0000h
31:28	***Reserved.*** (PCI address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 10-39. (LAS1RR; 04h) Local Address Space 1 Range Register for PCI-to-Local Bus

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing a 0 indicates Local Address Space 1 maps into PCI Memory space. Writing a 1 indicates address Space 1 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 2/1 Meaning 0 0 Locate anywhere in 32-bit PCI Address space 0 1 Locate below 1 MB in PCI Address space 1 0 Locate anywhere in 64-bit PCI Address space 1 1 ***Reserved*** When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [27:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing a 1 indicates reads are prefetchable (does not affect the PCI 9030 operation, but is used for system status). When mapped into I/O space, it is included with bits [27:2] to indicate the decoding range.	Yes	Yes	0
27:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Bus Space 1. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIBAR3). ***Notes:*** *Range (**not** Range register) must be power of 2. "Range register value" is inverse of range.* *User should limit all I/O spaces to 256 bytes per "PCI Specification v2.2."*	Yes	Yes	000000h
31:28	***Reserved.*** (PCI address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 10-40. (LAS2RR; 08h) Local Address Space 2 Range Register for PCI-to-Local Bus

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing a 0 indicates Local Address Space 2 maps into PCI Memory space. Writing a 1 indicates address Space 2 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 2/1 Meaning 0 0 Locate anywhere in 32-bit PCI Address space 0 1 Locate below 1 MB in PCI Address space 1 0 Locate anywhere in 64-bit PCI Address space 1 1 ***Reserved*** When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [27:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing a 1 indicates reads are prefetchable (does not affect the PCI 9030 operation, but is used for system status). When mapped into I/O space, it is included with bits [27:2] to indicate the decoding range.	Yes	Yes	0
27:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Bus Space 2. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIBAR4). ***Notes:*** *Range (**not** Range register) must be power of 2. "Range register value" is inverse of range.* *User should limit all I/O spaces to 256 bytes per "PCI Specification v2.2."*	Yes	Yes	000000h
31:28	***Reserved.*** (PCI address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 10-41. (LAS3RR; 0Ch) Local Address Space 3 Range Register for PCI-to-Local Bus

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing a 0 indicates Local Address Space 3 maps into PCI Memory space. Writing a 1 indicates address Space 3 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 2/1 Meaning 0 0 Locate anywhere in 32-bit PCI Address space 0 1 Locate below 1 MB in PCI Address space 1 0 Locate anywhere in 64-bit PCI Address space 1 1 ***Reserved*** When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [27:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing a 1 indicates reads are prefetchable (does not affect the PCI 9030 operation, but is used for system status). When mapped into I/O space, it is included with bits [27:2] to indicate the decoding range.	Yes	Yes	0
27:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Bus Space 3. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIBAR5). ***Notes:*** *Range (**not** Range register) must be power of 2. "Range register value" is inverse of range.* *User should limit all I/O spaces to 256 bytes per "PCI Specification v2.2."*	Yes	Yes	000000h
31:28	***Reserved.*** (PCI address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 10-42. (EROMRR; 10h) Expansion ROM Range

Bit	Description	Read	Write	Value after Reset
0	**Address Decode Enable.** Bit 0 can only be enabled from the serial EEPROM. To disable, set PCI Expansion ROM Address Decode Enable bit to 0 (PCIERBAR[0]=0; 30h).	Yes	Serial EEPROM Only	0
10:1	***Reserved.***	Yes	No	0h
27:11	Specifies which PCI Address bits to use for decoding a PCI-to-Local Bus Expansion ROM. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to address bit 31. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIERBAR). Default is 64 KB. ***Note:*** *Range (**not** Range register) must be power of 2. "Range register value" is inverse of range.*	Yes	Yes	1111111111110 0000
31:28	***Reserved.*** (PCI address bits [31:28] are always included in decoding.)	Yes	Yes	1111

Register 10-43. (LAS0BA; 14h) Local Address Space 0 Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
0	**Space 0 Enable.** Writing a 1 enables decoding of PCI addresses for PCI Target access to Local Bus Space 0. Writing a 0 disables decoding.	Yes	Yes	1
1	***Reserved.***	Yes	No	0
3:2	If Local Bus Space 0 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [27:4] for remapping.	Yes	Yes	00
27:4	**Remap PCI Address to Local Address Space 0 into Local Address Space.** Bits in this register remap (replace) PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a Range multiple (**not** the Range register).*	Yes	Yes	0h
31:28	***Reserved.*** (Local address bits [31:28] do not exist in the PCI 9030.)	Yes	No	0h

Register 10-44. (LAS1BA; 18h) Local Address Space 1 Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
0	**Space 1 Enable.** Writing a 1 enables decoding of PCI addresses for PCI Target access to Local Bus Space 1. Writing a 0 disables decoding. PCIBAR3 can be enabled or disabled by setting or clearing this bit.	Yes	Yes	0
1	***Reserved.***	Yes	No	0
3:2	If Local Bus Space 1 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [27:4] for remapping.	Yes	Yes	00
27:4	**Remap PCI Address to Local Address Space 1 into Local Address Space.** Bits in this register remap (replace) PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a Range multiple (**not** the Range register).*	Yes	Yes	0h
31:28	***Reserved.*** (Local address bits [31:28] do not exist in the PCI 9030.)	Yes	No	0h

Register 10-45. (LAS2BA; 1Ch) Local Address Space 2 Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
0	**Space 2 Enable.** Writing a 1 enables decoding of PCI addresses for PCI Target access to Local Bus Space 2. Writing a 0 disables decoding. PCIBAR4 can be enabled or disabled by setting or clearing this bit.	Yes	Yes	0
1	***Reserved.***	Yes	No	0
3:2	If Local Bus Space 2 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [27:4] for remapping.	Yes	Yes	00
27:4	**Remap PCI Address to Local Address Space 2 into Local Address Space.** Bits in this register remap (replace) PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a Range multiple (**not** the Range register).*	Yes	Yes	0h
31:28	***Reserved.*** (Local address bits [31:28] do not exist in the PCI 9030.)	Yes	No	0h

Register 10-46. (LAS3BA; 20h) Local Address Space 3 Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
0	**Space 3 Enable.** Writing a 1 enables decoding of PCI addresses for PCI Target access to Local Bus Space 3. Writing a 0 disables decoding. PCIBAR5 can be enabled or disabled by setting or clearing this bit.	Yes	Yes	0
1	***Reserved.***	Yes	No	0
3:2	If Local Bus Space 3 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [27:4] for remapping.	Yes	Yes	00
27:4	**Remap PCI Address to Local Address Space 3 into Local Address Space.** Bits in this register remap (replace) PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a Range multiple (**not** the Range register).*	Yes	Yes	0h
31:28	***Reserved.*** (Local address bits [31:28] do not exist in the PCI 9030.)	Yes	No	0h

Register 10-47. (EROMBA; 24h) Expansion ROM Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
10:0	***Reserved.***	Yes	No	0h
27:11	**Remap PCI Expansion ROM Space into Local Address Space.** Bits in this register remap (replace) the PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a Range multiple (**not** the Range register).*	Yes	Yes	00000001000000000
31:28	***Reserved.*** (Local address bits [31:28] do not exist in the PCI 9030.)	Yes	No	0h

Register 10-48. (LAS0BRD; 28h) Local Address Space 0 Bus Region Descriptor

Bit	Description	Read	Write	Value after Reset
0	**Memory Space 0 Burst Enable.** Writing a 1 enables bursting. Writing a 0 disables bursting. Bursting occurs only if Prefetch Count is not equal to 00.	Yes	Yes	0
1	**Memory Space 0 READY# Input Enable.** Writing a 1 enables READY# input. Writing a 0 disables READY# input.	Yes	Yes	0
2	**Memory Space 0 BTERM# Input Enable.** Writing a 1 enables BTERM# input. Writing a 0 disables BTERM# input. For more information, refer to Section 2.2.4.3.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (prefetch count enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch four Lwords if bit 5 is set. 10 = Prefetch eight Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Counter Enable.** When set to 1 and Memory prefetching is enabled, the PCI 9030 prefetches up to the number of Lwords specified in prefetch count. When set to 0, the PCI 9030 ignores the count and continues prefetching until it is terminated by the PCI Bus.	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0h
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3).	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3).	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0h
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3).	Yes	Yes	00
23:22	**Memory Space 0 Local Bus Width.** Writing a 00 indicates an 8-bit bus width. Writing a 01 indicates a 16-bit bus width. Writing a 10 indicates a 32-bit bus width. ***Note:*** *Setting of 11 is* ***reserved****.*	Yes	Yes	10
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Writing a 1 specifies that in any Endian mode, use byte lanes [31:16] for a 16-bit Local Bus and byte lanes [31:24] for an 8-bit Local Bus. Writing a 0 specifies that in any Endian mode, use byte lanes [15:0] for a 16-bit Local Bus and byte lanes [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD strobe is asserted (0-3). Value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR strobe is asserted (0-3). Value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until end of cycle (0-3).	Yes	Yes	00

Register 10-49. (LAS1BRD; 2Ch) Local Address Space 1 Bus Region Descriptor

Bit	Description	Read	Write	Value after Reset
0	**Memory Space 1 Burst Enable.** Writing a 1 enables bursting. Writing a 0 disables bursting. Bursting occurs only if Prefetch Count is not equal to 00.	Yes	Yes	0
1	**Memory Space 1 READY# Input Enable.** Writing a 1 enables READY# input. Writing a 0 disables READY# input.	Yes	Yes	0
2	**Memory Space 1 BTERM# Input Enable.** Writing a 1 enables BTERM# input. Writing a 0 disables BTERM# input. For more information, refer to Section 2.2.4.3.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (prefetch count enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch four Lwords if bit 5 is set. 10 = Prefetch eight Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Counter Enable.** When set to 1 and Memory prefetching is enabled, the PCI 9030 prefetches up to the number of Lwords specified in prefetch count. When set to 0, the PCI 9030 ignores the count and continues prefetching until it is terminated by the PCI Bus.	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0h
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3).	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3).	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0h
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3).	Yes	Yes	00
23:22	**Memory Space 1 Local Bus Width.** Writing a 00 indicates an 8-bit bus width. Writing a 01 indicates a 16-bit bus width. Writing a 10 indicates a 32-bit bus width. ***Note:*** *Setting of 11 is* ***reserved****.*	Yes	Yes	10
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Writing a 1 specifies that in any Endian mode, use byte lanes [31:16] for a 16-bit Local Bus and byte lanes [31:24] for an 8-bit Local Bus. Writing a 0 specifies that in any Endian mode, use byte lanes [15:0] for a 16-bit Local Bus and byte lanes [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD strobe is asserted (0-3). Value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR strobe is asserted (0-3). Value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until end of cycle (0-3).	Yes	Yes	00

Register 10-50. (LAS2BRD; 30h) Local Address Space 2 Bus Region Descriptor

Bit	Description	Read	Write	Value after Reset
0	**Memory Space 2 Burst Enable.** Writing a 1 enables bursting. Writing a 0 disables bursting. Bursting occurs only if Prefetch Count is not equal to 00.	Yes	Yes	0
1	**Memory Space 2 READY# Input Enable.** Writing a 1 enables READY# input. Writing a 0 disables READY# input.	Yes	Yes	0
2	**Memory Space 2 BTERM# Input Enable.** Writing a 1 enables BTERM# input. Writing a 0 disables BTERM# input. For more information, refer to Section 2.2.4.3.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (prefetch count enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch four Lwords if bit 5 is set. 10 = Prefetch eight Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Counter Enable.** When set to 1 and Memory prefetching is enabled, the PCI 9030 prefetches up to the number of Lwords specified in prefetch count. When set to 0, the PCI 9030 ignores the count and continues prefetching until it is terminated by the PCI Bus.	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0h
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3).	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3).	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0h
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3).	Yes	Yes	00
23:22	**Memory Space 2 Local Bus Width.** Writing a 00 indicates an 8-bit bus width. Writing a 01 indicates a 16-bit bus width. Writing a 10 indicates a 32-bit bus width. ***Note:*** *Setting of 11 is* ***reserved****.*	Yes	Yes	10
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Writing a 1 specifies that in any Endian mode, use byte lanes [31:16] for a 16-bit Local Bus and byte lanes [31:24] for an 8-bit Local Bus. Writing a 0 specifies that in any Endian mode, use byte lanes [15:0] for a 16-bit Local Bus and byte lanes [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD strobe is asserted (0-3). Value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR strobe is asserted (0-3). Value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until end of cycle (0-3).	Yes	Yes	00

Register 10-51. (LAS3BRD; 34h) Local Address Space 3 Bus Region Descriptor

Bit	Description	Read	Write	Value after Reset
0	**Memory Space 3 Burst Enable.** Writing a 1 enables bursting. Writing a 0 disables bursting. Bursting occurs only if Prefetch Count is not equal to 00.	Yes	Yes	0
1	**Memory Space 3 READY# Input Enable.** Writing a 1 enables READY# input. Writing a 0 disables READY# input.	Yes	Yes	0
2	**Memory Space 3 BTERM# Input Enable.** Writing a 1 enables BTERM# input. Writing a 0 disables BTERM# input. For more information, refer to Section 2.2.4.3.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (prefetch count enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch four Lwords if bit 5 is set. 10 = Prefetch eight Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Counter Enable.** When set to 1 and Memory prefetching is enabled, the PCI 9030 prefetches up to the number of Lwords specified in prefetch count. When set to 0, the PCI 9030 ignores the count and continues prefetching until it is terminated by the PCI Bus.	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0h
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3).	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3).	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0h
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3).	Yes	Yes	00
23:22	**Memory Space 3 Local Bus Width.** Writing a 00 indicates an 8-bit bus width. Writing a 01 indicates a 16-bit bus width. Writing a 10 indicates a 32-bit bus width. ***Note:*** *Setting of 11 is **reserved**.*	Yes	Yes	10
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Writing a 1 specifies that in any Endian mode, use byte lanes [31:16] for a 16-bit Local Bus and byte lanes [31:24] for an 8-bit Local Bus. Writing a 0 specifies that in any Endian mode, use byte lanes [15:0] for a 16-bit Local Bus and byte lanes [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD strobe is asserted (0-3). Value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR strobe is asserted (0-3). Value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until end of cycle (0-3).	Yes	Yes	00

Register 10-52. (EROMBRD; 38h) Expansion ROM Bus Region Descriptor

Bit	Description	Read	Write	Value after Reset
0	**Expansion ROM Burst Enable.** Writing a 1 enables bursting. Writing a 0 disables bursting. Bursting occurs only if Prefetch Count is not equal to 00.	Yes	Yes	0
1	**Expansion ROM Space READY# Input Enable.** Writing a 1 enables READY# input. Writing a 0 disables READY# input.	Yes	Yes	0
2	**Expansion ROM Space BTERM# Input Enable.** Writing a 1 enables BTERM# input. Writing a 0 disables BTERM# input. For more information, refer to Section 2.2.4.3.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (prefetch count enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch four Lwords if bit 5 is set. 10 = Prefetch eight Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Counter Enable.** When set to 1 and Memory prefetching is enabled, the PCI 9030 prefetches up to the number of Lwords specified in prefetch count. When set to 0, the PCI 9030 ignores the count and continues prefetching until it is terminated by the PCI Bus.	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0h
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3).	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3).	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31).	Yes	Yes	0h
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3).	Yes	Yes	00
23:22	**Expansion ROM Space Local Bus Width.** Writing a 00 indicates an 8-bit bus width. Writing a 01 indicates a 16-bit bus width. Writing a 10 indicates a 32-bit bus width. ***Note:*** *Setting of 11 is* ***reserved****.*	Yes	Yes	00
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Writing a 1 specifies that in any Endian mode, use byte lanes [31:16] for a 16-bit Local Bus and byte lanes [31:24] for an 8-bit Local Bus. Writing a 0 specifies that in any Endian mode, use byte lanes [15:0] for a 16-bit Local Bus and byte lanes [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD strobe is asserted (0-3). Value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR strobe is asserted (0-3). Value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until end of cycle (0-3).	Yes	Yes	00

10.5 CHIP SELECT REGISTERS

Register 10-53. (CS0BASE; 3Ch) Chip Select 0 Base Address

Bit	Description	Read	Write	Value after Reset
0	**Chip Select 0 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	**Local Base Address of Chip Select 0.** Write zeroes in the least significant bits to define the range for Chip Select 0. Starting from bit 1 and scanning toward bit 27, the first "1" found defines size. The remaining most significant bits, excluding the first "1" found, define base address.	Yes	Yes	0h
31:28	***Reserved.***	Yes	No	0h

Register 10-54. (CS1BASE; 40h) Chip Select 1 Base Address

Bit	Description	Read	Write	Value after Reset
0	**Chip Select 1 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	**Local Base Address of Chip Select 1.** Write zeroes in the least significant bits to define the range for Chip Select 1. Starting from bit 1 and scanning toward bit 27, the first "1" found defines size. The remaining most significant bits, excluding the first "1" found, define base address.	Yes	Yes	0h
31:28	***Reserved.***	Yes	No	0h

Register 10-55. (CS2BASE; 44h) Chip Select 2 Base Address

Bit	Description	Read	Write	Value after Reset
0	**Chip Select 2 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	**Local Base Address of Chip Select 2.** Write zeroes in the least significant bits to define the range for Chip Select 2. Starting from bit 1 and scanning toward bit 27, the first "1" found defines size. The remaining most significant bits, excluding the first "1" found, define the base address.	Yes	Yes	0h
31:28	***Reserved.***	Yes	No	0h

Register 10-56. (CS3BASE; 48h) Chip Select 3 Base Address

Bit	Description	Read	Write	Value after Reset
0	**Chip Select 3 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	**Local Base Address of Chip Select 3.** Write zeroes in the least significant bits to define the range for Chip Select 3. Starting from bit 1 and scanning toward bit 27, the first "1" found defines size. The remaining most significant bits, excluding the first "1" found, define base address.	Yes	Yes	0h
31:28	***Reserved.***	Yes	No	0h

10.6 RUNTIME REGISTERS

Register 10-57. (INTCSR; 4Ch) Interrupt Control/Status

Bit	Description	Read	Write	Value after Reset
0	**Local Interrupt 1 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
1	**Local Interrupt 1 Polarity.** Value of 1 indicates active high. Value of 0 indicates Active low.	Yes	Yes	0
2	**Local Interrupt 1 Status.** Value of 1 indicates interrupt active. Value of 0 indicates Interrupt not active.	Yes	No	0
3	**Local Interrupt 2 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
4	**Local Interrupt 2 Polarity.** Value of 1 indicates active high. Value of 0 indicates Active low.	Yes	Yes	0
5	**Local Interrupt 2 Status.** Value of 1 indicates interrupt active. Value of 0 indicates Interrupt not active.	Yes	No	0
6	**PCI Interrupt Enable.** Value of 1 enables PCI interrupt.	Yes	Yes	0
7	**Software Interrupt.** Value of 1 generates interrupt.	Yes	Yes	0
8	**Local Interrupt 1 Select Enable.** Value of 1 indicates enabled edge triggerable interrupt. Value of 0 indicates enabled level triggerable interrupt. ***Note:*** *Operates only in High Polarity mode.*	Yes	Yes	0
9	**Local Interrupt 2 Select Enable.** Value of 2 indicates enabled edge triggerable interrupt. Value of 0 indicates enabled level triggerable interrupt. ***Note:*** *Operates only in High Polarity mode.*	Yes	Yes	0
10	**Local Edge Triggerable Interrupt Clear.** Writing 1 to this bit clears Interrupt 1.	Yes	Yes	0
11	**Local Edge Triggerable Interrupt Clear.** Writing 1 to this bit clears Interrupt 2.	Yes	Yes	0
15:12	***Reserved.***	Yes	No	0h

Register 10-58. (PROT_AREA; 4Eh) Serial EEPROM Write-Protected Address Boundary

Bit	Description	Read	Write	Value after Reset
6:0	**Serial EEPROM.** Serial EEPROM starting at Lword boundary (48 Lwords = 192 bytes) for VPD accesses. Serial EEPROM addresses below this boundary are read-only. ***Note:*** *Anything below the programmed address may contain the PCI 9030 Configuration data.*	Yes	Yes	0110000
15:7	***Reserved.***	Yes	No	0h

Register 10-59. (CNTRL; 50h) PCI Target Response, Serial EEPROM, and Initialization Control

Bit	Description	Read	Write	Value after Reset
5:0	***Reserved***.	Yes	No	0h
6	**PCI Target Write FIFO Full Condition.** Value of 1 guarantees that when the PCI Target Write FIFO is full with PCI Target Write data, there is always one location remaining empty for the PCI Target Read address to be accepted by the PCI 9030. Value of 0 Retries all PCI Target Read accesses when the PCI Target Write FIFO is full with PCI Target Write data.	Yes	Yes	0
7	**Local Arbiter LGNT Signal Select Enable.** Value of 1 selects LGNT to remain active until LREQ is de-asserted, although the PCI 9030 has a PCI Target transaction pending. Value of 0 selects LGNT to be de-asserted as soon as the PCI 9030 detects a PCI Target transaction pending and waits for LREQ to be de-asserted (Preempt condition).	Yes	Yes	0
8	**READY# Timeout Enable.** Value of 1 enables READY# timeout enable.	Yes	Yes	0
9	**READY# Timeout Select.** Values: 1 = 64 clocks 0 = 32 clocks	Yes	Yes	0
11:10	**PCI Target Write Delay.** Delay in LCLKs of ADS# from valid address. Values: 00 = 0 LCLKs 10 = 8 LCLKs 01 = 4 LCLKs 11 = 16 LCLKs	Yes	Yes	00
13:12	**PCI Configuration Base Address Register (PCIBAR) Enables.** Values: 00 = PCIBAR0 (Memory) and PCIBAR1 (I/O) enabled. 01 = PCIBAR0 (Memory) only. 10 = PCIBAR1 (I/O) only. 11 = PCIBAR0 (Memory) and PCIBAR1 (I/O) enabled.	Yes	Yes	00
14	**Delayed Read Mode.** When set to 1, the PCI 9030 operates in Delayed Transaction mode for PCI Target reads. The PCI 9030 issues a Retry to the PCI Host and prefetches Read data.	Yes	Yes	0
15	**PCI Read with Write Flush Mode.** Writing a 1 submits a request to flush a pending Read cycle if a Write cycle is detected. Writing a 0 submits a request to not effect pending reads when a Write cycle occurs (*PCI Specification* v2.2-compatible).	Yes	Yes	0
16	**PCI Read No Flush Mode.** Writing a 1 submits a request to not flush the Read FIFO if the PCI Read cycle completes (Read Ahead mode). Writing a 0 submits a request to flush the Read FIFO if a PCI Read cycle completes.	Yes	Yes	0
17	**PCI Read No Write Mode.** Writing a 1 forces a Retry on writes if a read is pending. Writing a 0 allows writes to occur while a read is pending.	Yes	Yes	0
18	**PCI Target Write Mode.** Writing a 1 indicates the PCI 9030 should disconnect when the PCI Target Write FIFO is full. Writing a 0 indicates the PCI 9030 should de-assert TRDY# when the PCI Target Write FIFO is full.	Yes	Yes	0
22:19	**PCI Target Retry Delay Clocks.** Contains the value (multiplied by 8) of the number of PCI Bus clocks after receiving a PCI-to-Local Read or Write access and not successfully completing a transfer. Only valid for read cycles if bit 14 is low. Only valid for write cycles if bit 17 is low.	Yes	Yes	Fh
23	**PCI Target LOCK# Enable.** Writing a 1 enables the PCI Target locked sequences. Writing a 0 disables PCI Target locked sequences.	Yes	Yes	0
24	**Serial EEPROM Clock for Local or PCI Bus Reads or Writes to Serial EEPROM.** Toggling this bit generates a serial EEPROM clock. (Refer to manufacturer's data sheet for the particular serial EEPROM being used.)	Yes	Yes	0
25	**Serial EEPROM Chip Select.** For Local or PCI Bus reads or writes to the serial EEPROM, setting this bit to 1 provides serial EEPROM chip select.	Yes	Yes	0
26	**Write Bit to Serial EEPROM.** For writes, this output bit is the input to serial EEPROM. Clocked into the serial EEPROM by serial EEPROM clock.	Yes	Yes	0

Register 10-59. (CNTRL; 50h) PCI Target Response, Serial EEPROM, and Initialization Control (Continued)

Bit	Description	Read	Write	Value after Reset
27	**Read Serial EEPROM Data Bit.** For reads, this input bit is the output of serial EEPROM. Clocked out of the serial EEPROM by serial EEPROM clock.	Yes	No	—
28	**Serial EEPROM Valid.** Value of 1 indicates a blank or programmed serial EEPROM is present.	Yes	No	0
29	**Reload Configuration Registers.** When set to 0, writing a value of 1 causes the PCI 9030 to reload Local Configuration registers from serial EEPROM.	Yes	Yes	0
30	**PCI Adapter Software Reset.** Value of 1 resets the PCI 9030 and issues a reset to the Local Bus. PCI and Local Configuration register contents do not reset.	Yes	Yes	0
31	**Disconnect with Flush Read FIFO.** Value of 1 causes a disconnect with flushing of the Read FIFO in Delayed Read mode (bit 14). Value of 0 causes a disconnect without flushing the Read FIFO (as a Retry).	Yes	Yes	0

Register 10-60. (GPIOC; 54h) General Purpose I/O Control

Bit	Description	Read	Write	Value after Reset
0	**GPIO0 or WAITo# Pin Select.** Selects the function of GPIO0/WAITo# pin. Value of 1 indicates pin is WAITo#. Value of 0 indicates pin is GPIO0.	Yes	Yes	0
1	**GPIO0 Direction.** Value of 0 indicates Input. Value of 1 indicates output. Always an output if WAITo# function is selected.	Yes	Yes	0
2	**GPIO0 Data.** If programmed as output, writing a value of 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
3	**GPIO1 or LLOCKo# Pin Select.** Selects the function of GPIO1/LLOCKo# pin. Value of 1 indicates pin is LLOCKo#. Value of 0 indicates pin is GPIO1.	Yes	Yes	0
4	**GPIO1 Direction.** Value of 0 indicates Input. Value of 1 indicates output. Always an output if LLOCK function is selected.	Yes	Yes	0
5	**GPIO1 Data.** If programmed as output, writing a value of 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
6	**GPIO2 or CS2# Pin Select.** Selects the function of GPIO2/CS2# pin. Value of 1 indicates pin is CS2#. Value of 0 indicates pin is GPIO2.	Yes	Yes	0
7	**GPIO2 Direction.** Value of 0 indicates Input. Value of 1 indicates output. Always an output if CS2 function is selected.	Yes	Yes	0
8	**GPIO2 Data.** If programmed as output, writing a value of 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
9	**GPIO3 or CS3# Pin Select.** Selects the function of GPIO3/CS3# pin. Value of 1 indicates pin is CS3#. Value of 0 indicates pin is GPIO3.	Yes	Yes	0
10	**GPIO3 Direction.** Value of 0 indicates Input. Value of 1 indicates output. Always an output if CS3 function is selected.	Yes	Yes	0
11	**GPIO3 Data.** If programmed as output, writing a value of 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
12	**GPIO4 or LA27 Pin Select.** Selects the function of GPIO4/LA27 pin. Value of 1 indicates LA27. Value of 0 indicates GPIO4.	Yes	Yes	1
13	**GPIO4 Direction.** Value of 0 indicates input. Value of 1 indicates output. Always an output if LA27 is selected.	Yes	Yes	0

Register 10-60. (GPIOC; 54h) General Purpose I/O Control (Continued)

Bit	Description	Read	Write	Value after Reset
14	**GPIO4 Data.** If programmed as output, writing a value of 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
15	**GPIO5 or LA26 Pin Select.** Selects the function of GPIO5/LA26 pin. Value of 1 indicates LA26. Value of 0 indicates GPIO5.	Yes	Yes	1
16	**GPIO5 Direction.** Value of 0 indicates input. Value of 1 indicates output. Always an output if LA26 is selected.	Yes	Yes	0
17	**GPIO5 Data.** If programmed as output, writing a value of 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
18	**GPIO6 or LA25 Pin Select.** Selects the function of GPIO6/LA25 pin. Value of 1 indicates LA25. Value of 0 indicates GPIO6.	Yes	Yes	1
19	**GPIO6 Direction.** Value of 0 indicates input. Value of 1 indicates output. Always an output if LA25 is selected.	Yes	Yes	0
20	**GPIO6 Data.** If programmed as output, writing a value of 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
21	**GPIO7 or LA24 Pin Select.** Selects the function of GPIO7/LA24 pin. Value of 1 indicates LA24. Value of 0 indicates GPIO7.	Yes	Yes	1
22	**GPIO7 Direction.** Value of 0 indicates input. Value of 1 indicates output. Always an output if LA24 is selected.	Yes	Yes	0
23	**GPIO7 Data.** If programmed as output, writing a value of 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
24	***Reserved.***	Yes	Yes	0
25	**GPIO8 Direction.** Value of 0 indicates input. Value of 1 indicates output.	Yes	Yes	0
26	**GPIO8 Data.** If programmed as output, writing a value of 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
31:27	***Reserved.***	Yes	Yes	0h

Note: *GPIO pins configured as outputs are driven only when the PCI 9030 owns the Local Bus. When another local master owns the bus (LGNT asserted), GPIO pins configured as outputs are floated. Refer to the PCI 9030 Design Notes for additional information.*

Register 10-62. (PMDATASCALE; 74h) Hidden 2 Power Management Data Scale

Bit	Description	Read	Write	Value after Reset
1:0	**Data_Scale 0.** Provides the D_0 Power Consumed scaling factor read in PMDATA[7:0]. Value read in PMCSR[14:13] when Data_Select = 0.	Refer to Note	Serial EEPROM	00
3:2	**Data_Scale 3.** Provides the D_3 Power Consumed scaling factor read in PMDATA[7:0]. Value read in PMCSR[14:13] when Data_Select = 3.	Refer to Note	Serial EEPROM	00
5:4	**Data_Scale 4.** Provides the D_0 Power Dissipated scaling factor read in PMDATA[7:0]. Value read in PMCSR[14:13] when Data_Select = 4.	Refer to Note	Serial EEPROM	00
7:6	**Data_Scale 7.** Provides the D_3 Power Dissipated scaling factor read in PMDATA[7:0]. Value read in PMCSR[14:13] when Data_Select = 7.	Refer to Note	Serial EEPROM	00
31:8	***Reserved.***	Refer to Note	Serial EEPROM	0h

Note: *This register can be read only two bits at a time, through PMCSR[14:13]. The two bits of PMDATASCALE returned in PMCSR[14:13] are selected by PMCSR[12:9].*

11 PIN DESCRIPTION

11.1 PIN SUMMARY

Tables in this section describe each PCI 9030 pin. Table 11-2 through Table 11-7 provide pin information common to all Local Bus modes of operation:

- Power and Ground
- Serial EEPROM Interface
- Test and Debug
- PCI System Bus Interface
- PCI Mode Independent Interface
- Local Bus Mode Independent Interface

Pins in Table 11-8 and Table 11-9 correspond to the PCI 9030 Local Bus modes—Multiplexed and Non-Multiplexed:

- Multiplexed Bus Mode Interface Pin Description (32-bit address/32-bit data)
- Non-Multiplexed Bus Mode Interface Pin Description (32-bit address/32-bit data)

For a visual of the chip pinout, refer to Section 13, “Physical Specifications.”

No internal pull-up or pull-down resistors are present in the PCI 9030. For the EEDO pin only, an external pull-up resistor is required. The pull-up resistor must be pulled to Early Power Vcc in CompactPCI Hot Swap platforms and normal Vcc in regular PCI platforms. A missing pull-up resistor for the EEDO signal may intermittently bring the PCI 9030 to a quiescent state. Recommended resistor values are 1k to 4.7k.

TRST# should be pulled low during PCI RST# assertion. If JTAG is not used, it is recommended that TRST# always be pulled low, using a 5.6k ohm resistor to ground, to put JTAG functionality into the reset state and enable normal chip logic operation.

The following table lists abbreviations used in this section to represent various pin types.

Table 11-1. Pin Type Abbreviations

Abbreviation	Pin Type
DTS	Driven tri-state pin, driven high for one-half CLK before float
I	Input pin only
I/O	Input and output pin
O	Output pin only
OC	Open collector pin
STS	Sustained tri-state pin, driven high for one CLK before float
TP	Totem pole pin
TS	Tri-state pin

As a Local Bus Master, the PCI 9030 drives all its outputs to the inactive state after the transaction is complete. If an External Master is present, the PCI 9030 tri-states all outputs when LGNT is asserted by the PCI 9030.

Note: *A “#” in the pin name indicates active low.*

Note for PCI pins: *DO NOT pull up or down on any pins unless the PCI 9030 is being used in an embedded design. Refer to PCI Local Bus Specification, v2.2.*

11.2 PINOUT COMMON TO ALL BUS MODES

Table 11-2. Power and Ground Pins (176-Pin PQFP)

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	Function
VDD	Power (+3.3V)	11	I	1, 14, 32, 45, 56, 70, 85, 100, 117, 133, 162	3.3 V power supply pins for core and I/O buffers. Liberal .01 to .1 µF decoupling capacitors should be placed near the PCI 9030.
$V_{I/O}$	Voltage Input/Output	1	I	53	System voltage select, 3.3 or 5V, from the PCI Bus.
VSS	Ground	14	I	13, 31, 44, 57, 66, 78, 88, 101, 113, 122, 132, 146, 163, 176	Ground pins.
Total		26			

Note: *The die contains 224 pads. Power and Grounds are double bounded in the PQFP packages to meet proper drive strength of the buffers.*

Table 11-3. Power and Ground Pins (180-Pin µBGA)

Symbol	Signal Name	Total Die Pads	Total Pins	Pin Type	µBGA Pin Number	Function
NC	Spare	—	4	—	A1, A14, P1, P14	Applicable only to 180-Pin µBGA. ***Unused***.
VDD	Power (+3.3V)	34	11	I	B2, B6, B13, E1, F11, J5, K13, M8, N2, N5, P12	3.3 V power supply pins for core and I/O buffers. Liberal .01 to .1 µF decoupling capacitors should be placed near the PCI 9030.
$V_{I/O}$	Voltage Input/Output	1	1	I	L5	System voltage select, 3.3 or 5V, from the PCI Bus.
VSS	Ground	39	14	I	A2, A10, B14, C6, E13, F5, G13, J3, J10, K6, L7, N1, N10, P13	Ground pins.
Total		74	30			

Table 11-4. Serial EEPROM Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	µBGA Pin Number	Function
EECS	Serial EEPROM Chip Select	1	O TP 6 mA	158	C7	Serial EEPROM chip select.
EEDI	Serial EEPROM Data In	1	O TP 6 mA	161	D6	Write data to serial EEPROM.
EEDO	Serial EEPROM Data Out	1	I	159	E7	Read data from serial EEPROM.
EESK	Serial Data Clock	1	O TP 6 mA	160	A7	Serial EEPROM clock pin.
Total		4				

Note: *The serial EEPROM interface operates at core voltage (+3.3V). The PCI 9030 requires serial EEPROM use that can operate up to 250 kHz.*

Table 11-5. Test and Debug Pins

Symbol	Signal Name	Total Pins	Pin Type	CompactPCI Hot Swap BIAS Precharge Voltage	PQFP Pin Number	µBGA Pin Number	Function
TCK	Test Clock Input	1	I	1V	165	A6	Clock source for the PCI 9030 test access port (TAP). The maximum clock rate into the TCK pin is LCLK rate or less than one-half of the LCLK rate.
TDI	Test Data In	1	I	1V	168	A5	Used to input serial data into the TAP. When the TAP enables this pin, it is sampled on the rising edge of TCK and the data is input to the selected TAP Shift register. ***Note:*** *No internal pull-up.*
TDO	Test Data Output	1	O TS PCI	1V	167	C5	Used to transmit data from the PCI 9030 TAP. Data from the selected TAP Shift registers is shifted out on TDO.
BD_SEL#/ TEST	Board Select/ Test Pin	1	I	No Connect	112	G11	**CompactPCI Hot Swap Systems:** Should be pulled high externally. The pull-up resistor needs to be connected to early power. **Non-Hot Swap and other Systems:** Should be pulled low externally. **In combination with EEDO:** Used as a IDDQ test enable pin. When pulled high, all outputs except LEDon# are placed in tri-state, and PCI Hot Swap precharge resistors are active. When pulled low, all outputs remain in normal operation and PCI Hot Swap precharge resistors are not active.
TMS	Test Mode Select	1	I	1V	166	B5	Sampled by TAP on the rising edge of TCK. The TAP state machine uses the TMS pin to determine the mode in which the TAP operates. ***Note:*** *Not used to select JTAG operation.*
TRST#	Test Reset	1	I	1V	164	E6	Reset used by JTAG testers. TRST# should be pulled low during PCI RST# assertion. If JTAG is not used, it is recommended that TRST# always be pulled low, using a 5.6k ohm resistor to ground, to put JTAG functionality into the reset state and enable normal chip logic operation.
Total		6					

Table 11-6. PCI System Bus Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	CompactPCI Hot Swap BIAS Precharge Voltage	PQFP Pin Number	µBGA Pin Number	Function
AD[31:0]	Address and Data	32	I/O TS PCI	1V	173-175, 2-6, 9-12, 15-18, 30, 33-39, 41-43, 46-50	A3, D4, B3, C3, C2, B1, C1, D3, E4, D1, E3, E2, F3, F2, F4, F1, J2, J1, K2, K3, K1, K4, L2, L3, M1, L4, M2, M3, N3, P2, P3, M4	All multiplexed on the same PCI pins. The Bus transaction consists of an Address phase, followed by one or more Data phases. The PCI 9030 supports both Read and Write bursts.
C/BE[3:0]#	Bus Command and Byte Enables	4	I	1V	7, 19, 29, 40	D2, G5, J4, L1	All multiplexed on the same PCI pins. During the Transaction Address phase, defines the bus command. During the Data phase, used as byte enables. Refer to the *PCI Local Bus Specification* v2.2 for further details.
DEVSEL#	Device Select	1	O STS PCI	1V	23	G1	When actively driven, indicates the driving device decoded its address as Target of current access.
ENUM#	Enumeration	1	O OC PCI	$V_{I/O}$	51	N4	Interrupt output set when an adapter using the PCI 9030 was recently inserted or ready to be removed from a PCI slot.
FRAME#	Cycle Frame	1	I	1V	20	G2	Driven by the current Master to indicate the beginning and duration of an access. FRAME# is asserted to indicate the bus transaction is beginning. While FRAME# is asserted, Data transfers continue. When FRAME# is de-asserted, the transaction is in the final Data phase.
IDSEL	Initialization Device Select	1	I	1V	8	E5	Used as a chip select during Configuration Read and Write transactions.
INTA#	Interrupt A	1	O OC PCI	$V_{I/O}$	170	B4	PCI Interrupt request.
IRDY#	Initiator Ready	1	I	1V	21	G3	Indicates initiating agent (Bus Master) ability to complete the current transaction Data phase.
LOCK#	Lock	1	I	1V	25	H2	Indicates an atomic operation that may require multiple transactions to complete.

Table 11-6. PCI System Bus Interface Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	CompactPCI Hot Swap BIAS Precharge Voltage	PQFP Pin Number	µBGA Pin Number	Function
PAR	Parity	1	I/O TS PCI	1V	28	H1	Even parity across AD[31:0] and C/BE[3:0]#. All PCI agents require parity generation. PAR is stable and valid one clock after the Address phase. For Data phases, PAR is stable and valid one clock after either IRDY# is asserted on a Write transaction or TRDY# is asserted on a Read transaction. Once PAR is valid, it remains valid until one clock after current Data phase completes.
PCLK	Clock	1	I	No Connection	172	A4	Provides timing for all transactions on the PCI Bus and is an input to every PCI device. The PCI 9030 operates up to 33 MHz.
PERR#	Parity Error	1	O STS PCI	1V	26	H3	Reports data parity errors during all PCI transactions, except during a special cycle.
PME#	Power Management Event	1	O OC PCI	$V_{I/O}$	169	D5	Wake-up event interrupt.
RST#	Reset	1	I	$V_{I/O}$	171	C4	Used to bring PCI-specific registers, sequencers, and signals to a default state.
SERR#	System Error	1	O OC PCI	1V	27	H5	Reports address parity errors, data parity errors on the Special Cycle command, or any other system error where the result is catastrophic.
STOP#	Stop	1	O STS PCI	1V	24	H4	Indicates the current Target is requesting that the Master stop the current transaction.
TRDY#	Target Ready	1	O STS PCI	1V	22	G4	Indicates the Target agent (selected device) ability to complete the current Data phase transaction.
Total		51					

Table 11-7. Local Bus Mode Independent Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	µBGA Pin Number	Function
BCLKo	BCLK Out	1	O TP 12 mA	71	K8	Provides a buffered version PCI clock for optional use by the Local Bus. Not in phase with the PCI clock.
CPCISW	CompactPCI Switch	1	I	54	P4	CompactPCI board latch status input.
CS[1:0]#	Chip Selects	2	O TS 12 mA	148, 147	B9, C9	General purpose chip selects. The base and range of each is programmable by Configuration registers.
GPIO0/ WAITo#	General Purpose I/O 0 or WAIT Out	1	I/O TS 12 mA	154	D8	Can be programmed to a configurable general purpose I/O pin, GPIO0, or Local Bus WAIT out pin. WAITo# is asserted when wait states are caused by the internal wait state generator. Serves as an output to provide ready-out status.
GPIO1/ LLOCKo#	General Purpose I/O 1 or LLOCK Out	1	I/O TS 12 mA	155	A8	Can be programmed to a configurable general purpose I/O pin, GPIO1, or Local Bus LLOCK out pin, LLOCKo#. LLOCKo# indicates an atomic operation that may require multiple transactions to complete and can be used by the Local Bus to lock resources.
GPIO2/ CS2#	General Purpose I/O 2 or Chip Select 2 Out	1	I/O TS 12 mA	156	D7	Can be programmed to a configurable general purpose I/O pin, GPIO2, or as Chip Select 2 output pin, CS2#.
GPIO3/ CS3#	General Purpose I/O 3 or Chip Select 3 Out	1	I/O TS 12 mA	157	B7	Can be programmed to a configurable general purpose I/O pin, GPIO3, or as Chip Select 3 output pin, CS3#.
GPIO8	General Purpose I/O 8	1	I/O TS 12 mA	94	L12	Configurable general purpose I/O pin.
LCLK	Local Bus Clock	1	I	145	E9	Local clock, up to 60 MHz, and may be asynchronous to PCI clock.
LEDon#	LED On	1	O OC 24 mA	52	K5	Hot Swap board indicator LED.
LGNT	Local Bus Grant	1	O TP 12 mA	150	A9	Asserted by PCI 9030 to grant control of the Local Bus to a Local Bus Master. When the PCI 9030 requires the Local Bus, it can optionally signal a preempt by de-asserting LGNT.
LINTi1	Local Interrupt Input 1	1	I	152	B8	When asserted, causes a PCI interrupt. Polarity is determined by INTCSR configuration register.
LINTi2	Local Interrupt Input 2	1	I	153	C8	When asserted, causes a PCI interrupt. Polarity is determined by INTCSR configuration register.

Table 11-7. Local Bus Mode Independent Interface Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	µBGA Pin Number	Function
LPMESET	Local Power Management Event Set	1	I	103	J12	As an input, the Local Initiator can issue LPMESET to the PCI 9030 in the case of a Power Management Wake-Up event. LPMESET must be asserted to the PCI 9030 no less than one Local Clock pulse. The PCI 9030 latches the LPMESET assertion, sets the PME# status bit (PMCSR[15]), and asserts PME# to the PCI Bus, if enabled.
LPMINT#	Local Power Management Interrupt	1	O TP 12 mA	126	D13	Could be used for Local Power Management Events. The PCI 9030 drives the interrupt to the external Master to request a Power State Change.
LREQ	Local Bus Request	1	I	151	E8	Asserted by a Local Bus Master to request Local Bus use.
LRESETo#	Local Bus Reset Out	1	O TP 12 mA	149	D9	Asserted when the PCI 9030 chip is reset. Can be used to drive Local processor RESET# input.
MODE	Bus Mode	1	I	76	K9	Selects the PCI 9030 Bus Operation mode: Mode — Bus Mode 1 — Multiplexed 0 — Non-Multiplexed
Total		19				

11.3 MULTIPLEXED LOCAL BUS MODE PINOUT

Table 11-8. Multiplexed Bus Mode Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	µBGA Pin Number	Function
ADS#	Address Strobe	1	O TS 12 mA	138	C11	Indicates a valid address and start of a new Bus access. Asserted for the first clock of a Bus access.
ALE	Address Latch Enable	1	O TS 12 mA	75	M9	Asserted during the Address phase and de-asserted before the Data phase.
BLAST#	Burst Last	1	O TS 12 mA	139	B11	Driven by the current Local Bus Master to indicate the last transfer in a Bus access.
BTERM#	Burst Terminate	1	I	144	B10	If the Bterm Mode bit is disabled through the PCI 9030 Configuration registers, the PCI 9030 also bursts up to four Lwords. If enabled, the PCI 9030 continues to burst until BTERM# input is asserted or the burst is complete. BTERM# is a Ready input that breaks up a Burst cycle and causes another Address cycle to occur. Used in conjunction with the PCI 9030 programmable wait state generator.
GPIO4/ LA27	General Purpose I/O 4 or Address Bus	1	I/O TS 12 mA	137	A12	Can be programmed to a configurable general purpose I/O pin, GPIO4, or as Address Bus output pin, LA27.
GPIO5/ LA26	General Purpose I/O 5 or Address Bus	1	I/O TS 12 mA	136	A13	Can be programmed to a configurable general purpose I/O pin, GPIO5, or as Address Bus output pin, LA26.
GPIO6/ LA25	General Purpose I/O 6 or Address Bus	1	I/O TS 12 mA	135	B12	Can be programmed to a configurable general purpose I/O pin, GPIO6, or as Address Bus output pin, LA25.
GPIO7/ LA24	General Purpose I/O 7 or Address Bus	1	I/O TS 12 mA	134	C12	Can be programmed to a configurable general purpose I/O pin, GPIO7, or as Address Bus output pin, LA24.
LA[23:2]	Address Bus	22	O TS 12 mA	131-127, 125-123, 121-118, 116-114, 111-105	C13, D11, C14, D14, D12, E11, E14, E12, F14, F10, F12, F13, G14, G10, G12, H14, H11, H12, H13, H10, J14, J11	Carries the upper 22 bits of the 28-bit physical Address Bus. During bursts, LA[23:2] increment to indicate successive Data cycles.
LAD[31:0]	Address/ Data Bus	32	I/O TS 12 mA	61-65, 67-69, 72-74, 77, 79-84, 86-87, 89-93, 95-99, 102, 104	L6, P6, K7, N7, M7, P7, L8, N8, P8, L9, N9, P9, M10, P10, L10, N11, M11, P11, L11, N12, N13, M12, M13, N14, M14, L13, K10, K11, L14, K12, K14, J13	During an Address phase, the bus carries the upper 26 bits of 28-bit physical Address Bus [27:2]. During a Data phase, the bus carries 32 bits of data. 8 bit = LAD[7:0] 16 bit = LAD[15:0] 32 bit = LAD[31:0] During an ADS# assertion, carries the Local Address Bus (LA[27:2]).

Table 11-8. Multiplexed Bus Mode Interface Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	µBGA Pin Number	Function
LBE[3:0]#	Byte Enables	4	O TS 12 mA	55, 58-60	M5, P5, M6, N6	Encoded, based on the bus-width configuration: **32-Bit Bus** Four byte enables indicate which of the four bytes are active during a data cycle: LBE3# Byte Enable 3 = LAD[31:24] LBE2# Byte Enable 2 = LAD[23:16] LBE1# Byte Enable 1 = LAD[15:8] LBE0# Byte Enable 0 = LAD[7:0] **16-Bit Bus** LBE3# Byte High Enable (BHE#) = LAD[15:8] LBE2# ***Unused*** LBE1# Address bit 1 (LA1) LBE0# Byte Low Enable (BLE#) = LAD[7:0] **8-Bit Bus** LBE3# ***Unused*** LBE2# ***Unused*** LBE1# Address bit 1 (LA1) LBE0# Address bit 0 (LA0)
LW/R#	Write/Read	1	O TS 12 mA	142	A11	Asserted low for reads and high for writes.
RD#	Read Strobe	1	O TS 12 mA	141	D10	General purpose read strobe. The timing is controlled by current Bus Region Descriptor register.
READY#	Local Ready Input	1	I	143	C10	Local ready input indicates Read data on the bus is valid or a Write Data transfer is complete. Used in conjunction with the PCI 9030 programmable wait state generator.
WR#	Write Strobe	1	O TS 12 mA	140	E10	General purpose write strobe. Timing is controlled by the current Bus Region Descriptor register.
Total		70				

11.4 NON-MULTIPLEXED LOCAL BUS MODE PINOUT

Table 11-9. Non-Multiplexed Bus Mode Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	µBGA Pin Number	Function
ADS#	Address Strobe	1	O TS 12 mA	138	C11	Indicates a valid address and start of a new Bus access. Asserted for the first clock of a Bus access.
ALE	Address Latch Enable	1	O TS 12 mA	75	M9	Asserted during the Address phase and de-asserted before the Data phase.
BLAST#	Burst Last	1	O TS 12 mA	139	B11	Driven by the current Local Bus Master to indicate the last transfer in a Bus access.
BTERM#	Burst Terminate	1	I	144	B10	If the Bterm Mode bit is disabled through the PCI 9030 Configuration registers, the PCI 9030 also bursts up to four Lwords. If enabled, the PCI 9030 continues to burst until BTERM# input is asserted or the burst is complete. BTERM# is a Ready input that breaks up a Burst cycle and causes another Address cycle to occur. Used in conjunction with the PCI 9030 programmable wait state generator.
GPIO4/ LA27	General Purpose I/O 4 or Address Bus	1	I/O TS 12 mA	137	A12	Can be programmed to a configurable general purpose I/O pin, GPIO4, or as Address Bus output pin, LA27.
GPIO5/ LA26	General Purpose I/O 5 or Address Bus	1	I/O TS 12 mA	136	A13	Can be programmed to a configurable general purpose I/O pin, GPIO5, or as Address Bus output pin, LA26.
GPIO6/ LA25	General Purpose I/O 6 or Address Bus	1	I/O TS 12 mA	135	B12	Can be programmed to a configurable general purpose I/O pin, GPIO6, or as Address Bus output pin, LA25.
GPIO7/ LA24	General Purpose I/O 7 or Address Bus	1	I/O TS 12 mA	134	C12	Can be programmed to a configurable general purpose I/O pin, GPIO7, or as Address Bus output pin, LA24.
LA[23:2]	Address Bus	22	O TS 12 mA	131-127, 125-123, 121-118, 116-114, 111-105	C13, D11, C14, D14, D12, E11, E14, E12, F14, F10, F12, F13, G14, G10, G12, H14, H11, H12, H13, H10, J14, J11	Carries the upper 22 bits of the 28-bit physical Address Bus. During bursts, LA[23:2] increment to indicate successive Data cycles.

Table 11-9. Non-Multiplexed Bus Mode Interface Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	µBGA Pin Number	Function
LBE[3:0]#	Byte Enables	4	O TS 12 mA	55, 58-60	M5, P5, M6, N6	Encoded, based on the bus-width configuration: **32-Bit Bus** Four byte enables indicate which of the four bytes are active during a data cycle: LBE3# Byte Enable 3 = LD[31:24] LBE2# Byte Enable 2 = LD[23:16] LBE1# Byte Enable 1 = LD[15:8] LBE0# Byte Enable 0 = LD[7:0] **16-Bit Bus** LBE3# Byte High Enable (BHE#) = LD[15:8] LBE2# ***Unused*** LBE1# Address bit 1 (LA1) LBE0# Byte Low Enable (BLE#) = LD[7:0] **8-Bit Bus** LBE3# ***Unused*** LBE2# ***Unused*** LBE1# Address bit 1 (LA1) LBE0# Address bit 0 (LA0)
LD[31:0]	Data Bus	32	I/O TS 12 mA	61-65, 67-69, 72-74, 77, 79-84, 86-87, 89-93, 95-99, 102, 104	L6, P6, K7, N7, M7, P7, L8, N8, P8, L9, N9, P9, M10, P10, L10, N11, M11, P11, L11, N12, N13, M12, M13, N14, M14, L13, K10, K11, L14, K12, K14, J13	Carries 8-, 16-, or 32-bit data quantities, depending upon a Target bus-width configuration: 8 bit = LD[7:0] 16 bit = LD[15:0] 32 bit = LD[31:0]
LW/R#	Write/Read	1	O TS 12 mA	142	A11	Asserted low for reads and high for writes.
RD#	Read Strobe	1	O TS 12 mA	141	D10	General purpose read strobe. The timing is controlled by current Bus Region Descriptor register.
READY#	Local Ready Input	1	I	143	C10	Local ready input indicates Read data on the bus is valid or a Write Data transfer is complete. Used in conjunction with the PCI 9030 programmable wait state generator.
WR#	Write Strobe	1	O TS 12 mA	140	E10	General purpose write strobe. Timing is controlled by the current Bus Region Descriptor register.
Total		70				

11.5 DEBUG INTERFACE

The PCI 9030 provides a JTAG Boundary Scan interface which can be utilized to debug a pin's connectivity to the board.

11.5.1 IEEE 1149.1 Test Access Port (JTAG Debug Port)

The IEEE 1149.1 Test Access Port (TAP), commonly called the JTAG (Joint Test Action Group) debug port, is an architectural standard described in IEEE Standard 1149.1–1990, *IEEE Standard Test Access Port and Boundary Scan Architecture*. The standard describes a method for accessing internal chip facilities using a four- or five-signal interface.

The JTAG debug port, originally designed to support scan-based board testing, is enhanced to support the attachment of debug tools. The enhancements, which comply with the IEEE 1149.1 specifications for vendor-specific extensions, are compatible with standard JTAG hardware for boundary-scan system testing.

- **JTAG Signals**—JTAG debug port implements the four required JTAG signals, TCLK, TMS, TDI, TDO, and the optional TRST# signal.
- **JTAG Clock Requirements**—The TCLK signal frequency can range from DC to one-half of the internal chip clock frequency.
- **JTAG Reset Requirements**—JTAG debug port logic is reset at the same time as a system reset. Upon receiving TRST#, the JTAG TAP controller returns to the Test-Logic Reset state.

11.5.2 JTAG Instructions

The JTAG debug port provides the standard **extest, sample/preload,** and **bypass** instructions. Invalid instructions behave as the **bypass** instruction. There are three private instructions.

The following tables list the JTAG instructions and infrared (IR) outputs.

Table 11-10. JTAG Instructions

Instruction	Input Code	Comments
Extest	0000	IEEE 1149.1 standard
Sample/Preload	0100	IEEE 1149.1 standard
Bypass	1111	IEEE 1149.1 standard

Table 11-11. JTAG Infrared Outputs

Instruction	IR Output	Comments
Extest	0001	IEEE 1149.1 standard
Sample/Preload	0101	IEEE 1149.1 standard
Bypass	1101	IEEE 1149.1 standard

11.5.3 JTAG Boundary Scan

Boundary Scan Description Language (BSDL), IEEE 1149.1b-1994, is a supplement to IEEE 1149.1-1990 and IEEE 1149.1a-1993 *Standard Test Access Port and Boundary-Scan Architecture*. BSDL, a subset of the IEEE 1076-1993 Standard VHSIC Hardware Description Language (VHDL), allows a rigorous description of testability features in components which comply with the standard. It is used by automated test pattern generation tools for package interconnect tests and electronic design automation (EDA) tools for synthesized test logic and verification. BSDL supports robust extensions that can be used for internal test generation and to write software for hardware debug and diagnostics.

The primary components of BSDL include the logical port description, physical pin map, instruction set, and boundary register description.

The logical port description assigns symbolic names to the pins of a chip. Each pin has a logical type of in, out, inout, buffer, or linkage that defines the logical direction of signal flow.

The physical pin map correlates the logical ports of the chip to the physical pins of a specific package. A BSDL description can have several physical pin maps; each map is given a unique name.

Instruction set statements describe the bit patterns that must be shifted into the Instruction Register to place the chip in the various test modes defined by the standard. Instruction set statements also support descriptions of instructions that are unique to the chip.

The boundary register description lists each cell or shift stage of the Boundary Register. Each cell has a unique number; the cell numbered 0 is the closest to the Test Data Out (TDO) pin and the cell with the highest number is closest to the Test Data In (TDI) pin. Each cell contains additional information, including: cell type, logical port associated with the cell, logical function of the cell, safe value, control cell number, disable value, and result value.

12 ELECTRICAL SPECIFICATIONS

12.1 GENERAL ELECTRICAL SPECIFICATIONS

Table 12-1. Absolute Maximum Ratings

Specification	Maximum Rating
Storage Temperature	-55 to +125 °C
Ambient Temperature with Power Applied	-40 to +85 °C
Supply Voltage to Ground	-0.5 to +4.6V
Input Voltage (VIN)	VSS -0.5 to 11.0V
Output Voltage (VOUT)	VSS -0.5V to VDD +0.5
Maximum Package Power Dissipation	
176-Pin PQFP	1W
180-Pin µBGA	0.5W

Note: *Package Power Dissipation derived with assumption that 1.0m/s air flow is available.*

Table 12-2. Operating Ranges

Ambient Temperature	Supply Voltage (VDD)	Input Voltage (VIN)	
		Min	Max
-40 to +85 °C	3.0 to 3.6V	VSS	11.0V

Table 12-3. Capacitance (Sample Tested Only)

Parameter	Test Conditions	Pin Type	Value		Units
			Typical	Maximum	
CIN	VIN = 0V	Input	4	6	pF
COUT	VOUT = 0V	Output	6	10	pF

The following table lists the package thermal resistance ($\Theta_{j\text{-}a}$).

Table 12-4. Package Thermal Resistance

	Air Flow			
Package Type	0m/s	1m/s	2m/s	3m/s
176-Pin PQFP	65 (°C/W)	45	35	30
180-Pin µBGA	48 (°C/W)	34	26	22

Table 12-5. Electrical Characteristics over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
VOH[1]	Output High Voltage	VDD = Min VIN = VIH or VIL	IOH = -12.0 mA	2.4	—	V
VOL[1]	Output Low Voltage		IOL = 12 mA	—	0.4	V
VIH	Input High Level	—	—	2.0	11.0	V
VIL	Input Low Level	—	—	-0.5	0.8	V
VOH3	PCI 3.3V Output High Voltage	VDD = Min VIN = VIH or VIL	IOH = -500 µA	0.9 VDD	—	V
VOL3	PCI 3.3V Output Low Voltage	—	IOL = 1500 µA	—	0.1 VDD	V
VIH3	PCI 3.3V Input High Level	—	—	0.5 VDD	VDD +0.5	V
VIL3	PCI 3.3V Input Low Level	—	—	-0.5	0.3 VDD	V
IIL	Input Leakage Current	VSS ≤ VIN ≤ VDD, VDD = Max		-10	+10	µA
ILPC[2]	DC Current Per Pin During Pre-Charge	VP = 0.8 to 1.2V		—	1.0	mA
IOZ	Tri-State Output Leakage Current	VDD = Max		-10	+10	µA
ICC	Power Supply Current[3]	VDD=3.6V, PCLK = 33 MHz, LCLK = 60 MHz 80 outputs switching simultaneously		—	150	mA
ICCL ICCH ICCZ	Quiescent Power Supply Current	VCC = Max VIN = GND or VCC		—	50	µA

Notes:

1 Except in the case of EESK, EEDI, EECS, and LPMINT# pins.

2 ILPC is the DC current flowing from VDD to Ground during precharge, as both PMOS and NMOS devices remain on during precharge. It is not the leakage current flowing into or out of the pin under precharge.

3 Maximum value based upon I/O simultaneously switching outputs.

12.2 LOCAL INPUTS

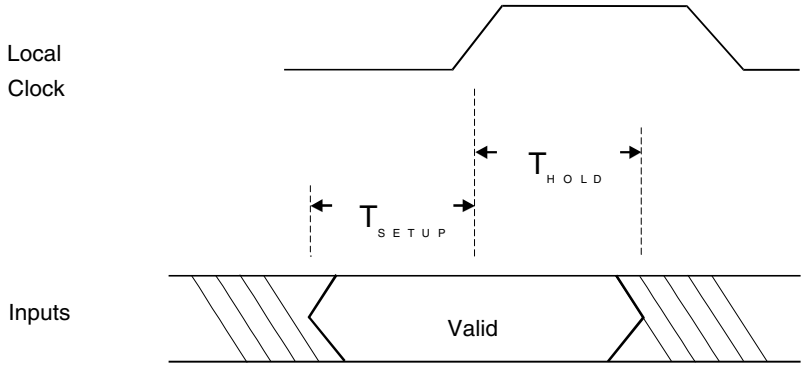


Figure 12-1. PCI 9030 Local Input Setup and Hold Waveform

Table 12-6. AC Electrical Characteristics (Local Inputs) over Operating Range

Signals (Synchronous Inputs) C_L = 50 pF, Vcc = 3.0V, Ta = 85 °C	Bus Mode	T_{SETUP} (ns) (WORST CASE)	T_{HOLD} (ns) (WORST CASE)
BTERM#	All	7.0	1
LAD[31:0] (Data)	Multiplexed	5.0	1
LD[31:0]	Non-Multiplexed	5.0	1
LPMESET	All	5.0	1
LREQ	All	5.0	1
READY#	All	7.0	1
Input Clocks	**Bus Mode**	**Min**	**Max**
Local Clock Input Frequency	All	0	60 MHz
PCI Clock Input Frequency	All	0	33 MHz

Note: *These values are provided as an example and are only representative of general performance characteristics of the PLX PCI devices.*

12.3 LOCAL OUTPUTS

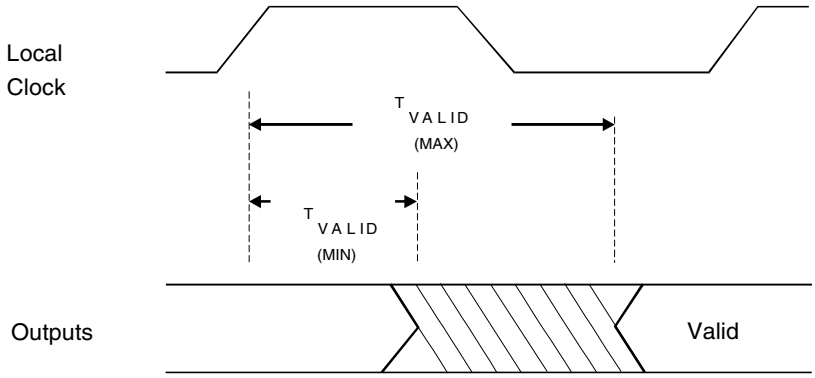


Figure 12-2. PCI 9030 Local Output Delay

Table 12-7. AC Electrical Characteristics (Local Outputs) over Operating Range

Signals (Synchronous Outputs) C_L = 50 pF, Vcc = 3.0V, Ta = 85 °C	Bus Mode	Output T_{VALID} (Max)
ADS#	All	10.0
BLAST#	All	10.0
CS0#	All	10.0
CS1#	All	10.0
CS2#	All	10.0
CS3#	All	10.0
LA[27:2]	All	10.0
LAD[31:0] (Data)	Multiplexed	10.0
LBE[3:0]#	All	10.0
LD[31:0]	Non-Multiplexed	10.0
LGNT	All	11.0
LLOCKo#	All	10.0
LPMINT#	All	10.0
LW/R#	All	10.0
RD#	All	10.0
WAITo#	All	10.0
WR#	All	10.0

Notes: *All T_{VALID} (Min) values are greater than 5 ns.*

Timing derating for loading is ±35 PS/PF.

These values are provided as an example and are only representative of general performance characteristics of PLX PCI devices.

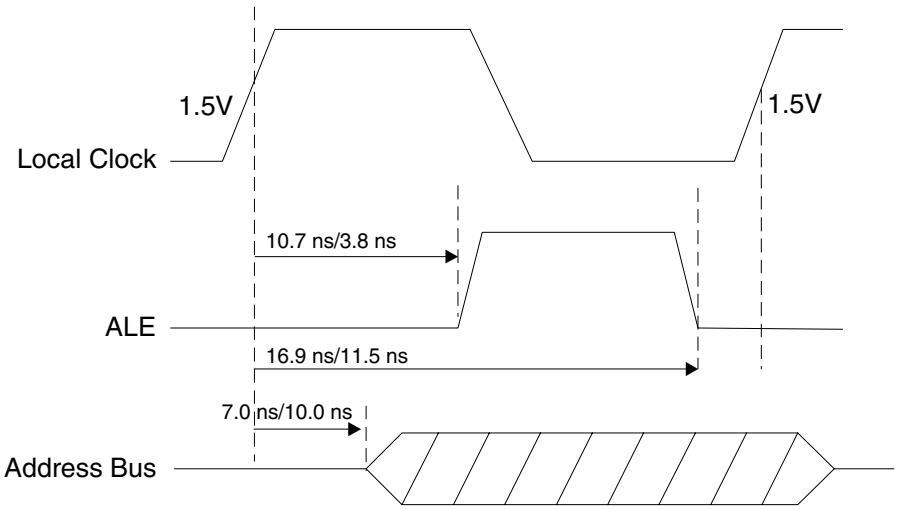


Figure 12-3. PCI 9030 ALE Output Delay (Min/Max) to the Local Clock at 60 MHz

13 PHYSICAL SPECIFICATIONS

13.1 176-PIN PQFP

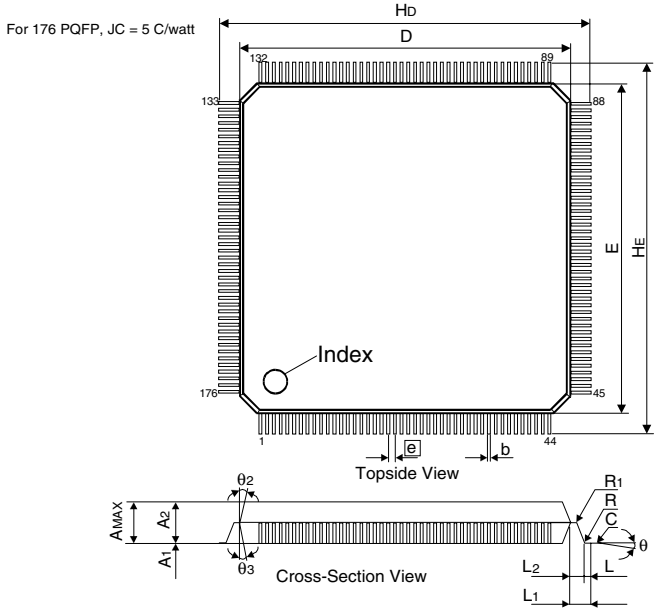
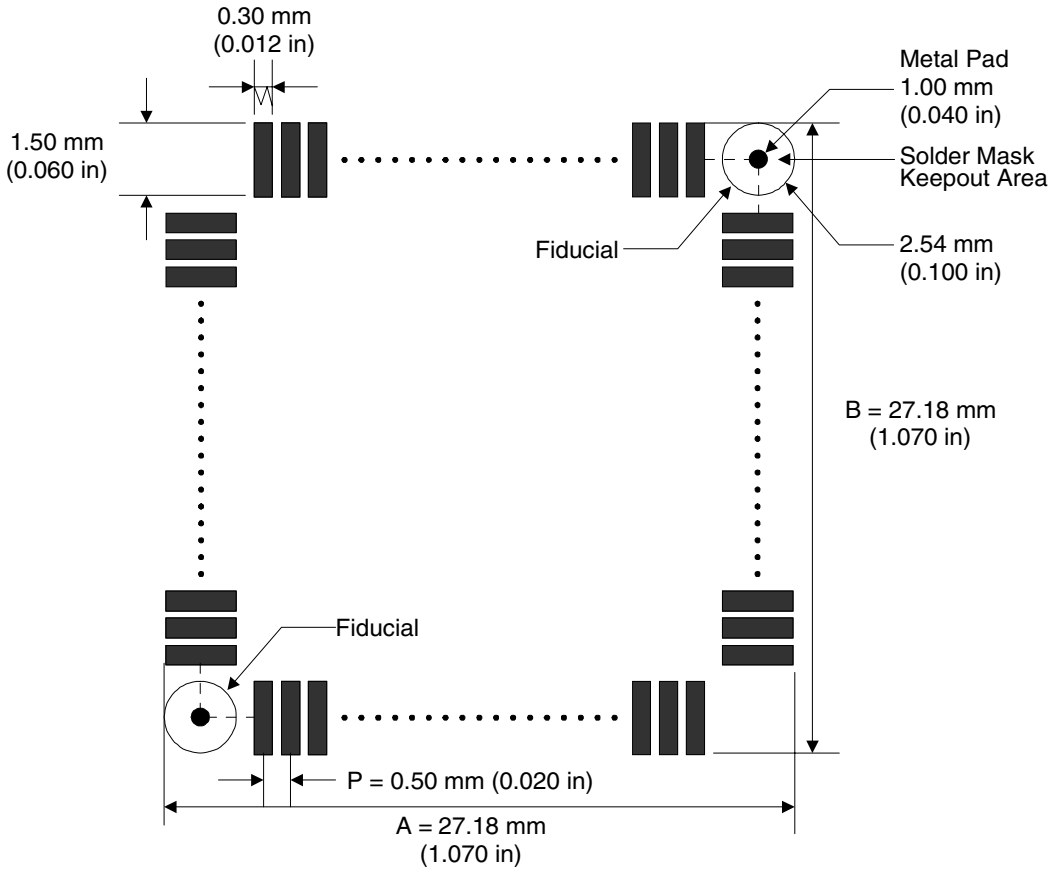


Figure 13-1. 176-Pin PQFP Package Mechanical Dimensions—Topside and Cross-Section Views

Table 13-1. 176-Pin PQFP Package Mechanical Dimensions (Legend for Figure 13-1)

Lead Type STD (QFP18-176 Pin STD)			
Symbol	**Dimensions in Millimeters**		
	Min.	**Nom.**	**Max.**
E	23.9	24	24.1
D	23.9	24	24.1
A	—	—	3
A1	—	0.1	—
A2	2.6	2.7	2.8
e	—	0.5	—
b	0.15	0.2	0.3
C	0.1	0.15	0.2
θ	0°	—	10°
L	0.3	0.5	0.7
L1	—	1	—
L2	—	0.5	—
H_E	25.6	26	26.4
H_D	25.6	26	26.4
θ2	—	15°	—
θ3	—	15°	—
R	—	0.2	—
R1	—	0.2	—



Note: *Leave 0.002 inch solder mask clearance around pads.*

Figure 13-2. 176-Pin PQFP PCB Layout Suggested Land Pattern

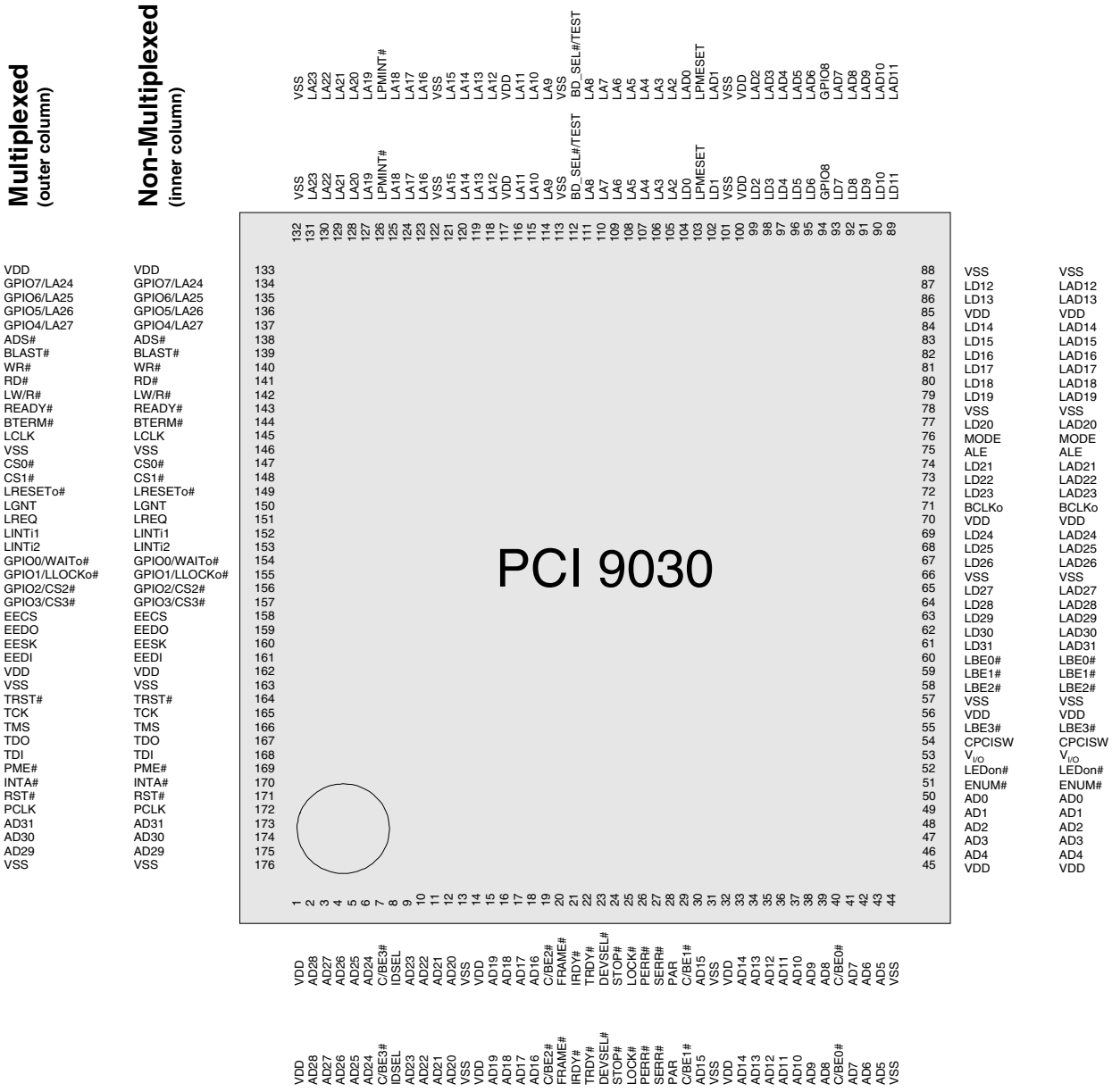


Figure 13-3. 176-Pin PQFP Signal and Pinout

13.2 180-PIN µBGA

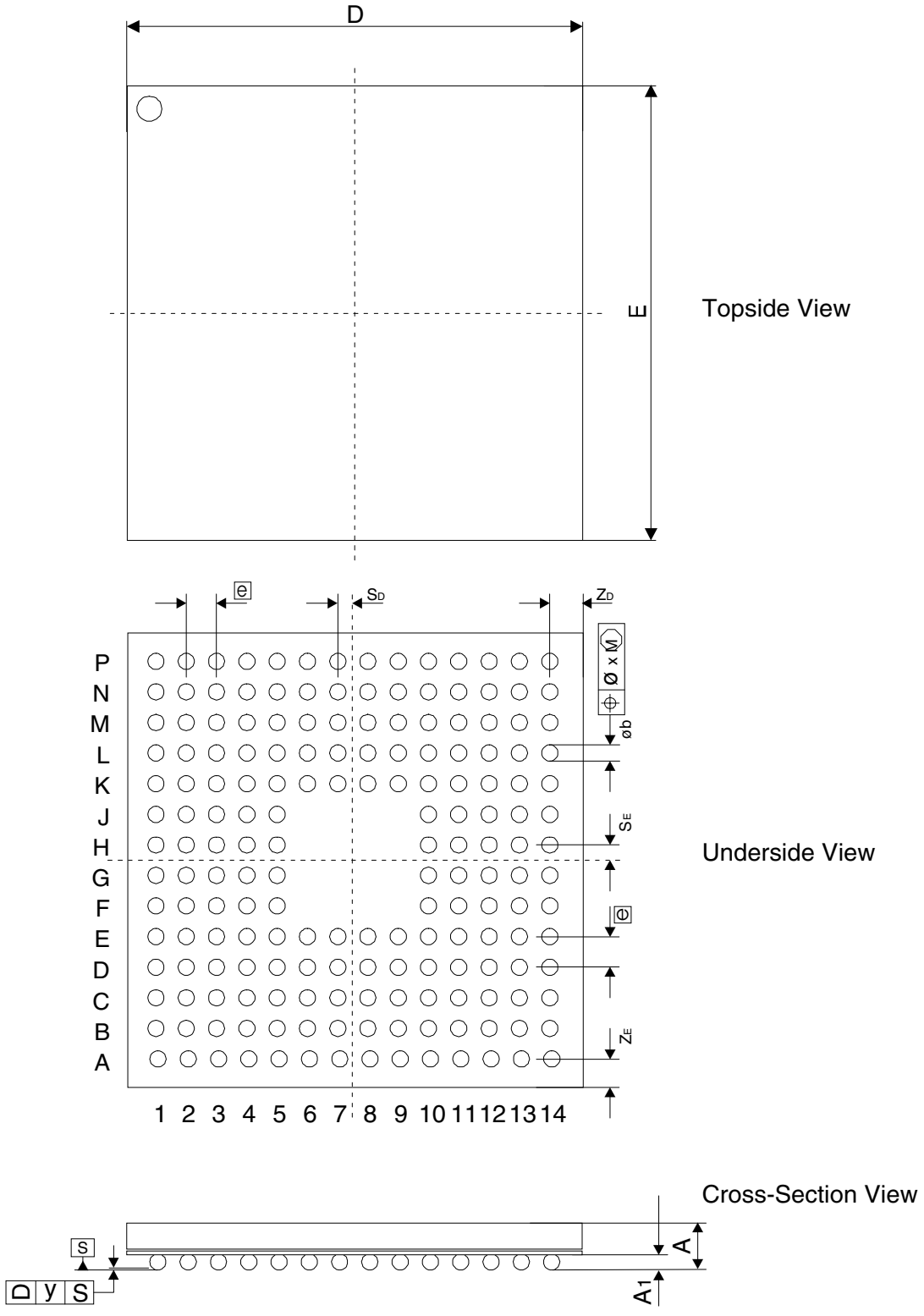


Figure 13-4. 180-Pin µBGA Package Mechanical Dimensions—Topside, Underside, and Cross-Section Views

Table 13-2. 180-Pin µBGA Package Mechanical Dimensions (Legend for Figure 13-4)

Symbol	Dimensions (in Millimeters)		
	Min.	Nom.	Max.
D	11.85	12.0	12.3
E	11.85	12.0	12.3
A	—	—	1.20
A_1	0.30	0.35	0.45
e	—	0.80	—
øb	0.40	0.45	0.55
x	—	—	0.08
y	—	—	0.10
S_D	—	0.40	—
S_E	—	0.40	—
Z_D	—	0.80	—
Z_E	—	0.80	—

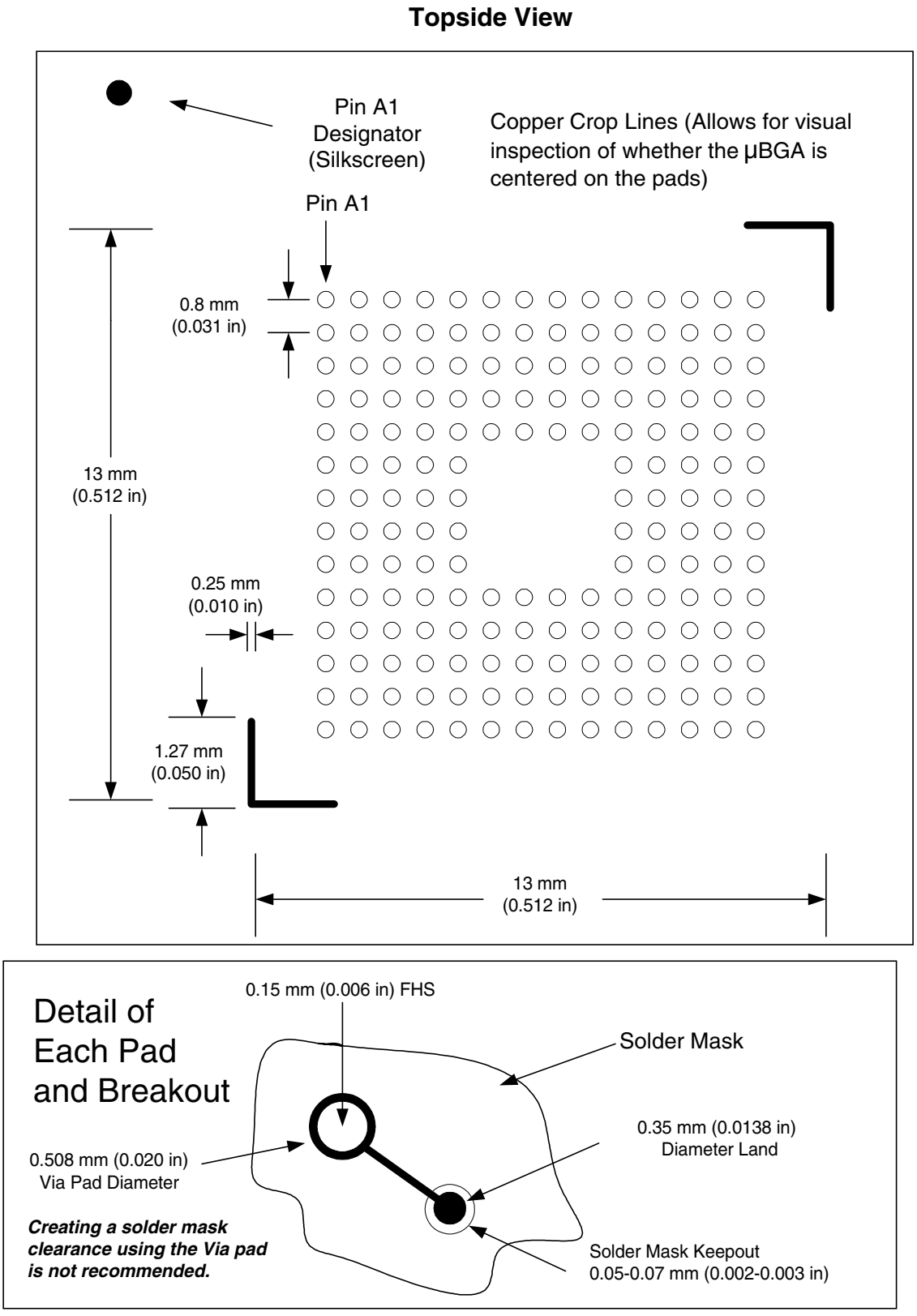


Figure 13-5. 180-Pin µBGA PCB Layout Suggested Land Pattern

G=GND

P	**P1**	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	**P14**
N	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14
M	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13	M14
L	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14
K	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14
J	J1	J2	J3	J4	J5					J10	J11	J12	J13	J14
H	H1	H2	H3	H4	H5					H10	H11	H12	H13	H14
G	G1	G2	G3	G4	G5					G10	G11	G12	G13	G14
F	F1	F2	F3	F4	F5					F10	F11	F12	F13	F14
E	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14
D	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14
C	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14
B	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14
A	**A1**	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	**A14**
	1	2	3	4	5	6	7	8	9	10	11	12	13	14

4 Spare, Not Connected Pins

Figure 13-6. 180-Pin µBGA Package Layout—Underside View

Note: *The following abbreviations apply in Table 13-3:*
NC = Not Connected
M = Multiplexed Mode
NM = Non-Multiplexed Mode

Table 13-3. 180-Pin µBGA PCI 9030 Pinout

Pin #	Symbol	Bus Mode	Pin #	Symbol	Bus Mode	Pin #	Symbol	Bus Mode	Pin #	Symbol	Bus Mode
A1	NC	All	C3	AD28	All	E5	IDSEL	All	H1	PAR	All
A2	VSS	All	C4	RST#	All	E6	TRST#	All	H2	LOCK#	All
A3	AD31	All	C5	TDO	All	E7	EEDO	All	H3	PERR#	All
A4	PCLK	All	C6	VSS	All	E8	LREQ	All	H4	STOP#	All
A5	TDI	All	C7	EECS	All	E9	LCLK	All	H5	SERR#	All
A6	TCK	All	C8	LINTi2	All	E10	WR#	All	H10	LA4	All
A7	EESK	All	C9	CS0#	All	E11	LA18	All	H11	LA7	All
A8	GPIO1/LLOCKo#	All	C10	READY#	All	E12	LA16	All	H12	LA6	All
A9	LGNT	All	C11	ADS#	All	E13	VSS	All	H13	LA5	All
A10	VSS	All	C12	GPIO7/LA24	All	E14	LA17	All	H14	LA8	All
A11	LW/R#	All	C13	LA23	All	F1	AD16	All	J1	AD14	All
A12	GPIO4/LA27	All	C14	LA21	All	F2	AD18	All	J2	AD15	All
A13	GPIO5/LA26	All	D1	AD22	All	F3	AD19	All	J3	VSS	All
A14	NC	All	D2	C/BE3#	All	F4	AD17	All	J4	C/BE1#	All
B1	AD26	All	D3	AD24	All	F5	VSS	All	J5	VDD	All
B2	VDD	All	D4	AD30	All	F10	LA14	All	J10	VSS	All
B3	AD29	All	D5	PME#	All	F11	VDD	All	J11	LA2	All
B4	INTA#	All	D6	EEDI	All	F12	LA13	All	J12	LPMESET	All
B5	TMS	All	D7	GPIO2/CS2#	All	F13	LA12	All	J13	LAD0 LD0	M NM
B6	VDD	All	D8	GPIO0/WAITo#	All	F14	LA15	All	J14	LA3	All
B7	GPIO3/CS3#	All	D9	LRESETo#	All	G1	DEVSEL#	All	K1	AD11	All
B8	LINTi1	All	D10	RD#	All	G2	FRAME#	All	K2	AD13	All
B9	CS1#	All	D11	LA22	All	G3	IRDY#	All	K3	AD12	All
B10	BTERM#	All	D12	LA19	All	G4	TRDY#	All	K4	AD10	All
B11	BLAST#	All	D13	LPMINT#	All	G5	C/BE2#	All	K5	LEDon#	All
B12	GPIO6/LA25	All	D14	LA20	All	G10	LA10	All	K6	VSS	All
B13	VDD	All	E1	VDD	All	G11	BD_SEL#/TEST	All	K7	LAD29 LD29	M NM
B14	VSS	All	E2	AD20	All	G12	LA9	All	K8	BCLKo	All
C1	AD25	All	E3	AD21	All	G13	VSS	All	K9	MODE	All
C2	AD27	All	E4	AD23	All	G14	LA11	All	K10	LAD5 LD5	M NM

Table 13-3. 180-Pin µBGA PCI 9030 Pinout (Continued)

Pin #	Symbol	Bus Mode	Pin #	Symbol	Bus Mode	Pin #	Symbol	Bus Mode	Pin #	Symbol	Bus Mode
K11	LAD4 LD4	M NM	L12	GPIO8	All	M13	LAD9 LD9	M NM	N14	LAD8 LD8	M NM
K12	LAD2 LD2	M NM	L13	LAD6 LD6	M NM	M14	LAD7 LD7	M NM	P1	NC	All
K13	VDD	All	L14	LAD3 LD3	M NM	N1	VSS	All	P2	AD2	All
K14	LAD1 LD1	M NM	M1	AD7	All	N2	VDD	All	P3	AD1	All
L1	C/BE0#	All	M2	AD5	All	N3	AD3	All	P4	CPCISW	All
L2	AD9	All	M3	AD4	All	N4	ENUM#	All	P5	LBE2#	All
L3	AD8	All	M4	AD0	All	N5	VDD	All	P6	LAD30 LD30	M NM
L4	AD6	All	M5	LBE3#	All	N6	LBE0#	All	P7	LAD26 LD26	M NM
L5	$V_{I/O}$	All	M6	LBE1#	All	N7	LAD28 LD28	M NM	P8	LAD23 LD23	M NM
L6	LAD31 LD31	M NM	M7	LAD27 LD27	M NM	N8	LAD24 LD24	M NM	P9	LAD20 LD20	M NM
L7	VSS	All	M8	VDD	All	N9	LAD21 LD21	M NM	P10	LAD18 LD18	M NM
L8	LAD25 LD25	M NM	M9	ALE	All	N10	VSS	All	P11	LAD14 LD14	M NM
L9	LAD22 LD22	M NM	M10	LAD19 LD19	M NM	N11	LAD16 LD16	M NM	P12	VDD	All
L10	LAD17 LD17	M NM	M11	LAD15 LD15	M NM	N12	LAD12 LD12	M NM	P13	VSS	All
L11	LAD13 LD13	M NM	M12	LAD10 LD10	M NM	N13	LAD11 LD11	M NM	P14	NC	All

Table 13-4. 180-Pin µBGA Six-Layer Board Routing Example (Four Routing Layers)—Sample Parameters

Routing Layer Parameters	Via size		Other Parameters	Via size	
	mm	inches		mm	inches
Component Side	0.509	0.0200	Land Pad Side	0.350	0.0138
First Inside Layer	0.634	0.0250	Solder Mask Opening	0.549	0.0216
Second Inside Layer	0.634	0.0250	Trace Width	0.127	0.0050
Solder Side	0.634	0.0250	Drill Size for the Via	0.254	0.0100
			Hole Side for the Via	0.152	0.0060

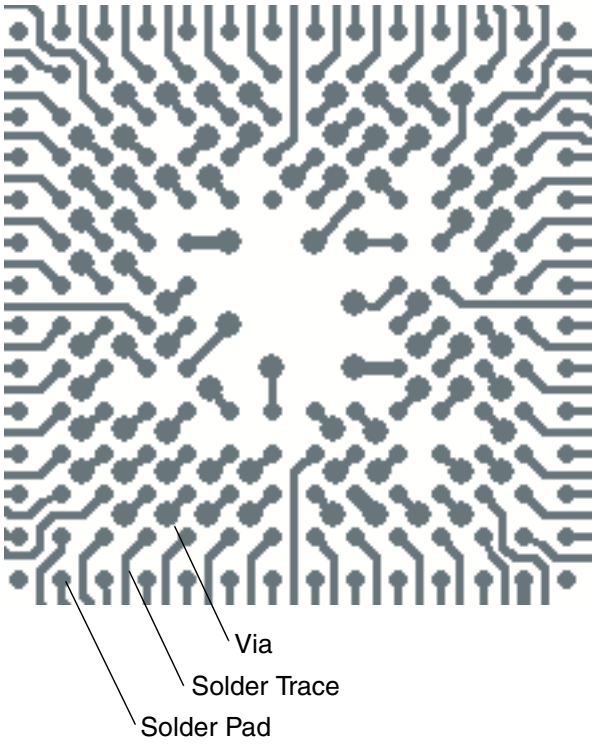


Figure 13-7. 180-Pin µBGA Six-Layer Board Routing Example (Four Routing Layers)—Component Side

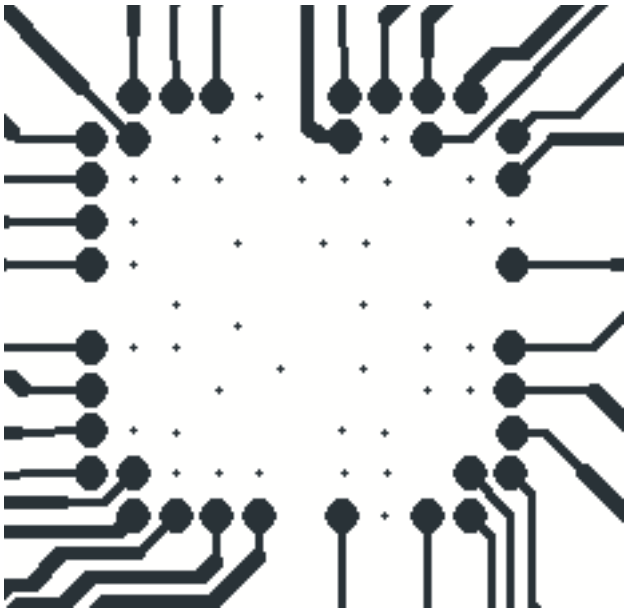


Figure 13-8. 180-Pin µBGA Six-Layer Board Routing Example (Four Routing Layers)—First Inside Layer

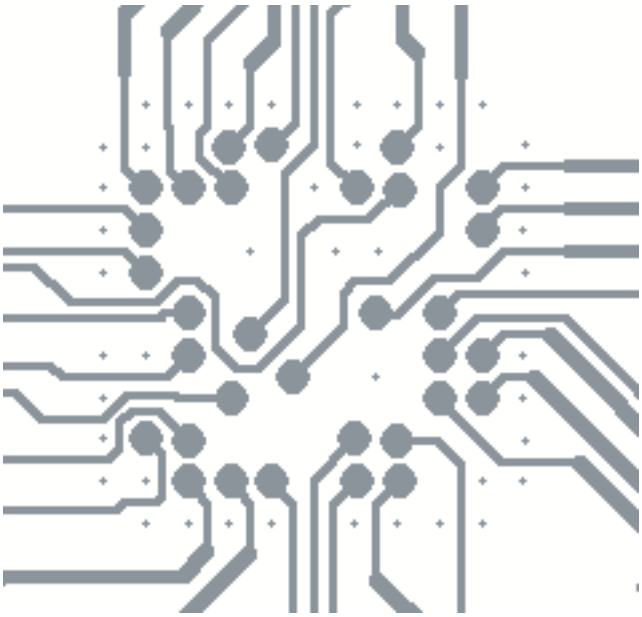


Figure 13-9. 180-Pin µBGA Six-Layer Board Routing Example (Four Routing Layers)—Second Inside Layer

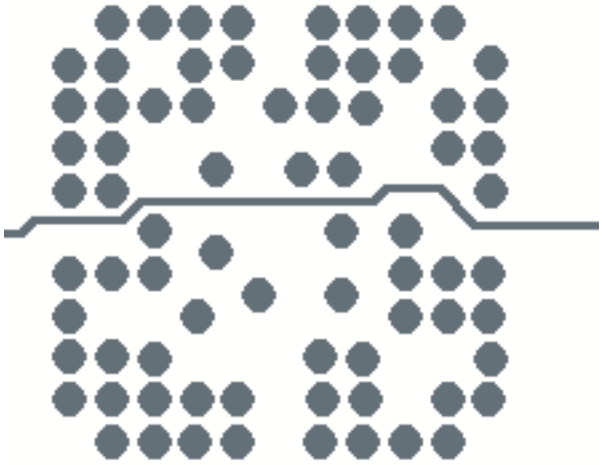


Figure 13-10. 180-Pin µBGA Six-Layer Board Routing Example (Four Routing Layers)—Solder Side

A GENERAL INFORMATION

A.1 ORDERING INSTRUCTIONS

The PCI 9030 is a 32-bit, 33-MHz PCI Bus Target Interface Device featuring advanced SMARTarget technology, which includes a programmable Target interface. The PCI 9030 offers 3.3V, 5V tolerant PCI and Local signaling, supports Universal PCI Adapter designs, 3.3V core, low-power CMOS offered in two package options—176-pin PQFP and 180-pin (ball) µBGA. The device is designed to operate at Industrial Temperature range.

Table A-1. Available Packages

Package	Ordering Part Number
176-pin PQFP	PCI 9030-AA60PI
180-pin µBGA	PCI 9030-AA60BI

A.2 UNITED STATES AND INTERNATIONAL REPRESENTATIVES, AND DISTRIBUTORS

A list of PLX Technology, Inc., representatives and distributors can be found at http://www.plxtech.com.

A.3 TECHNICAL SUPPORT

PLX Technology, Inc., technical support information is listed at http://www.plxtech.com; or call 408 774-9060 or 800 759-3735.

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