Integrated Circuit Systems, Inc.

ICS960002

Power PC Based LBP

Features

- CPU, ASIC, and PCI can run at 2.5V or 3.3V selectable.

- Generates the following system clocks:
  - 1-CPU (2.5V/3.3V) (66.66MHz to 100.00MHz)
  - 2-PCI (2.5V/3.3V) (33.33MHz)
  - 2-ASIC (2.5V/3.3V) (66.66MHz to 100.00MHz)
  - 1-ASIC (2.5V/3.3V) (33.33MHz to 100.00MHz)
  - 1-USB (3.3V) (48MHz)

- SKEW Characteristics:
  - CPU to ASIC < 250ps

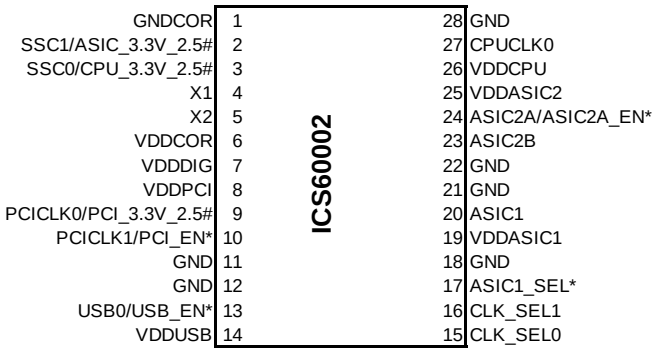
- Jitter Characteristics
  - CPU/ASIC <150ps (cycle to cycle)

-Spread Spectrum features
  - Off
  - -0.5%, 1.0%, and 1.25% Downspread

- Power Management
  - Enable/Disable PCI, ASIC2, and/or USB independently

- Uses external 14.318MHz crystal or reference clock

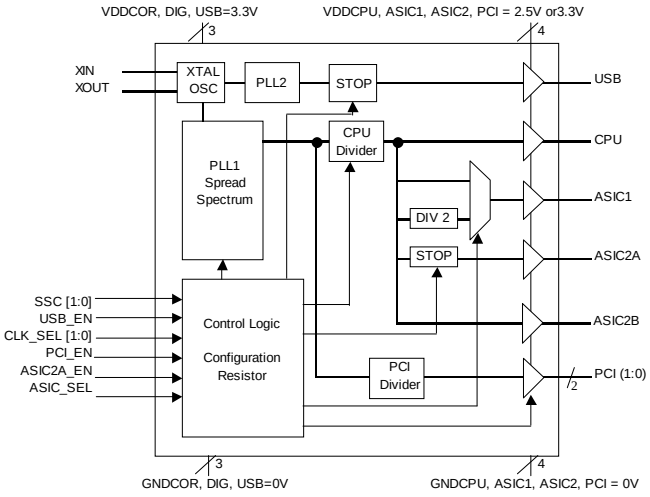
Pin Configuration



Note: * 60Kohm to 120Kohm Internal Pullup Resistor

209Mil SSOP

Block Diagram



Power Groups

Pin Number		Description
VDD	GND	
6, 7	1, 18	3.3V Internal Logic and Core Power
8	11	PCI outputs
14	12	USB outputs
19	21	ASIC1 outputs
25	22	ASIC2 outputs
26	28	CPU ouputs

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	GNDCOR	PWR	Ground pin for the PLL core.
2	SSC1/ASIC_3.3V_2.5#	IN	Spread Spectrum amplitude control with latched VDDASIC 3.3V/2.5V# select.
3	SSC0/CPU_3.3V_2.5#	IN	Spread Spectrum amplitude control with latched VDDCPU 3.3V/2.5V# select.
4	X1	IN	Crystal input,nominally 14.318MHz.
5	X2	OUT	Crystal output, Nominally 14.318MHz
6	VDDCOR	PWR	3.3V power for the PLL core.
7	VDDDIG	PWR	3.3V internal digital power.
8	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
9	PCICLK0/PCI_3.3V_2.5#	I/O	PCI clock output with latched VDDCPU 3.3V/2.5V# select.
10	PCICLK1/PCI_EN*	I/O	PCI clock output with latched PCI enable function at startup.
11	GND	PWR	Ground pin.
12	GND	PWR	Ground pin.
13	USB0/USB_EN*	I/O	USB clock output with latched USB enable function at startup.
14	VDDUSB	PWR	Supply for USB clocks,3.3V nominal
15	CLK_SEL0	IN	Function select pin. See table for details.
16	CLK_SEL1	IN	Function select pin. See table for details.
17	ASIC1_SEL*	IN	Function select pin. See table for details.
18	GND	PWR	Ground pin.
19	VDDASIC1	PWR	Supply for ASIC1clocks,3.3V nominal
20	ASIC1	OUT	ASIC1 clock output.
21	GND	PWR	Ground pin.
22	GND	PWR	Ground pin.
23	ASIC2B	OUT	ASIC2B clock output.
24	ASIC2A/ASIC2A_EN*	I/O	ASIC2A clock output with latched ASIC2A_EN enable function at startup.
25	VDDASIC2	PWR	Supply for ASIC2 clocks,3.3V nominal
26	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
27	CPUCLK0	OUT	CPU clock outputs. 3.3V
28	GND	PWR	Ground pin.

NOTE: Internal pull-up resitors on pin 10, 13, 17, and 24. No internal resistor for pin 2, 3, 9, 15 or 16.

Pin 2, 3 and 9 functionality:
When the device Powers-up, the pin work as latch pin to decide supply voltage on VDDxxx, and then will work as select pin of SS(or output pin).
When High(VDD=3.3V) is latched, the output buffer of xxx will be optimized at VDDxxx=3.3V, When Low(GND) is latched, the output buffer of xxx will be optimized at VDDxxx=2.5V.
The voltage of the latch point is approximate VDDCORE/DIG=1.8V.
and it will take effect within the time of clock stabilization.

Frequency Tables

CLK_SEL1	CLK_SEL0	CPU (MHz)	ASIC1 (MHz)		ASIC2 [A, B] (MHz)
			ASIC1_SEL=1	ASIC1_SEL=0	
0	0	66.66	66.66	33.33	66.66
0	1	100.00	100.00	50.00	100.00
1	0	83.33	83.33	41.67	83.33
1	1	88.88	88.88	44.44	88.88

Spread Spectrum Selection Table

SSC1	SSC0	Spread Spectrum Modulation [MHz]
0	0	OFF
0	1	-0.50% Down Spread
1	0	-1.00% Down Spread
1	1	-1.25% Down Spread

Power Management Table

USB_EN	PCI_EN	ASIC2_EN	USB	PCICLK(1,0)	ASIC2A
0	X	X	Tri-state	X	X
1	X	X	48MHz	X	X
X	0	X	X	Tri-state	X
X	1	X	X	33.3MHz	X
X	X	0	X	X	Tri-state
X	X	1	X	X	SELECTED

Absolute Maximum Ratings

Supply Voltage 5.5V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - AC Specification

T_A = 0 - 70°C; V_{DD} = 3.3 V or 2.5V +/-5%; C_L=20pF(unless otherwise stated)

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Frequency	Z_O		12	14.31818	16	MHz
SST modulation sweep rate	fmod		-	32.2	-	kHz
Transition Time	T_{Trans}	To 1st crossing of target Freq.		1.1	3	ms
Settling Time	T_S	From 1st crossing to 1% target Freq.		1.5	3	ms
Input Capacitance	C_{IN}	Logic Inputs		<2	5	pF
	C_{OUT}	Output pin capacitance		<2	6	pF
	C_{INX}	X1 & X2 pins	27	30	45	pF
Output Rise Time	t_{r2B}	0.8V to 2.0V with no load		0.5	1.5	ns
Output Fall Time	tf_{2B}	2.0V to 0.8V with no load		0.5	1.5	ns
Duty Cycle	d_{t2B}	At VDD/2	45	50	55	%
CPU and ASIC Skew	t_{sk2B}	Equal Power Supply for both ASIC and CPU at same Frequency; Cl =20 pF		200	250	ps
Max. Absolute Period Jitter	$t_{jitabs2B}$	CPU and ASIC only.	-150	-	150	ps
	$t_{jitabs2B}$	PCI	-175	-	175	
	$t_{jitabs2B}$	USB	-150	-	150	
Max. Jitter, cycle to cycle	$t_{jcyc-cyc2B}$	CPU and ASIC only.		90	120	ps
	$t_{jcyc-cyc2B}$	PCI		110	200	ps
	$t_{jcyc-cyc2B}$	USB		95	150	ps

Electrical Characteristics - DC Specification

T_A = 0 - 70°C; V_{DD} =See table below; C_L = 20 pF (unless otherwise stated)

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage	VDDCOR	Nominal voltage is 3.3V	2.97	3.3V	3.63	V
	VDDDIG					
	VDDUSB					
	VDDPCI	Nominal voltage is 3.3V or 2.5V	2.25	2.5V	2.75	V
	VDDASIC1					
	VDDASIC2		2.97	3.3V	3.63	V
	VDDCPU					
Input High Voltage	V_{IH}	For all normal input	2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	For all normal input	V_{SS} - 0.3		0.8	V
Output High Voltage	$V_{OH3.3}$	I_{OH} = -25mA	2.4			V
Output Low Voltage	$V_{OL3.3}$	I_{OL} = 25mA			0.4	V
Output High Voltage	$V_{OH2.5}$	I_{OH} = -25mA	2			V
Output Low Voltage	$V_{OL2.5}$	I_{OL} = 25mA			0.4	V
Operating Supply Current	I_{DD}	No Load		35	50	mA

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used both to provide the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. When no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, then only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

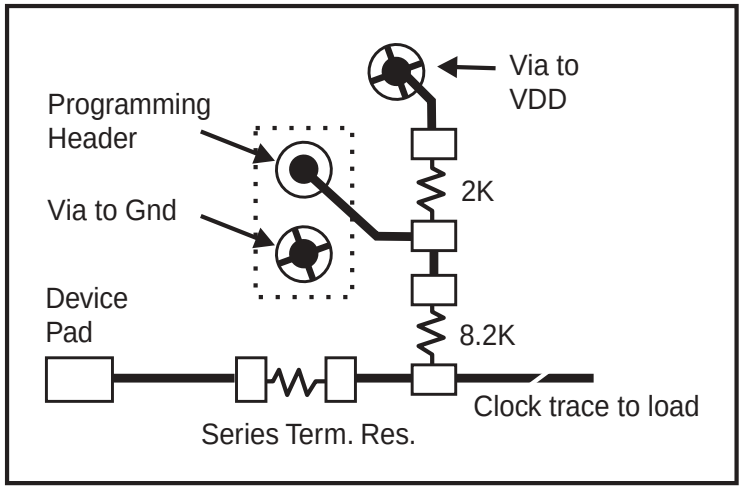
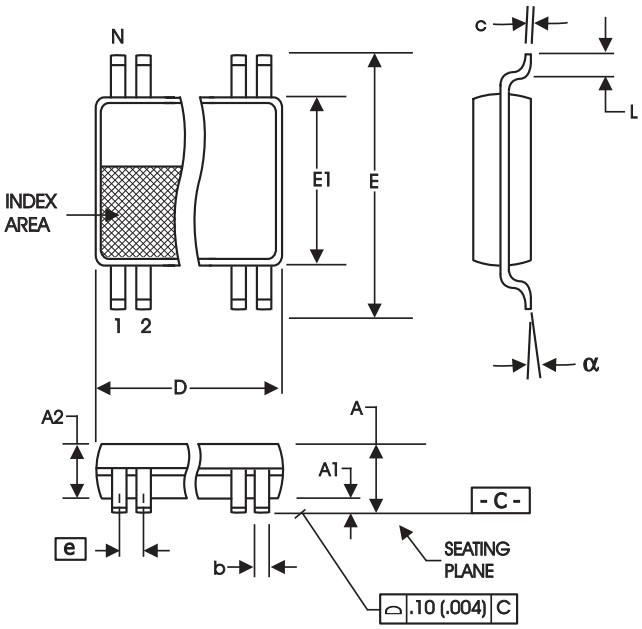


Fig. 1



209 mil SSOP

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SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	2.00	--	.079
A1	0.05	--	.002	--
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
c	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
e	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.90	10.50	.390	.413

Reference Doc.: JEDEC Publication 95, MO-150

10-0033

Ordering Information

ICS960002yF-T

Example:

ICS XXXX y **F - T**

- **Designation for tape and reel packaging**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0677E—03/05/03