NIPPON PRECISION CIRCUITS INC.

SM8702AM

Clock Generator IC

OVERVIEW

The SM8702AM is a clock generator IC that can generate clock signals up to and exceeding 100MHz for personal computer (PC) motherboards. It uses a single 14.318MHz crystal oscillator element and 2 built-in PLLs to simultaneously and independently generate 2 CPU clocks, 6 PCI bus clocks, 2 reference clocks with the same frequency as the crystal element, 48MHz USB interface clock, and 24MHz Super I/O chip clock outputs. It also has 14 outputs that can function as SDRAM clocks by buffering an external input SDRAM clock.

FEATURES

- Intel® Pentium® II, Pentium® III, and AMD x86-compatibles supported
- 2.5/3.3V CPU clock outputs and IOAPIC clock output
- 14 × SDRAM clock outputs (3 DIMMs)
- 2 × CPU clock outputs
  (60), 66, 75, 83, 95, 100, 103, 112, (124), 133MHz CPU/SDRAM clock frequencies. Values in parentheses are available as mask options.
- 6 × PCI bus clock outputs (one free-running output)
  33MHz or 1/2, 1/3, 1/4 of the CPU clock frequency
- 2 × reference clock outputs and 1 × IOAPIC clock output
  14.318MHz REF/IOAPIC clock frequency
- 1 × 48MHz USB interface clock output
- 1 × 24MHz clock output for Super I/O chip
- I^2C serial data bus for frequency/mode output control
- CPU-stop and PCI-stop functions
- Spread Spectrum Clock Generator (SSCG) outputs
  Center spread/Down spread, ± 0.5% or ± 1.5%
- 3.3V (VDD) and 2.5/3.3V (VDDL) supply voltages
- 48-pin SSOP package (pin compatible with ICS9148-26)

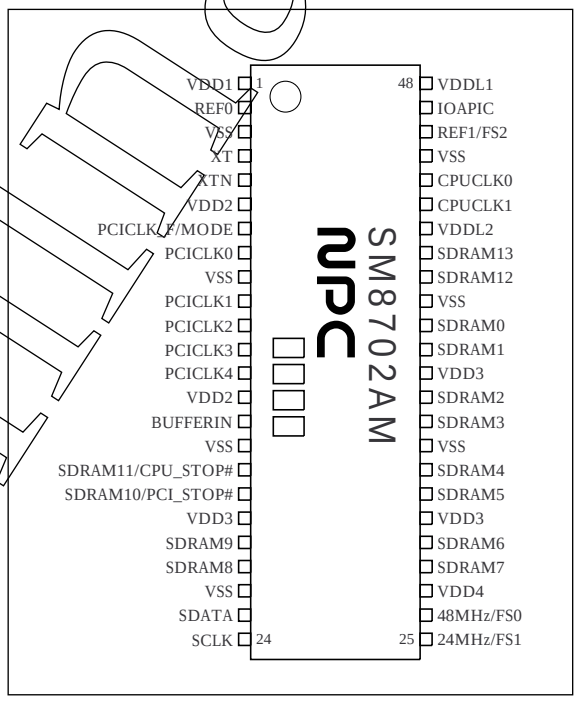
APPLICATIONS

- PC motherboards using Intel® Pentium®, Pentium® II/III, AMD-K6 devices, and x86 architecture CPUs

PINOUT

48-pin SSOP (300 mil)

(Top view)



ORDERING INFORMATION

Device	Package
SM8702AM	48-pin SSOP

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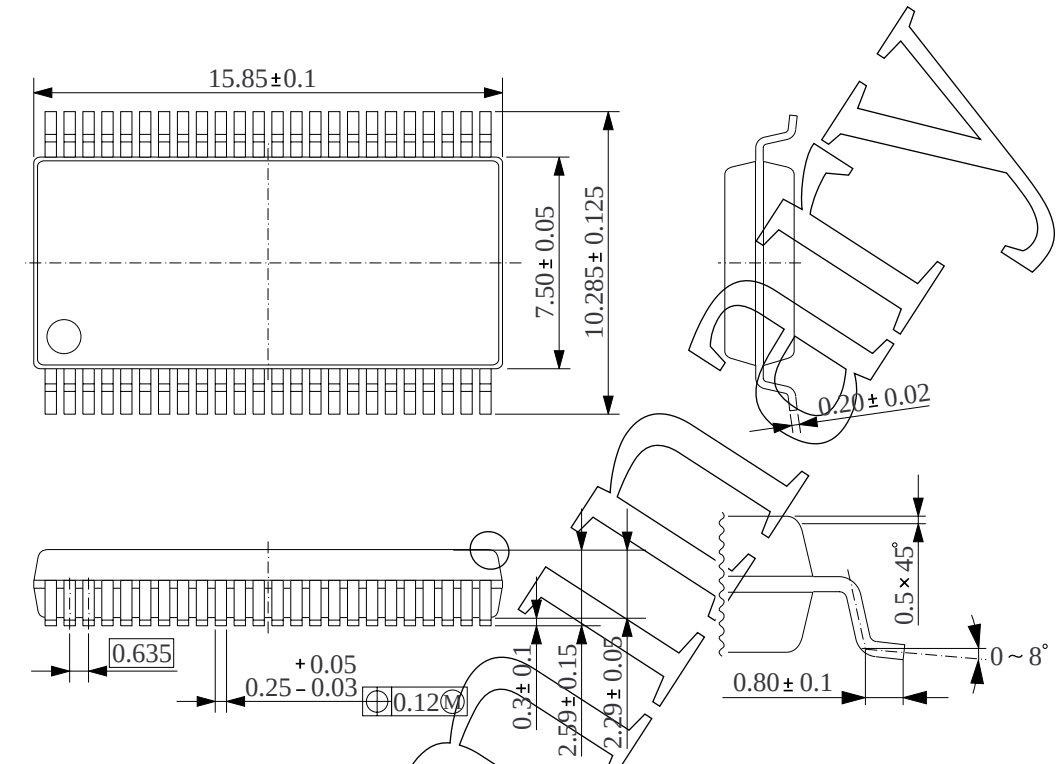
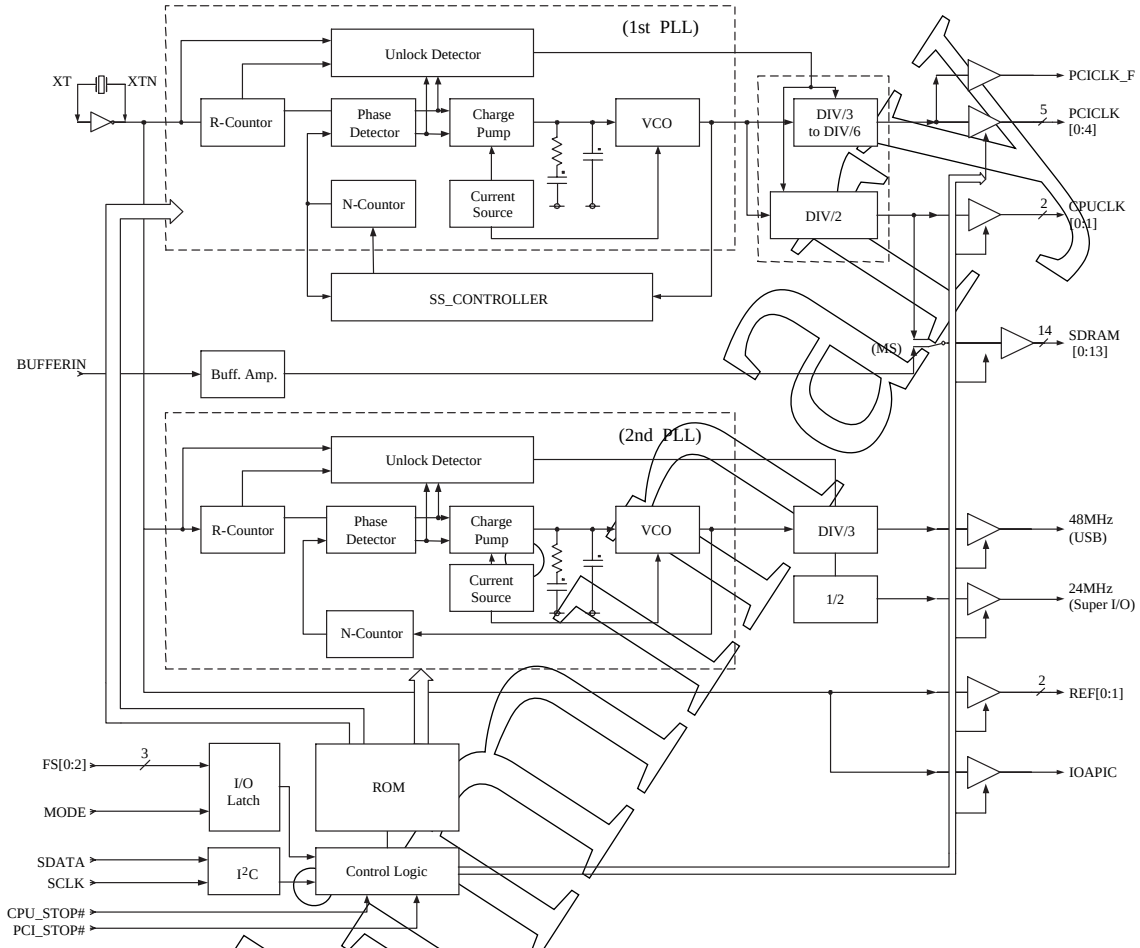
I^2C Bus is a registered trademark of Philips Electronics N. V..

PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Function	Notes
1	VDD1	–	3.3V supply	XT, XTN oscillator, REF[0:1] buffer, stop logic, 3.3V line
2	REF0	I/O	14.318MHz reference clock output	
3	VSS	–	Ground	Crystal oscillator, REF[0:1], 3.3Vline
4	XT	I	Crystal oscillator input	
5	XTN	O	Crystal oscillator output	
6	VDD2	–	3.3V supply	PCI clock output buffers, pre-buffer, stop logic, and internal circuit logic supply
7	PCICLK_F	O	PCI bus free-running clock output	
	MODE	I	Mode settings (latch input)	CPU_STOP# (pin 17) and PCI_STOP# (pin 18) mode select pin. MODE = HIGH: Desktop mode MODE = LOW: Mobile mode
8	PCICLK0	O	PCI bus clock output	
9	VSS	–	Ground (3.3V supply)	PCI clock output buffers, pre-buffer, stop logic
10	PCICLK1	O	PCI bus clock output	

Number	Name	I/O	Function	Notes
11	PCICLK2	O	PCI bus clock output	
12	PCICLK3	O	PCI bus clock output	
13	PCICLK4	O	PCI bus clock output	
14	VDD2	–	3.3V supply	PCI clock output buffers, pre-buffer, stop logic
15	BUFFERIN	I	SDRAM clock input	Input on BUFFERIN is buffered and then output on SDRAM[0:13]
16	VSS	–	Ground (3.3V supply)	SDRAM clock output buffers, pre-buffer, stop logic
17	SDRAM11	I/O	SDRAM clock output	
	CPU_STOP#		CPU clock outputs stop control	In mobile mode (MODE = LOW), CPUCLK[0:1] tied LOW when CPU_STOP# = LOW.
18	SDRAM10	I/O	SDRAM clock output	
	PCI_STOP#		PCI clock outputs stop control	In mobile mode (MODE = LOW), PCICLK[0:4] tied LOW when PCI_STOP# = LOW.
19	VDD3	–	3.3V supply	SDRAM clock output buffers, pre-buffer, stop logic
20	SDRAM9	O	SDRAM clock output	
21	SDRAM8	O	SDRAM clock output	
22	VSS	–	Ground (3.3V supply)	PLL and internal logic ground, I^2C interface, 24MHz/48MHz output ground
23	SDATA	I/O	I^2C serial data input	
24	SCLK	I	I^2C clock input	
25	24MHz	I/O	24MHz clock output	
	FS1		Frequency select 1 (latch input)	
26	48MHz	I/O	48MHz USB clock output	
	FS0		Frequency select 0 (latch input)	
27	VDD4	–	3.3V supply	I^2C interface, 24MHz/48MHz output supply, PLL and internal logic supply
28	SDRAM7	O	SDRAM clock output	
29	SDRAM6	O	SDRAM clock output	
30	VDD3	–	3.3V supply	SDRAM clock output buffers, pre-buffer, stop logic
31	SDRAM5	O	SDRAM clock output	
32	SDRAM4	O	SDRAM clock output	
33	VSS	–	Ground (3.3V supply)	SDRAM clock output buffers, pre-buffer, stop logic
34	SDRAM3	O	SDRAM clock output	
35	SDRAM2	O	SDRAM clock output	
36	VDD3	–	3.3V supply	SDRAM clock output buffers, pre-buffer, stop logic
37	SDRAM1	O	SDRAM clock output	
38	SDRAM0	O	SDRAM clock output	
39	VSS	–	Ground (3.3V supply)	SDRAM clock output buffers, pre-buffer, stop logic
40	SDRAM12	O	SDRAM clock output	
41	SDRAM13	O	SDRAM clock output	
42	VDDL2	–	2.5/3.3V supply	CPU clock output buffers, pre-buffer, stop logic
43	CPUCLK1	O	CPU clock output	
44	CPUCLK0	O	CPU clock output	
45	VSS	–	Ground (2.5/3.3V supply)	CPU clock output buffers, pre-buffer, stop logic
46	REF1	I/O	14.318MHz reference clock output	
	FS2		Frequency select 2 (latch input)	
47	IOAPIC	O	14.318MHz IOAPIC clock output	
48	VDDL1	–	2.5/3.3V supply	IOAPIC output buffer, pre-buffer, stop logic

SPECIFICATIONS

Absolute Maximum Ratings

VDD:VDD1, VDD2, VDD3, VDD4

VDDL:VDDL1, VDDL2 unless otherwise noted.

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD} (V_{DD1},V_{DD2},V_{DD3},V_{DD4})	–0.3 to 6.0	V
	V_{DDL} (V_{DDL1},V_{DDL2})	–0.3 to 6.0	V
	V_{SS}	0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT}	–0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}	–55 to 125	°C
Power dissipation	P_D	0.8	W

Recommended Operating Conditions

V_{SS} = 0V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltages	V_{DD} (V_{DD1},V_{DD2}, V_{DD3},V_{DD4})	Excludes internal core, CPU clock and IOAPIC output stages	3.135	3.300	3.465	V
	V_{DDL} (V_{DDL1},V_{DDL2})	Internal core, CPU clock and IOAPIC output stages	2.375	2.500	2.625	V
Operating temperature range	T_{opr}		0	–	70	°C
Maximum load capacitance	C_{L1}	CPUCLK	10	–	20	pF
	C_{L2}	PCICLK, SDRAM	20	–	30	pF
	C_{L3}	REF, 24/48MHz, IOAPIC	10	–	20	pF
Reference frequency	f_{REF}		–	14.318	–	MHz

DC Electrical Characteristics

T_a = 0 to 70°C, V_{DD} = 3.3V ± 5%, V_{DDL} = 2.5V ± 5%, V_{SS} = 0V unless otherwise noted.

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
HIGH-level input voltage	V_{IH}	All pins excl. XT, XTN		2.0	–	V_{DD}	V
LOW-level input voltage	V_{IL}	All pins excl. XT, XTN, SDATA, SCLK		V_{SS}	–	0.8	V
		SDATA, SCLK: I^2C interface		V_{SS}	–	0.7	
HIGH-level input current	I_{IH}	$V_{IH} = V_{DD}$		–10	–	10	µA
LOW-level input current	I_{IL}	V_{IL} = 0V		–	–	10	µA
HIGH-level output voltage	$V_{OH(3.3V)}$	All clock outputs: I_{OH} = –1mA, V_{DD} = 3.135V	PCICLK, SDRAM, REF, 24/48MHz pins. Also, CPUCLK[0:1] and IOAPIC outputs, when VDDL[1:2] = 3.3V.	2.4	–	–	V
LOW-level output voltage	$V_{OL(3.3V)}$	All clock outputs: I_{OL} = 1mA, V_{DD} = 3.135V		–	–	0.4	V
HIGH-level output voltage	$V_{OH(2.5V)}$	CPUCLK[0:1], IOAPIC: I_{OH} = –1mA, V_{DDL} = 2.375V	CPUCLK[0:1] and IOAPIC outputs, when VDDL[1:2] = 2.5V.	2.0	–	–	V
LOW-level output voltage	$V_{OL(2.5V)}$	CPUCLK[0:1], IOAPIC: I_{OL} = 1mA, V_{DDL} = 2.375V		–	–	0.4	V
HIGH-level output current	I_{OH}	CPUCLK[0:1]: V_{OH} = 1.7V	f_{OUT} = 66.5MHz	8.5		23.0	mA
		PCICLK_F, PCICLK[0:4]: V_{OH} = 2.0V		18.7	–	42.6	
		SDRAM[0:13]: V_{OH} = 2.0V		18.7	–	42.6	
		REF[0:1], 24/48MHz: V_{OH} = 2.0V		18.7	–	42.6	
		IOAPIC: V_{OH} = 1.7V		8.5	–	23.0	
LOW-level output current	I_{OL}	CPUCLK[0:1]: V_{OL} = 0.7V	f_{OUT} = 66.5MHz	11.0	–	25.3	mA
		PCICLK_F, PCICLK[0:4]: V_{OL} = 0.8V		18.7	–	40.3	
		SDRAM[0:13]: V_{OL} = 0.8V		18.7	–	40.3	
		REF[0:1], 24/48MHz: V_{OL} = 0.8V		18.7	–	40.3	
		IOAPIC: V_{OL} = 0.7V		11.0	–	25.3	
Output leakage current	I_{OZ}	Outputs high impedance		–10	–	10	µA
Current consumption	I_{DD}	C_L = 0pF, V_{DD} = 3.465V	f_{OUT} = 66.5MHz	–	–	180	mA
	I_{DDL1}	C_L = 0pF, V_{DDL} = 3.465V		–	–	30	
	I_{DDL2}	C_L = 0pF, V_{DDL} = 2.625V		–	–	20	

AC Electrical Characteristics

CPU clock characteristics 1

T_a = 0 to 70°C, V_{DD} = 3.3V ± 5%, V_{DDL} = 2.5V ± 5%, V_{SS} = 0V, $f_{X'tal}$ = 14.318MHz, C_L = 20pF unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output clock rise time[1]	t_r	V_{OL} = 0.4V → V_{OH} = 2.0V transition time		–	–	2.0	ns
Output clock fall time[1]	t_f	V_{OH} = 2.0V → V_{OL} = 0.4V transition time		–	–	2.0	ns
Duty cycle	Dt	V_T = 1.25V		45	50	55	%
Output clock jitter[1]	t_{jc}	V_T = 1.25V, rising edge	Cycle-to-cycle jitter	–	–	250	ps
Output clock skew[1]	t_{skw}	V_T = 1.25V, rising edge	Between CPUCLK0 and CPUCLK1	–	–	250	ps
Clock frequency stabilize time[1]	t_{stb}	Cold start	Supply ON (V_{DD} = 3.3V) until clock reaches specified frequency	–	–	3	ms
Output impedance[2]	Z_O	V_O = 0.5V_{DDL}		10	–	90	Ω

1. Design maximum values, not 100% guaranteed.
2. Design estimate values, not 100% guaranteed.

CPU clock characteristics 2

T_a = 0 to 70°C, V_{DD} = V_{DDL} = 3.3V ± 5%, V_{SS} = 0V, $f_{X'tal}$ = 14.318MHz, C_L = 20pF unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output clock rise time[1]	t_r	V_{OL} = 0.4V → V_{OH} = 2.4V transition time		–	–	2.5	ns
Output clock fall time[1]	t_f	V_{OH} = 2.4V → V_{OL} = 0.4V transition time		–	–	2.5	ns
Duty cycle	Dt	V_T = 1.5V		45	50	55	%
Output clock jitter[1]	t_{jc}	V_T = 1.5V, rising edge	Cycle-to-cycle jitter	–	–	250	ps
Output clock skew[1]	t_{skw}	V_T = 1.5V, rising edge	Between CPUCLK0 and CPUCLK1	–	–	250	ps
Clock frequency stabilize time[1]	t_{stb}	Cold start	Supply ON (V_{DD} = 3.3V) until clock reaches specified frequency	–	–	3	ms
Output impedance[2]	Z_O	V_O = 0.5V_{DDL}		10	–	60	Ω

1. Design maximum values, not 100% guaranteed.
2. Design estimate values, not 100% guaranteed.

PCI clock characteristics

T_a = 0 to 70°C, V_{DD} = 3.3V ± 5%, V_{SS} = 0V, $f_{X'tal}$ = 14.318MHz, C_L = 30pF unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output clock rise time[1]	t_r	V_{OL} = 0.8V → V_{OH} = 2.4V transition time		–	–	2.0	ns
Output clock fall time[1]	t_f	V_{OH} = 2.4V → V_{OL} = 0.8V transition time		–	–	2.0	ns
Duty cycle	Dt	V_T = 1.5V		45	50	55	%
Output clock jitter[1]	t_{jc}	V_T = 1.5V, rising edge	Cycle-to-cycle jitter	–	–	250	ps
Output clock skew[1]	t_{skw}	V_T = 1.5V, rising edge	Between PCI clocks: PCICLK_F and PCICLK[0:4]	–	–	250	ps
CPU/PCI clock skew[2]	t_{hpsk}	$V_{T\text{-}CPUCLK}$ = 1.25/1.5V, $V_{T\text{-}PCICLK}$ = 1.5V, rising edges	Between CPU and PCI clocks: CPUCLK[0:1] and PCICLK_F/PCICLK[0:4]	1.0	2.2	4.0	ns
Clock frequency stabilize time[1]	t_{stb}	Cold start	Supply ON (V_{DD} = 3.3V) until clock reaches specified frequency	–	–	3	ms
Output impedance[3]	Z_O	V_O = 0.5V_{DD}		10	–	60	Ω

1. Design maximum values, not 100% guaranteed.
2. CPUCLK and PCICLK rising edges, $V_{T\text{-}CPUCLK}$ = 1.25V (V_{DDL} = 2.5V)/1.5V (V_{DDL} = 3.3V), $V_{T\text{-}PCICLK}$ = 1.5V skew measurement.
3. Design estimate values, not 100% guaranteed.

SDRAM clock characteristics

T_a = 0 to 70°C, V_{DD} = V_{DDL} = 3.3V ± 5%, V_{SS} = 0V, $f_{X'tal}$ = 14.318MHz, C_L = 30pF unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output clock rise time[1]	t_r	V_{OL} = 0.8V → V_{OH} = 2.4V transition time		–	–	2.0	ns
Output clock fall time[1]	t_f	V_{OH} = 2.4V → V_{OL} = 0.8V transition time		–	–	2.0	ns
Duty cycle[1]	Dt	V_T = 1.5V, BUFFERIN input clock signal rise and fall time rate ≥ 1V/ns	3.3V BUFFERIN input clock signal logic level	40	50	60	%
Output clock skew[1]	t_{skw}	V_T = 1.5V, rising edge, BUFFERIN input clock signal rise and fall time rate ≥ 1V/ns	Between SDRAM clocks: SDRAM[0:13]	–	200	600	ps
Input to output propagation delay[2,3]	t_{pd}	$V_{T\text{-}BUFFERIN}$ = 1.5V, $V_{T\text{-}SDRAM}$ = 1.5V, rising edges, BUFFERIN input clock signal rise and fall time rate ≥ 1V/ns	Between BUFFERIN and SDRAM[0:13]	–	5.5	7.0	ns
Output impedance[3]	Z_O	V_O = 0.5V_{DD}		10	–	60	Ω

1. Design maximum values, not 100% guaranteed.
2. BUFFERIN and SDRAM rising edges, $V_{T\text{-}BUFFERIN}$ = 1.5V (logic level = 3.3V), $V_{T\text{-}SDRAM}$ = 1.5V delay measurement.
3. Design estimate values, not 100% guaranteed.

24MHz/48MHz, REF[0:1] clock characteristics

T_a = 0 to 70°C, V_{DD} = 3.3V ± 5%, V_{SS} = 0V, $f_{X'tal}$ = 14.318MHz, C_L = 20pF unless otherwise noted.

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
Output clock rise time[1]	t_r	V_{OL} = 0.8V → V_{OH} = 2.4V transition time		–	–	2.0	ns
Output clock fall time[1]	t_f	V_{OH} = 2.4V → V_{OL} = 0.8V transition time		–	–	2.0	ns
Duty cycle[1]	Dt	V_T = 1.5V		40	50	60	%
Output clock jitter[1]	t_{jc}	V_T = 1.5V, rising edge	Absolute jitter	–	250	800	ps
Clock frequency stabilize time[1]	t_{stb}	Cold start	Supply ON (V_{DD} = 3.3V) until clock reaches specified frequency	–	–	3	ms
Output impedance[2]	Z_O	V_O = 0.5V_{DD}		10	–	60	Ω

1. Design maximum values, not 100% guaranteed.
2. Design estimate values, not 100% guaranteed.

IOAPIC clock characteristics

T_a = 0 to 70°C, V_{DD} = 3.3V ± 5%, V_{SS} = 0V, $f_{X'tal}$ = 14.318MHz, C_L = 20pF unless otherwise noted.

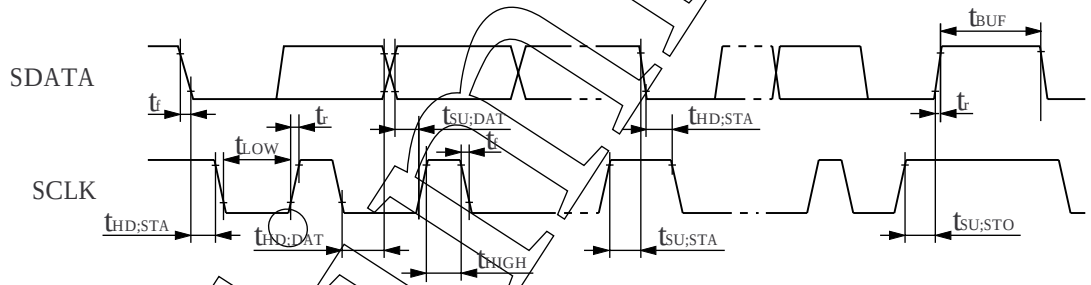
Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
Output clock rise time[1]	t_r	V_{OL} = 0.8V → V_{OH} = 2.4V transition time, V_{DDL1} = 3.3V		–	–	2.0	ns
		V_{OL} = 0.4V → V_{OH} = 2.0V transition time, V_{DDL1} = 2.5V		–	–	2.0	
Output clock fall time[1]	t_f	V_{OH} = 2.4V → V_{OL} = 0.8V transition time, V_{DDL1} = 3.3V		–	–	2.0	ns
		V_{OH} = 2.0V → V_{OL} = 0.4V transition time, V_{DDL1} = 2.5V		–	–	2.0	
Duty cycle[1]	Dt	V_T = 1.5V, V_{DDL1} = 3.3V		40	50	60	%
Output clock jitter[1]	t_{jc}	V_T = 1.5V, rising edge	Absolute jitter	–	250	800	ps
Clock frequency stabilize time[1]	t_{stb}	Cold start	Supply ON (V_{DD} = 3.3V) until clock reaches specified frequency	–	–	3	ms
Output impedance[2]	Z_O	V_O = 0.5V_{DD}		10	–	90	Ω

1. Design maximum values, not 100% guaranteed.
2. Design estimate values, not 100% guaranteed.

I²C serial interface electrical characteristics

T_a = 0 to 70°C, V_{DD} = 3.3V ± 5%, V_{SS} = 0V, $f_{X'tal}$ = 14.318MHz, C_L = 30pF unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Serial clock frequency	f_{SCLK}	I²C standard mode	0	–	100	kHz
Serial clock start state hold time	$t_{HD;STA}$		4.0	–	–	µs
Serial clock LOW-level pulsewidth	t_{LOW}		4.7	–	–	µs
Serial clock HIGH-level pulsewidth	t_{HIGH}		4.0	–	–	µs
Successive start state setup time	$t_{SU;STA}$		4.7	–	–	µs
Data hold time	$t_{HD;DAT}$	I²C device data	0	–	3.45	µs
Data input setup time	$t_{SU;DAT}$		250	–	–	ns
Pulse rise time	t_r		–	–	1000	ns
Pulse fall time	t_f		–	–	300	ns
Stop state setup time	$t_{SU;STO}$		4.0	–	–	µs
Serial data bus buffer time	t_{BUF}		4.7	–	–	µs
Bus line load capacitance	C_b		–	–	400	pF



I²C serial data timing

FUNCTIONAL DESCRIPTION

Mode Setting Overview

There are 2 methods that can be used to set the frequency and clock output start/stop operating modes.

- Using external inputs (pins 7, 17, 18, 25, 26, 46) or,
- Using data read in from an I^2C serial interface.

The default state is where the operating state is set by external pin control. Thus, the output frequency can be set by FS[0:2] (pins 25, 26, 46). Note that the SSCG function is OFF in this case. If the I^2C serial data byte 0 bit 3 is set to 1, then the output frequency is determined by data using the I^2C interface. Then, the Spread Spectrum function (SSCG) can be selected using I^2C data. However, if mode settings using I^2C data and external pin control conflict or overlap, the mode settings dictated by I^2C data have precedence over external pin control.

During normal operation, pins 17 and 18 can function as SDRAM clock outputs (desktop mode) or they can function as CPUCLK output stop control and PCICLK output stop control (mobile mode), depending on the state of MODE (pin 7) when power is first applied.

In addition to output frequency settings, other operating mode settings which can be controlled by I^2C serial data include SSCG operation and mode, and output pin grouping enable/disable switching.

Hardware Frequency Selection

When power is applied, the frequency setting is controlled by FS[0:2] when byte 0 bit 3 is set to 0. Note that if byte 0 bit 3 is set to 1, the frequency is selected by bits 4 to 6 in the same manner as inputs FS0 to FS2.

Inputs			Output frequency	
FS2	FS1	FS0	CPUCLK [MHz]	PCICLK [MHz]
HIGH	HIGH	HIGH	100.2	33.4
HIGH	HIGH	LOW	133	33.2
HIGH	LOW	HIGH	112.1	37.3
HIGH	LOW	LOW	103	34.3
LOW	HIGH	HIGH	66.5	33.2
LOW	HIGH	LOW	83.3	41.6
LOW	LOW	HIGH	74.9	37.4
LOW	LOW	LOW	94.7	31.6

Mode and Power Management Inputs

The SM8702AM supports 2 operating modes, desktop mode and mobile mode, selected by MODE (pin 7).

If MODE is HIGH when power is first applied, desktop mode is selected. In this mode, pins 17 and 18 function as SDRAM clock outputs, SDRAM11 and SDRAM10, respectively.

If MODE is LOW when power is first applied, mobile mode is selected. In this mode, pins 17 and 18 function as the CPU clock (CPUCLK[0:1]) and PCI clock (PCICLK[0:4]) output stop control signal inputs, CPU_STOP# and PCI_STOP#, respectively. This function is used mainly to reduce power consumption.

MODE	Pin 17	Pin 18	Mode
HIGH	SDRAM11	SDRAM10	Desktop mode Pins 17 and 18 are outputs.
LOW	CPU_STOP#	PCI_STOP#	Mobile mode Pins 17 and 18 are inputs.

Operating Mode Summary

The state of the various external inputs and outputs in the operating modes is indicated in the following table.

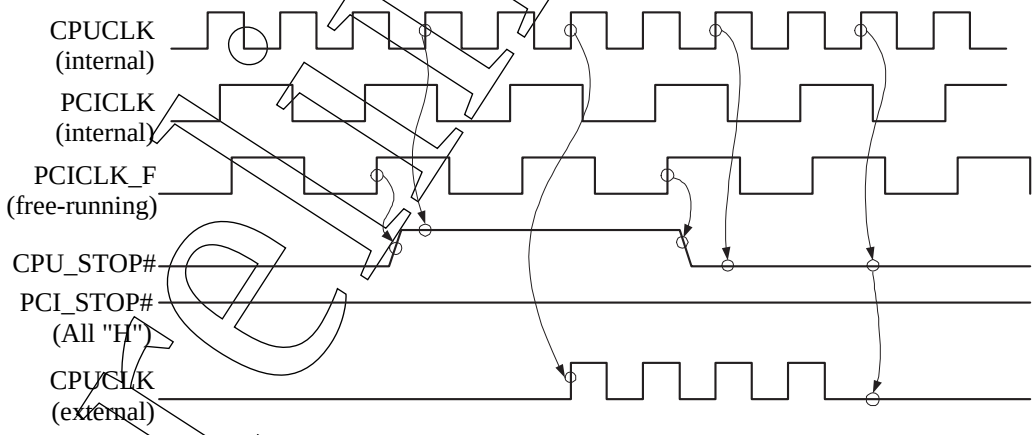
MODE	SDRAM11/ CPU_STOP#	SDRAM10/ PCI_STOP#	CPUCLK[0:1]	PCICLK[0:4]	PCICLK_F, 24MHz/48MHz, SDRAM[0:13]	Crystal oscillator	VCO (internal signal)	Notes[1]
MODE = HIGH (desktop mode)	Enabled (SDRAM output)	Enabled (SDRAM output)	Enabled	Enabled	Enabled	Enabled	Enabled	Desktop mode. Pins 17 and 18 function as outputs.
MODE = LOW (mobile mode)	HIGH (CPU_STOP#input)	HIGH (PCI_STOP# input)	Enabled	Enabled	Enabled	Enabled	Enabled	Mobile mode. Pins 17 and 18 function as inputs. Pin 17 = CPU_STOP# Pin 18 = PCI_STOP#
	HIGH (CPU_STOP#input)	LOW (PCI_STOP# input)	Enabled	Disabled	Enabled	Enabled	Enabled	
	LOW (CPU_STOP#input)	HIGH (PCI_STOP# input)	Disabled	Enabled	Enabled	Enabled	Enabled	
	LOW (CPU_STOP#input)	LOW (PCI_STOP# input)	Disabled	Disabled	Enabled	Enabled	Enabled	

1. Enabled = output functions active. Disabled = LOW-level output.

CPU Clock Stop Function

In mobile mode, selected using MODE (pin 7), the CPUCLK[0:1] clock outputs can be stopped by external pin control. The asynchronous stop signal input on CPU_STOP# is sampled internally on the rising edge of the PCI free-running output clock (PCICLK_F).

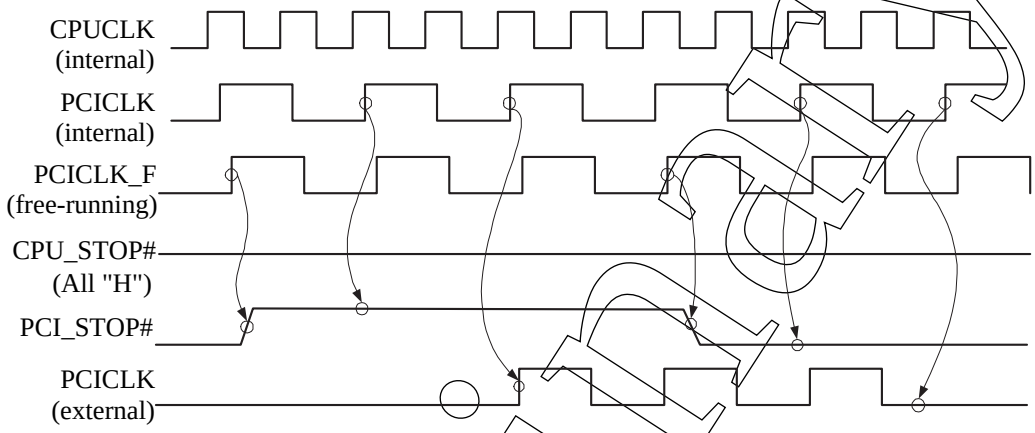
When CPU_STOP# goes LOW, the CPU clock outputs (CPUCLK) stop after a delay of 2 to 4 clock cycles. When CPU_STOP# goes HIGH, the CPU clock outputs start after a delay of 2 to 4 clock cycles. The actual start and stop delay varies with the output frequency up to a maximum of 4 CPU clock cycles.



PCI Clock Stop Function

In mobile mode, selected using MODE (pin 7), the PCICLK[0:4] clock outputs can be stopped by external pin control, in the same way as the CPU clock stop function.

When PCI_STOP# goes LOW, the PCI clock outputs (PCICLK) stop, and when PCI_STOP# goes HIGH, the PCI clock outputs start. In either case, the PCI_STOP# signal is sampled internally on the rising edge of PCICLK, and the output state transition occurs with 1 PCI clock cycle delay.



I²C Bus Serial Data Format

The format of the I²C serial data on SDATA (pin 23) which is input in sync with the serial data clock on SCLK (pin 24) is shown below.

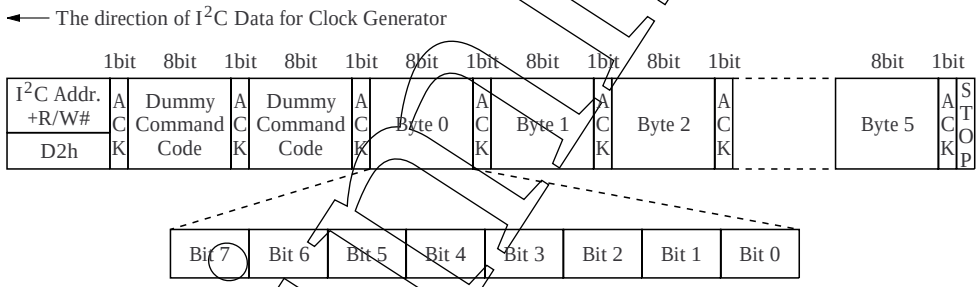
The SM8702AM I²C address is given below.

A6	A5	A4	A3	A2	A1	A0	R/W#
1	1	0	1	0	0	1	

R/W# = 0 or 1

In the start sequence, the I²C bus serial data is fed into the clock generator in the following direction.

1. I²C address with R/W# = 0
2. ACK acknowledge bit
3. Two successive 8-bit dummy command code data words (including ACK acknowledge bit)
4. 8-bit dummy command code (Byte 0 to Byte 5)



The data transfer speed is 100k bps (I²C standard mode), with input logic level of 3.3V. When power is first applied, all internal registers are restored to their default state as below.

- Byte0 : default = 0 (bit 0 to bit 3 and bit 7)
  : default = 1 (bit 4 to bit 6)
- Byte 1 to Byte 5 : default = 1 (all bits)

I²C Bus Data Bytes

Byte 0: function and frequency select

Bit	Function	Power-ON default	Notes
7	0: Spread spectrum ± 1.5% modulation 1: Spread spectrum ± 0.5% modulation	0	The spread spectrum accuracy of modulation is not guaranteed.
6:4	Frequency select bits Bit 6 / Bit 5 / Bit 4 / CPUCLK [MHz] / PCICLK [MHz] 1 1 1 100.2 33.4 1 1 0 133 33.2 1 0 1 112.1 37.3 1 0 0 103 34.3 0 1 1 66.5 33.2 0 1 0 83.3 41.6 0 0 1 74.9 37.4 0 0 0 94.7 31.6	1	The power-ON default for bits 4 to 6 is 1. When bit 3 is set to 1 (I²C select), bits 4 to 6 select the frequency in the same write cycle timing.
3	0: Hardware frequency select using FS[0:2] 1: I²C bus serial data frequency select	0	FS[0:2] are latch inputs
2	0: Spread spectrum center spread select 1: Spread spectrum down spread select	0	
1	0: Normal operating mode (SSCG disabled) 1: Spread spectrum operating mode (SSCG enabled)	0	
0	0: Normal output mode (running) 1: Three-state output mode	0	All outputs are high impedance when bit 0 is set to 1.

Byte 1: CPU register

Bit	Pin number	Power-ON default[1]	Notes
7	26	1	48MHz USB
6	25	1	24MHz (Super I/O)
5	–	1	(Reserved)
4	–	1	(Reserved)
3	–	1	(Reserved)
2	–	1	(Reserved)
1	43	1	CPUCLK1 enable
0	44	1	CPUCLK0 enable

1. 1 = enabled, 0 = disabled

Byte 2: PCI register

Bit	Pin number	Power-ON default[1]	Notes
7	–	1	(Reserved)
6	7	1	PCICLK_F enable
5	–	1	(Reserved)
4	14	1	PCICLK4 enable
3	12	1	PCICLK3 enable
2	11	1	PCICLK2 enable
1	10	1	PCICLK1 enable
0	8	1	PCICLK0 enable

1. 1 = enabled, 0 = disabled

Byte 3: SDRAM register

Bit	Pin number	Power-ON default[1]	Notes
7	–	1	(Reserved)
6	–	1	(Reserved)
5	–	1	(Reserved)
4	–	1	(Reserved)
3	17, 18	1	SDRAM[10:11] enable in desktop mode only (MODE = HIGH)
2	20, 21, 40, 41	1	SDRAM[8,9,12,13] enable
1	28, 29, 31, 32	1	SDRAM[4:7] enable
0	34, 35, 37, 38	1	SDRAM[0:3] enable

1. 1 = enabled, 0 = disabled

Byte 4: Reserved register

Bit	Pin number	Power-ON default[1]	Notes
7	–	1	(Reserved)
6	–	1	(Reserved)
5	–	1	(Reserved)
4	–	1	(Reserved)
3	–	1	(Reserved)
2	–	1	(Reserved)
1	–	1	(Reserved)
0	–	1	(Reserved)

1. 1 = enabled, 0 = disabled

Byte 5: REF/IOAPIC register

Bit	Pin number	Power-ON default[1]	Notes
7	–	1	(Reserved)
6	–	1	(Reserved)
5	–	1	(Reserved)
4	47	1	IOAPIC enable
3	–	1	(Reserved)
2	–	1	(Reserved)
1	46	1	REF1 enable
0	2	1	REF0 enable

1. 1 = enabled, 0 = disabled

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