Power driver IC for CD changer

BD7961FM

BD7961FM is a 6-channel driver IC developed for CD changer. In addition to the 4-channel BTL driver and the 2-channel loading driver, the 3.3V regulator and 5.0V regulator used in the peripheral circuit are also incorporated. The size reduction of the set is achieved by integrating functions that were used in two chips into a single chip.

●Applications

CD changer

●Features

1) This circuit is a 6-channel driver IC consisting of four BTL drivers and two loading drivers.
2) Two wide dynamic range loading drivers of MOS output (R_{ON}=1.0Ω).
3) The circuit is provided with loading driver voltage setting terminals.
4) A 5.0V regulator and a 3.3V regulator are built in.
   (Each regulator has an external PNP transistor and an ON/OFF switch)
5) The circuit has a mute switch.
6) A thermal shutdown circuit is built in.
7) Since HSOP-M36 power package is used, the set requires a reduced space.

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	15	V
Power dissipation	Pd	2200*	mW
Operating temperature range	Topr	−35 to +85	°C
Storage temperature range	Tstg	−55 to +150	°C

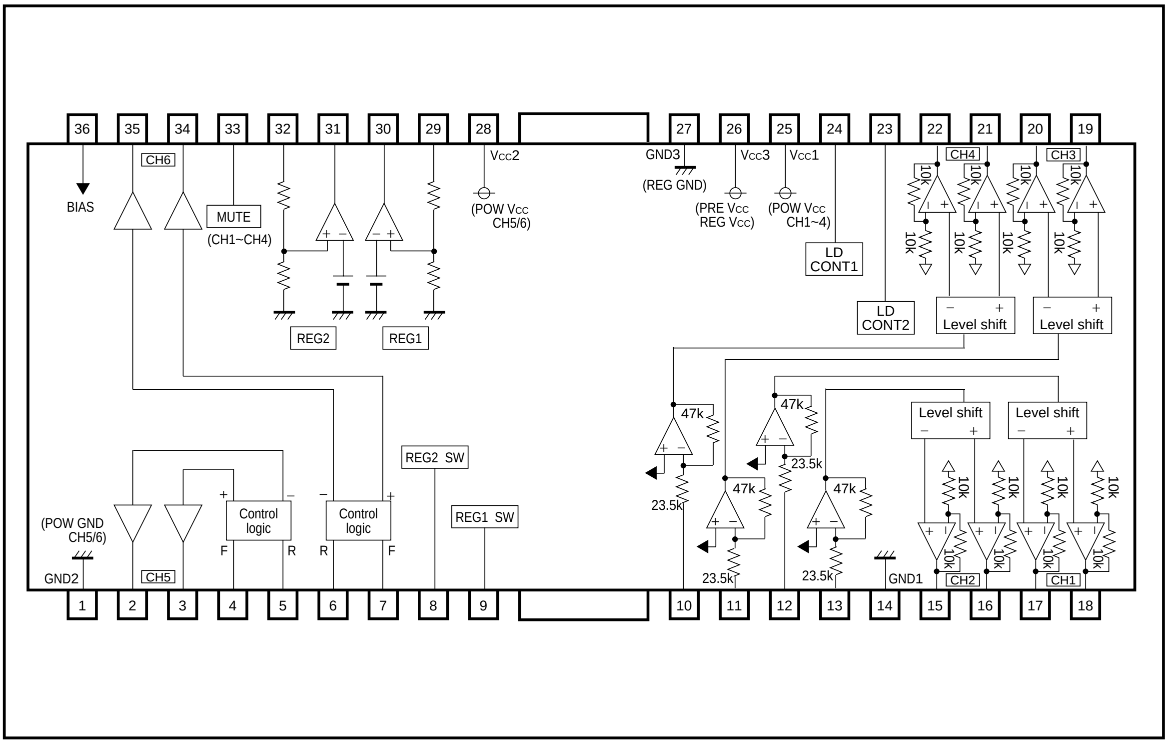
* Reduced by 17.6mW for each increase in Ta of 1°C over 25°C, on less than 3% (percentage occupied by copper foil), 70mm×70mm, t=1.6mm, glass epoxy mounting.

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage 1	$V_{CC}1$	4.5	8.0	14.0	V
Supply voltage 2	$V_{CC}2$	4.5	8.0	14.0	V
Supply voltage 3*	$V_{CC}3$	6.0	8.0	14.0	V

* When REG2 (5.0-V regulator) is not used, the supply voltage3 (VCC3) is 4.5 to 14.0V.

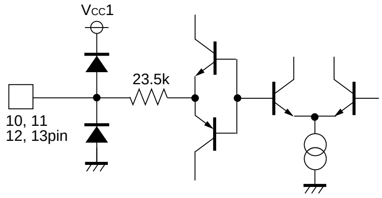
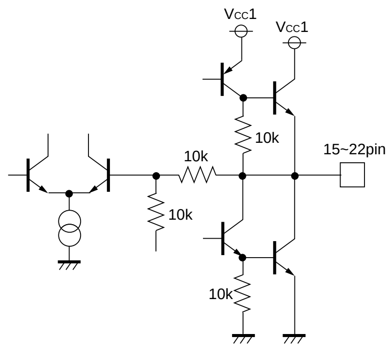
●Block diagram

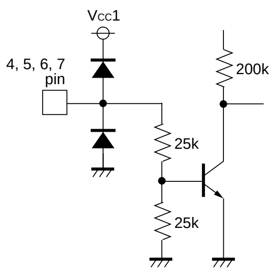
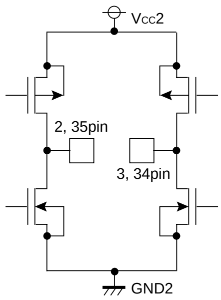
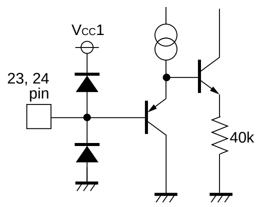


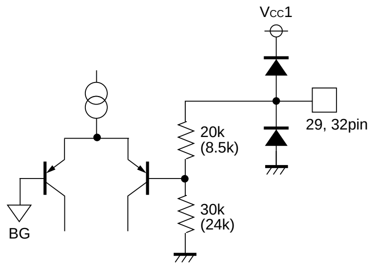
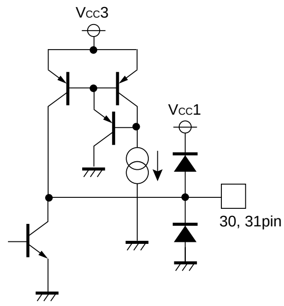
●Pin descriptions

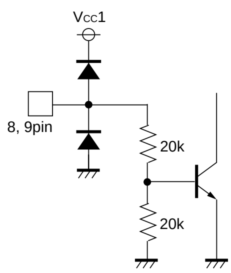
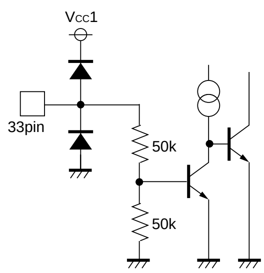
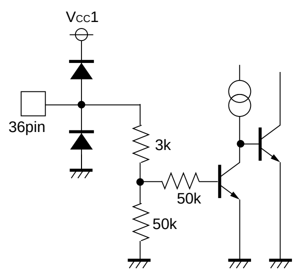
Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	GND2	POW GND (loading driver unit)	19	OUT3+	BTL driver (CH3) output +
2	OUT5–	Loading driver (CH5) output –	20	OUT3–	BTL driver (CH3) output –
3	OUT5+	Loading driver (CH5) output +	21	OUT4+	BTL driver (CH4) output +
4	IN5FWD	Loading driver (CH5) FWD input	22	OUT4–	BTL driver (CH4) output –
5	IN5REV	Loading driver (CH5) REV input	23	LDCONT2	Loading driver (CH6) voltage setting terminal
6	IN6REV	Loading driver (CH6) REV input	24	LDCONT1	Loading driver (CH5) voltage setting terminal
7	IN6FWD	Loading driver (CH6) FWD input	25	Vcc1	Supply voltage (BTL driver unit)
8	REG2SW	Regulator 2 switch terminal	26	Vcc3	Supply voltage (regulator unit)
9	REG1SW	Regulator 1 switch terminal	27	GND3	REG GND (regulator unit)
10	IN4	CH4 input	28	Vcc2	Supply voltage (loading driver unit)
11	IN3	CH3 input	29	REG1OUT	Regulator 1 output
12	IN1	CH1 input	30	REG1_B	Regulator 1 Tr base
13	IN2	CH2 input	31	REG2_B	Regulator 2 Tr base
14	GND1	POW GND (BTL driver unit)	32	REG2OUT	Regulator 2 output
15	OUT2–	BTL driver (CH2) output –	33	MUTE	BTL driver mute terminal
16	OUT2+	BTL driver (CH2) output +	34	OUT6+	Loading driver (CH6) output +
17	OUT1–	BTL driver (CH1) output –	35	OUT6–	Loading driver (CH6) output –
18	OUT1+	BTL driver (CH1) output +	36	BIAS	BIAS terminal

●Input output circuit

IN1/IN2/IN3/IN4	OUT1+/OUT1–/OUT2+/OUT2– OUT3+/OUT3–/OUT4+/OUT4–
	

IN5FWD/IN5REV IN6FWD/IN6REV	OUT5+/OUT5– OUT6+/OUT6–	LDCONT1/LDCONT2
		

REG1OUT/REG2OUT	REG1_B/REG2_B
	

REG1SW/REG2SW	MUTE	BIAS
		

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●Electrical characteristics

(unless otherwise noted, Ta=25°C, $V_{CC}1$, $V_{CC}2$, $V_{CC}3$=8V, BIAS=2.5V, R_L=8Ω)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	$I_{CC}1$	12	25	38	mA	Under no load
Quiescent current (BTL MUTE)	$I_{CC}2$	5	10	15	mA	Under no load
〈 BTL driver CH1 to CH4 〉						
Output offset voltage	V_{OFS}	–70	0	+70	mV	
Max. output amplitude	V_{OM}	5.4	6.0	–	V	
Closed circuit voltage gain	G_{VC}	16	18	20	dB	V_{IN}=BIAS±0.5V
Difference between positive and nagative voltage gains	ΔG_{VC}	–2.0	0	2.0	dB	
〈 Loading driver CH5 and CH6 〉						
Output offset voltage	V_{OFSL}	–35	0	+35	mV	When brake is applied
Output saturation voltage H	V_{OLH}	–	0.32	0.48	V	I_O=500mA
Output saturation voltage L	V_{OLL}	–	0.18	0.27	V	I_O=500mA
Voltage gain	G_{VLD}	4.0	6.0	8.0	dB	LDCONT=1V
Difference between positive and nagative voltage gains	ΔG_{VLD}	–2.0	0	2.0	dB	
〈 Regulator 1〉						
Output voltage	V_{REG1}	3.135	3.300	3.465	V	
Output load stability	ΔV_{RL1}	5	10	20	mV	I_O=0~200mA
Supply voltage stability	ΔVV_{CC1}	5	10	20	mV	V_{CC}=6~10V I_O=100mA
REG1_B terminal sink current	I_{REGSI1}	2	–	–	mA	
〈 Regulator 2〉						
Output voltage	V_{REG2}	4.75	5.00	5.25	V	
Output load stability	ΔV_{RL2}	5	10	20	mV	I_O=0~200mA
Supply voltage stability	ΔVV_{CC2}	5	10	20	mV	V_{CC}=7~10V I_O=100mA
RE2_B terminal sink current	I_{REGSI2}	2	–	–	mA	

◎ The product is not designed for protection against radioactive rays.

●Measurement circuits

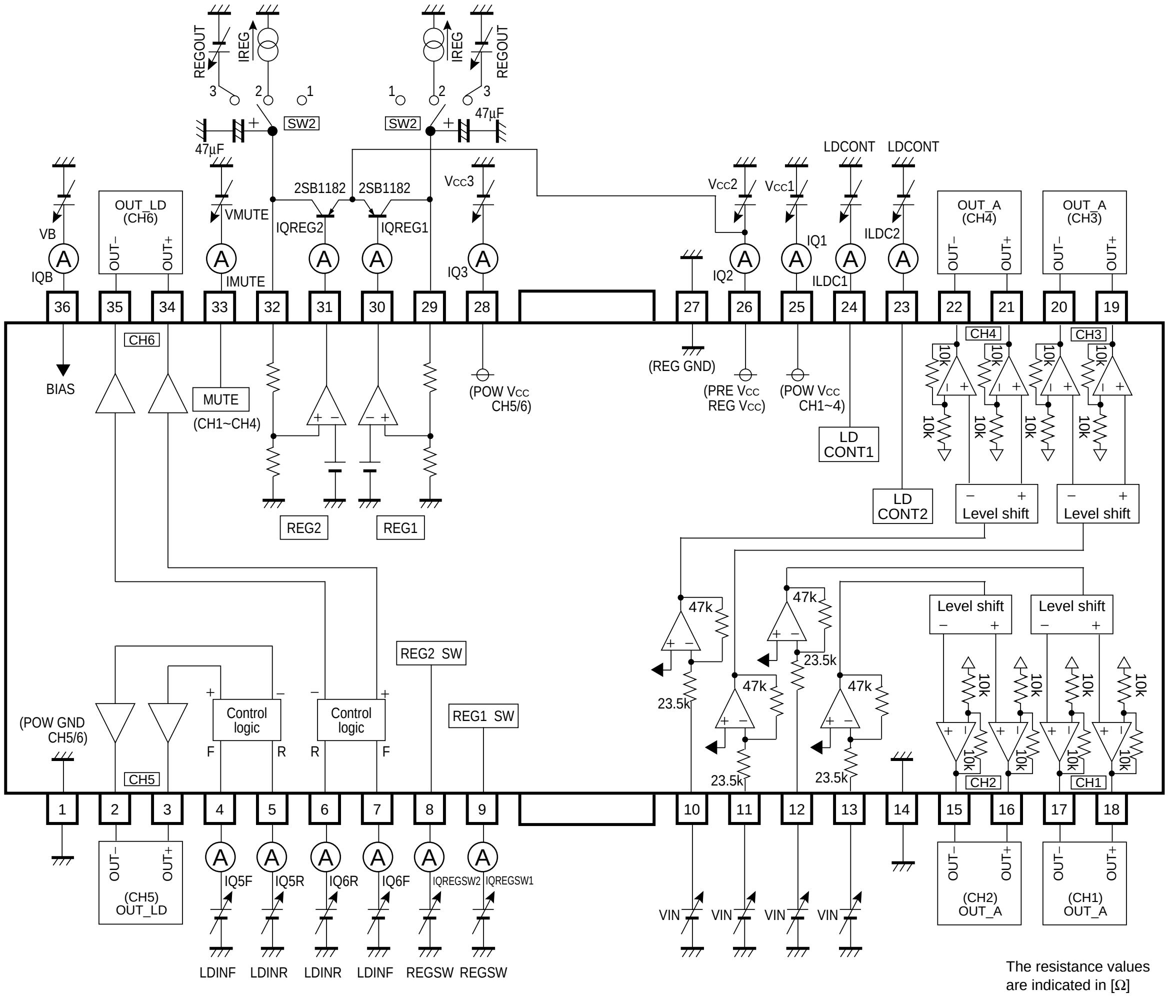


Fig.1

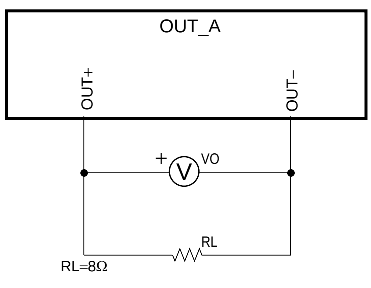


Fig.2

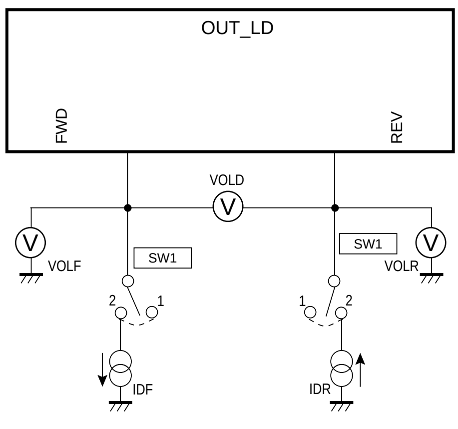


Fig.3

●Switch table for measuring circuit diagrams

(unless otherwise noted, Ta=25°C, $V_{CC}1$, $V_{CC}2$, $V_{CC}3$=8V, BIAS=2.5V, R_L=8Ω Unless otherwise specified, the switch 1 is used.)

Parameter	Symbol	SWITCH 1	SWITCH 2	Conditions	Measurement circuit
Quiescent current	$I_{CC}1$			*1	Fig.1
Quiescent current (BTL MUTE)	$I_{CC}2$			*2	Fig.1
〈 BTLdriver CH1 to CH4 〉					
Output offset voltage	V_{OFS}			V_{IN}=VB, VOFS=VO	Fig.2
Max. output amplitude	V_{OM}			V_{IN}=V_{CC}, VOM=VO	Fig.2
Closed circuit voltage gain(CH1 to CH4)	G_{VC}			V_{IN}=VB±0.5V, GVC=20log (VO/0.5)	Fig.2
Difference between positive and negative voltage gains (CH1 to CH4)	ΔG_{VC}				Fig.2
Mute terminal sink current	I_{MUTE}			VMUTE=5V, IMUTE=IMUTE	Fig.1
Bias terminal sink current	I_{BIAS}			VB=2.5V, IBIAS=IQB	Fig.1
〈 Loading driver CH5 and CH6 〉					
Output offset voltage	V_{OFSL}			LDINF=LDINR=5V, VOFSL=VOLD	Fig.3
Output saturation voltage H	V_{OLH}	2		*3	Fig.3
Output saturation voltage L	V_{OLL}	2		LDINF=5V, LDINR=0V, IDR=500mA, VOLL=VOLR	Fig.3
Voltage gain (Loading)	G_{VLD}			*4	Fig.1
Difference between positive and negative voltage gains (Loading)	ΔG_{VLD}				Fig.1
Input terminal sink current	I_{INL}			LDINF=LDINR=5V, IINL=IQ5F, IQ5R, IQ6F, IQ6R	Fig.1
LDCONT terminal source current	I_{LDC}			LDCONT=5V, ILDC=ILDC	Fig.1
〈 Regulator 1 〉					
Output voltage	V_{REG1}				Fig.1
Output load stability	ΔV_{RL1}		2	IREG=0~200mA	Fig.1
Supply voltage stability	ΔVV_{CC1}		2	V_{CC}=6~10V, IREG=100mA	Fig.1
REG1_B terminal sink current	I_{REGSI1}		3	REGOUT=2.5V, IREGSI1=IQREGSW1	Fig.1
REG1SW terminal sink current	I_{REG1}			REGSW=5V, IREGSI1=IQREGSW1	Fig.1
〈 Regulator 2 〉					
Output voltage	V_{REG2}				Fig.1
Output load stability	ΔV_{RL2}		2	IREG=0~200mA	Fig.1
Supply voltage stability	ΔVV_{CC2}		2	V_{CC}=7~10V, IREG=100mA	Fig.1
REG2_B terminal sink current	I_{REGSI2}		3	REGOUT=4V, IREGSI2=IQREGSW2	Fig.1
REG2SW terminal sink current	I_{REG2}			REGSW=5V, IREGSI2=IQREGSW2	Fig.1

*1 LDINF=LDINR=0V, REGSW=0V, VMUTE=5V, $I_{CC}1$=IQ1+IQ2+IQ3
*2 LDINF=LDINR=0V, REGSW=0V, VMUTE=0V, $I_{CC}2$=IQ1+IQ2+IQ3
*3 LDINF=5V, LDINR=0V, IDF=500mA, VOLH=V_{CC}-VOLF
*4 LDINF=5V, LDINR=0V, LDCONT=1V, GVLD=20log (VOLD/LDCONT)

●**Application example**

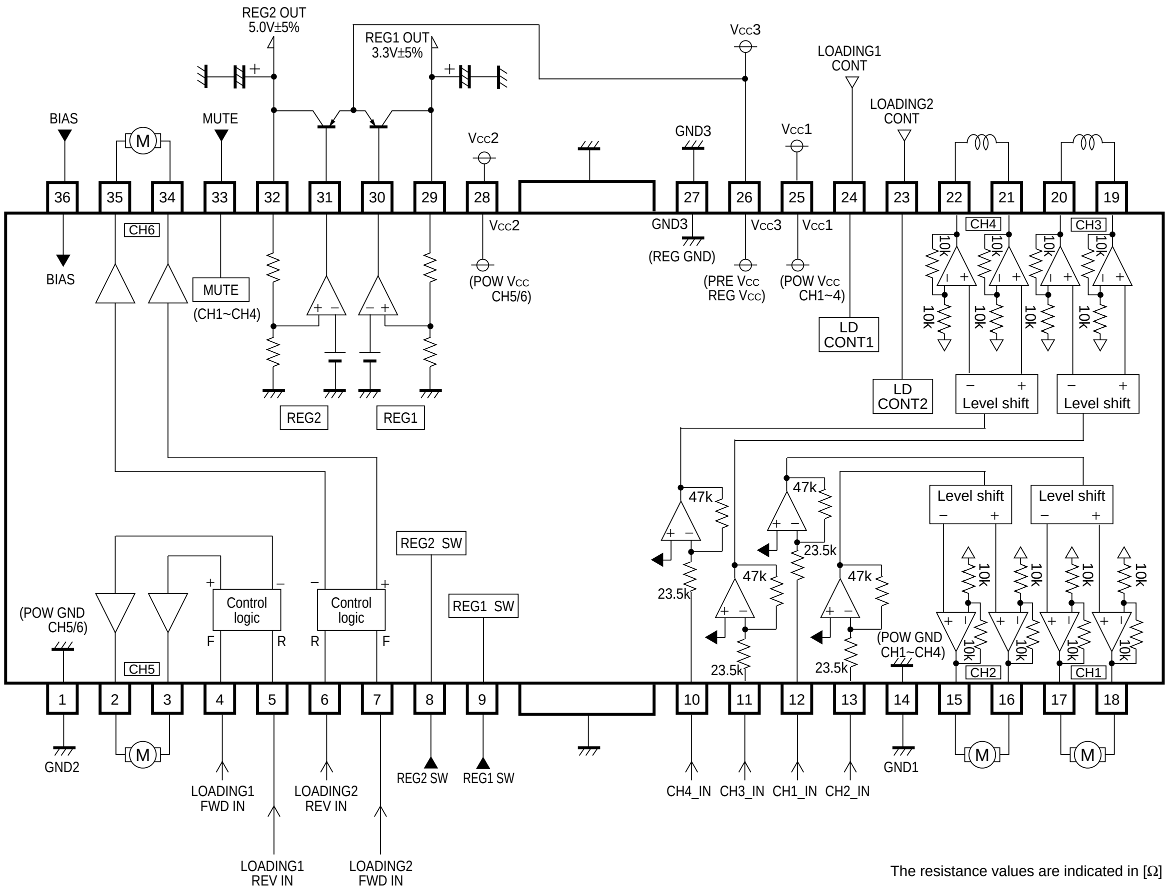


Fig.4

●**Operation notes**

(1) BD7961FM has a built-in thermal shutdown circuit.
When the chip temperature reaches 175°C (Typ.), the output current from all drivers is muted.
When the chip temperature returns to 150°C (Typ.), the circuit of the driver unit starts up.

(2) When the mute terminal (pin33) is opened or the terminal voltage is reduced to 0.5V or less, the output current of the BTL driver unit is muted.
In the normal state of use, pull up the voltage to 2.0V or more.

(3) When the voltage of the regulator switch terminals (pin8 and 9) is increased to 2.0V or more, the output from the regulator is muted. In the normal state of use, pull down the voltage to 0.5V or less.

(4) When the bias terminal (pin36) voltage is reduced to 0.7V or less, the BTL driver unit is muted.
In the normal state of use, set the voltage to 1.1V or more.

(5) Thermal shutdown mutes all drivers. When the mute ON voltage and the bias terminal voltage are reduced, only the BTL drivers are muted. When the drivers are muted, the BTL driver output terminal voltage becomes the internal bias voltage ($V_{CC}1-0.7$)/2V.

(6) The loading drivers operate according to the following logic.

INPUT		OUTPUT		Function
FWD	REV	OUT+	OUT−	
L	L	Hi Z	Hi Z	High impedance
L	H	L	H	REV mode
H	L	H	L	FWD mode
H	H	L	L	Brake mode

The output voltage can be changed by adjusting the voltage input to the LDCONT terminal (gain of 6dB Typ.). However, even if the input voltage is increased excessively, the output voltage will not exceed the max. output voltage that depends on the supply voltage.

(7) Supply the same voltage to $V_{CC}1$ (pin25), $V_{CC}2$ (pin28) and $V_{CC}3$ (pin26).
Insert by the pass capacitor (approx. 0.1µF) between V_{CC} pin and GND pin of IC as near as possible.

(8) Connect the radiating fin with external GND.

(9) Output pin is to avoid short-circuit with V_{CC}, GND and other output pins.
An integrated circuit is damaged, and smoke may come out by the case.

●Electrical characteristic curves

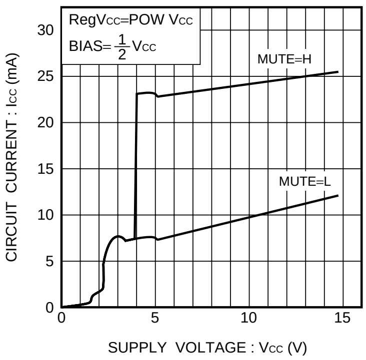


Fig.5 Circuit current characteristic

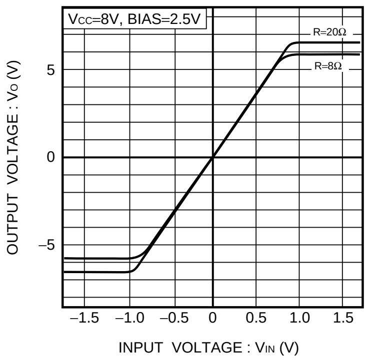


Fig.6 Input-output characteristic

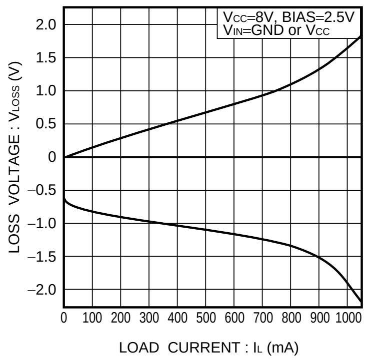


Fig.7 Output load current regulation

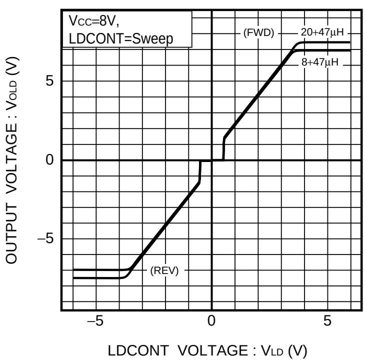


Fig.8 Input-output characteristic

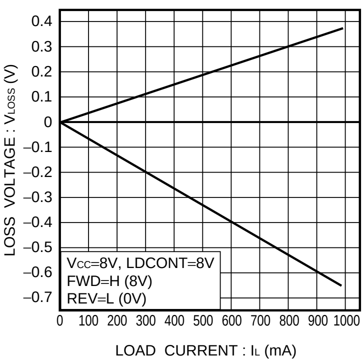


Fig.9 Output load current regulation

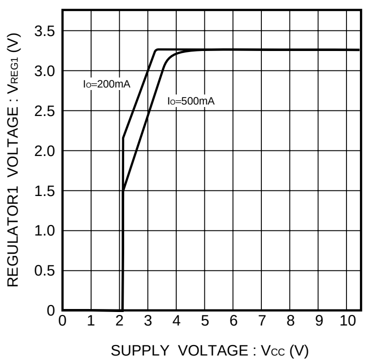


Fig.10 Reg1 power supply characteristic

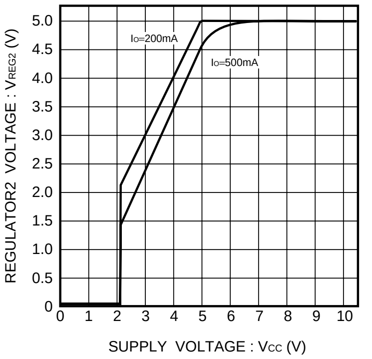


Fig.11 Reg2 power supply characteristic

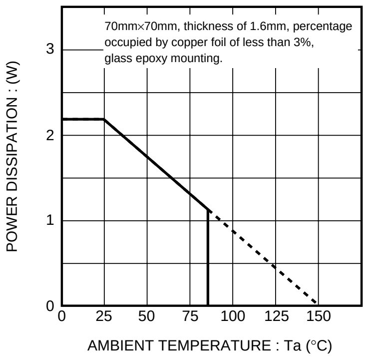
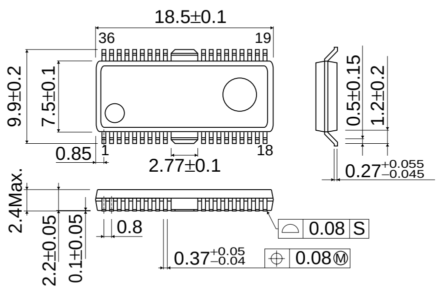


Fig.12 Power dissipation

●**External dimensions** (Units : mm)



HSOP-M36

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