MOTOROLA

MC54/74F353

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The MC54/74F353 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common Select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus-oriented systems.

- Inverted Version of F253
- Multifunction Capability
- Separate Enables for Each Multiplexer

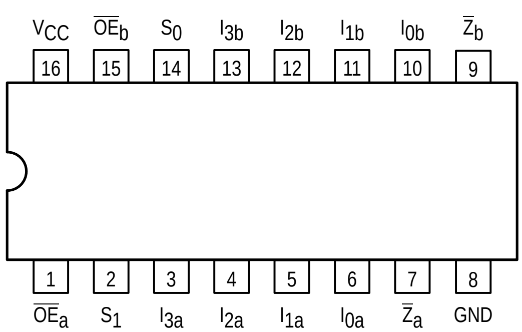
FUNCTIONAL DESCRIPTION

The MC54/74F353 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1).The 4-input multiplexers have individual Output enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (high Z) state. The logic equations for the outputs are shown below:

$$\overline{Z}_a=\overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$
$$\overline{Z}_b=\overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_1 b \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

CONNECTION DIAGRAM (TOP VIEW)



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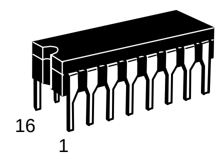
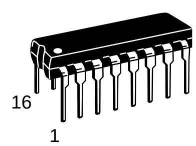
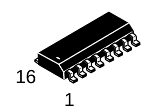


J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

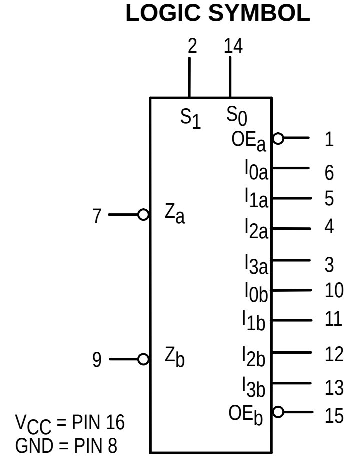


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

LOGIC SYMBOL

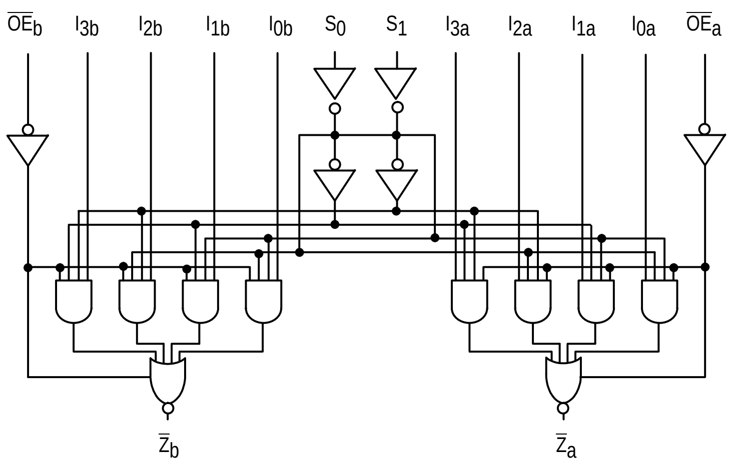


FUNCTION TABLE

Select Inputs		Data Inputs				Output Enable	Output
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	$\overline{Z}$
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs S_0 and S_1 are common to both sections.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High Impedance

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	–55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			–3.0	mA
I_{OL}	Output Current — Low	54, 74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				–1.2	V	I_{IN} = –18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.3		V	I_{OH} = –3.0 mA	V_{CC} = 4.5 V
		74	2.7	3.3		V	I_{OH} = –3.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
I_{OZH}	Output OFF Current — HIGH				50	μA	V_{OUT} = 2.7 V	V_{CC} = MAX
I_{OZL}	Output OFF Current — LOW				–50	μA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					100		V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				–0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		–60		–150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CCH}	Power Supply Current			9.3	14	mA	I_n, S_n, $\overline{OE}_n$ = GND	V_{CC} = MAX
I_{CCL}				13.3	20		I_n, S_n = GND	
I_{CCZ}				15	23		$\overline{OE}_n$ = 4.5 V	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		54F T_A = - 55°C to + 125°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		74F T_A = 0°C to + 70°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		Unit
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	3.5 3.0	11 8.5	3.0 2.5	14 11	3.0 2.5	12.5 9.5	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	2.5 1.0	7.0 3.5	2.0 1.0	9.0 5.0	2.0 1.0	8.0 4.0	ns
t_{PZH} t_{PZL}	Output Enable Time	3.0 3.5	8.0 8.0	3.0 3.0	10.5 10.5	3.0 3.0	9.0 9.0	
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	5.0 6.0	2.0 1.5	7.0 8.0	1.5 1.5	6.0 7.0	ns