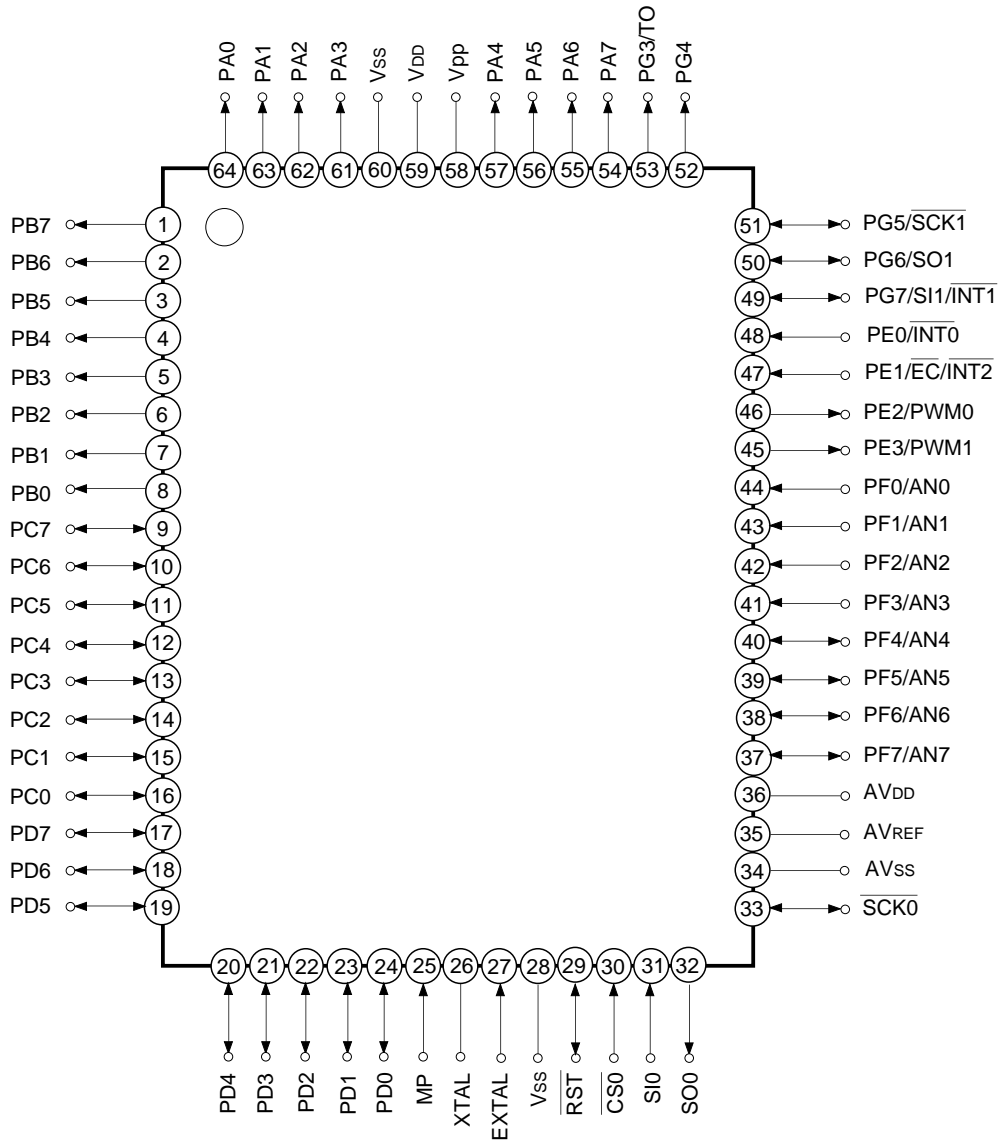


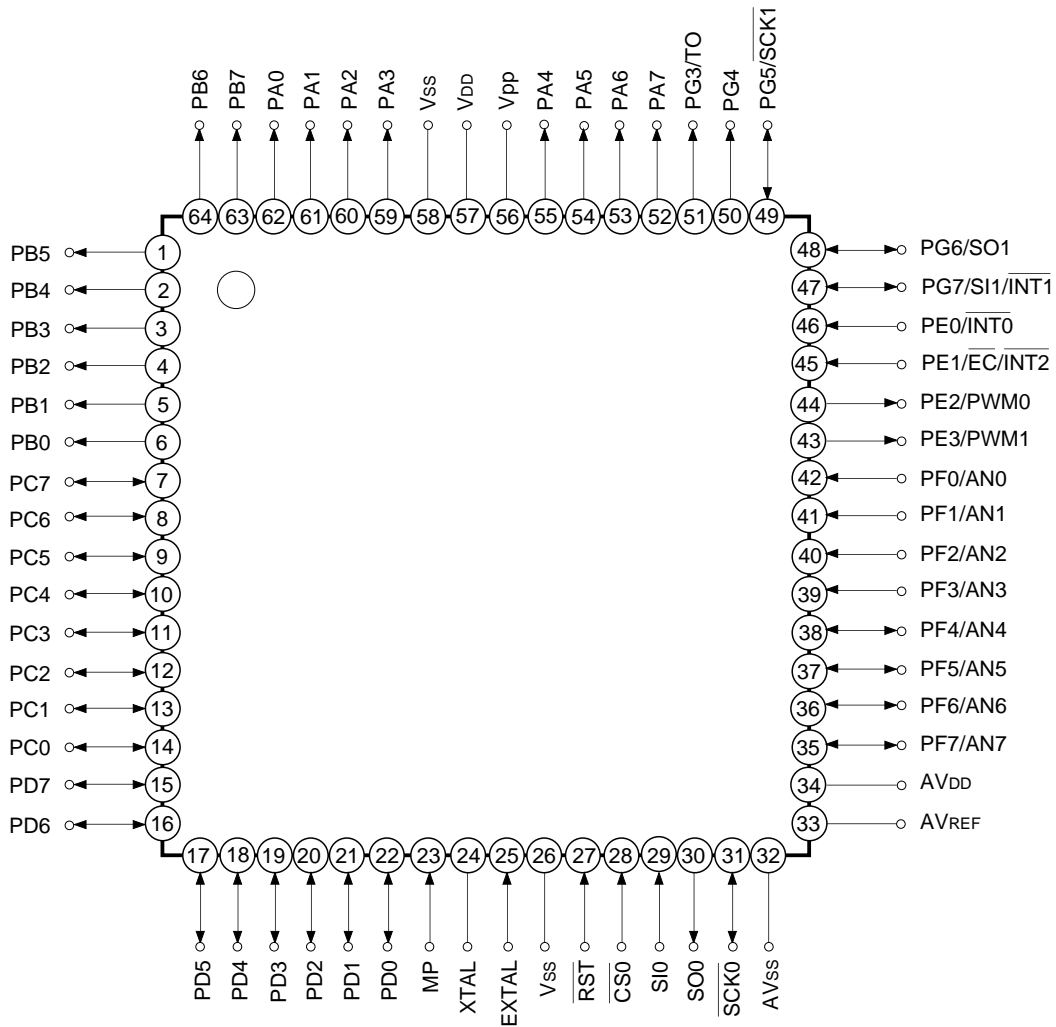
Block Diagram

Pin Configuration (Top View) 64-pin QFP



- Note)**
1. Vpp (Pin 58) is always connected to VDD.
 2. Vss (Pins 28 and 60) are both connected to GND.
 3. MP (Pin 25) is always connected to GND.

Pin Configuration (Top View) 64-pin LQFP



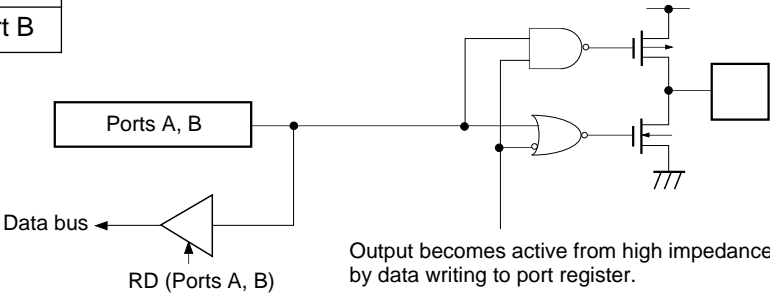
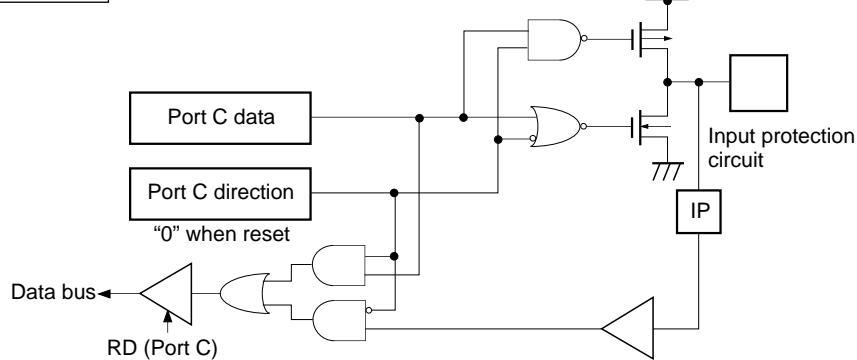
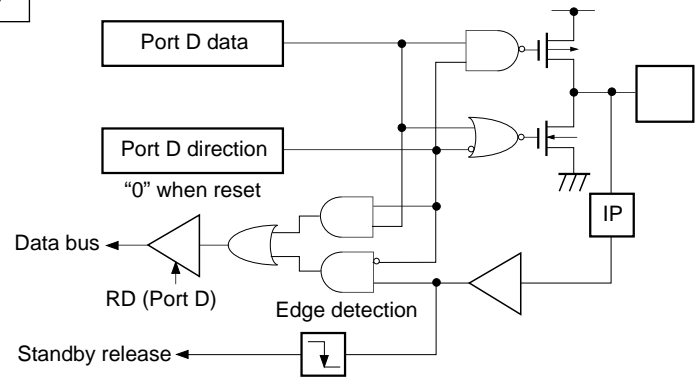
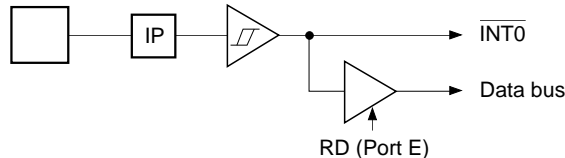
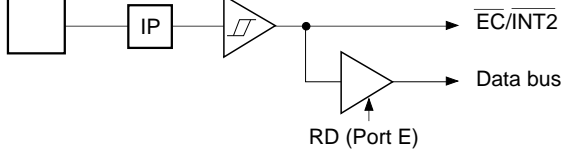
- Note)**
1. V_{PP} (Pin 56) is always connected to V_{DD}.
 2. V_{SS} (Pins 26 and 58) are both connected to GND.
 3. MP (Pin 23) is always connected to GND.

Pin Description

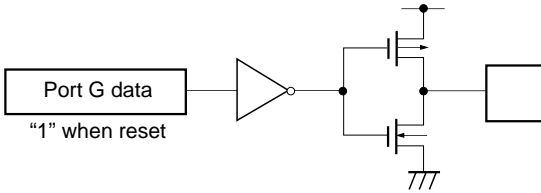
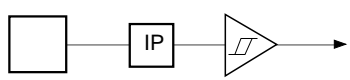
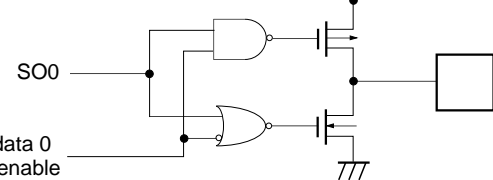
Symbol	I/O	Description	
PA0 to PA7	Output	(Port A) 8-bit output port. (8 pins)	
PB0 to PB7	Output	(Port B) 8-bit output port. (8 pins)	
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O and function as standby release input can be set in a unit of single bits. (8 pins)	
PE0/ $\overline{\text{INT0}}$	Input/Input	(Port E) 4-bit port. Lower 2 bits are for input; upper 2 bits are for output. (4 pins)	Input to request external interruption. Active at the falling edge. (2 pins)
PE1/ $\overline{\text{EC}}$ / $\overline{\text{INT2}}$	Input/Input/ Input		External event input for timer/counter.
PE2/PWM0	Output/Output		12-bit PWM output. (2 pins)
PE3/PWM1	Output/Output		
PF0/AN0 to PF3/AN3	Input/Input	(Port F) 8-bit port. Lower 4 bits are for input; upper 4 bits are for output. Lower 4 bits also serve as standby release input. (8 pins)	Analog input to A/D converter. (8 pins)
PF4/AN4 to PF7/AN7	Output/Input		
$\overline{\text{SCK0}}$	I/O	Serial clock (CH0) I/O.	
SO0	Output	Serial data (CH0) output.	
SI0	Input	Serial data (CH0) input.	
$\overline{\text{CS0}}$	Input	Serial interface (CH0) chip select input.	
PG3/TO	Output/Output	(Port G) 5-bit port. Lower 2 bits are for output; upper 3 bits are for I/O. I/O port can be set in a unit of single bits. (5 pins)	Timer/counter rectangular wave output.
PG4	Output		
PG5/ $\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O.
PG6/SO1	I/O/Output		Serial data (CH1) output.
PG7/SI1/ $\overline{\text{INT1}}$	I/O/Input/ Input		Serial data (CH1) input.
EXTAL	Input	Connects a crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
$\overline{\text{RST}}$	I/O	System reset; active at Low level. $\overline{\text{RST}}$ pin is I/O pin, which outputs Low level by incorporated power-on reset function when power turns on.	

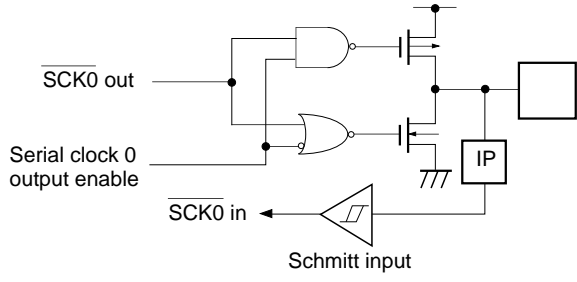
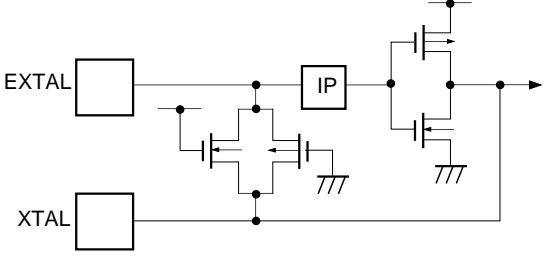
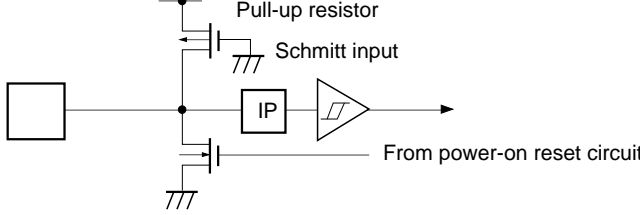
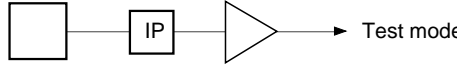
Symbol	I/O	Description
V _{pp}		Power supply for built-in PROM writing. Connect to V _{DD} for normal operation.
MP	Input	Test mode pin. Always connect to GND.
AV _{DD}		Positive power supply of A/D converter.
AV _{REF}	Input	Reference voltage input of A/D converter.
AV _{SS}		GND of A/D converter.
V _{DD}		Positive power supply.
V _{SS}		GND. Connect both V _{SS} pins to GND.

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
Port A Port B PA0 to PA7 PB0 to PB7 16 pins	 <p>Output becomes active from high impedance by data writing to port register.</p>	Hi-Z
Port C PC0 to PC7 8 pins	 <p>Port C direction "0" when reset</p>	Hi-Z
Port D PD0 to PD7 8 pins	 <p>Port D direction "0" when reset</p> <p>Edge detection</p> <p>Standby release</p>	Hi-Z
Port E PE0/ $\overline{\text{INT0}}$ 1 pin	 <p>Schmitt input</p> <p>RD (Port E)</p>	Hi-Z
Port E PE1/ $\overline{\text{EC}}$ / $\overline{\text{INT2}}$ 1 pin	 <p>Schmitt input</p> <p>RD (Port E)</p>	Hi-Z

Pin	Circuit format	When reset
<p>PE2/PWM0 PE3/PWM1</p> <p>2 pins</p>	<p>Port E</p>	<p>Hi-Z</p>
<p>PF0/AN0 to PF3/AN3</p> <p>4 pins</p>	<p>Port F</p>	<p>Hi-Z</p>
<p>PF4/AN4 to PF7/AN7</p> <p>4 pins</p>	<p>Port F</p>	<p>Hi-Z</p>
<p>PG3/TO</p> <p>1 pin</p>	<p>Port G</p>	<p>High level</p>

Pin	Circuit format	When reset
PG4 1 pin	Port G 	High level
PG5/SCK1 PG6/SO1 2 pins	Port G Port G function selection "0" when reset SCK1 out, SO1 Serial clock 1/data 1 output enable Port G data Port G direction "0" when reset Data bus ← RD (Port G) SCK1 in *1 PG6 is not schmitt input	Hi-Z
PG7/SI1/INT1 1 pin	Port G Port G data Port G direction "0" when reset Data bus ← RD (Port G) INT1 SI1 Schmitt input	Hi-Z
CS0 SI0 2 pins	Schmitt input 	Hi-Z
SO0 1 pin	SO0 Serial data 0 output enable 	Hi-Z

Pin	Circuit format	When reset
<p>$\overline{\text{SCK0}}$</p> <p>1 pin</p>		<p>Hi-Z</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during stop. XTAL becomes High level. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>		<p>Low level</p>
<p>MP</p> <p>1 pin</p>		<p>Hi-Z</p>

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	V _{pp}	-0.3 to +13.0	V	Incorporated PROM
	AV _{DD}	AV _{SS} to +7.0	V	
	AV _{SS}	-0.3 to +0.3	V	
	AV _{REF}	AV _{SS} to +7.0	V	
Input voltage	V _{IN}	-0.3 to +7.0*1	V	
Output voltage	V _{OUT}	-0.3 to +7.0*1	V	
High level output current	I _{OH}	-5	mA	
High level total output current	∑I _{OH}	-50	mA	Total of output pins
Low level output current	I _{OL}	15	mA	
Low level total output current	∑I _{OL}	130	mA	Total of output pins
Operating temperature	T _{opr}	-10 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP-64P-L01
		380	mW	LQFP-64P-L01

*1 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V. (CS0 and SI0 excluded.)

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	3.0	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing mode
		2.7	5.5	V	Guaranteed operation range for 1/16 frequency dividing mode
		2.5	5.5	V	Guaranteed data hold range during stop mode
	V _{pp}	V _{pp} = V _{DD}		V	*8
Analog voltage	AV _{DD}	3.0	5.5	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS Schmitt input*3
			5.5	V	CMOS Schmitt input*4
V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL pin*5	
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2, *7
			0.2V _{DD}	V	*2, *6
	V _{ILS}	0	0.2V _{DD}	V	CMOS Schmitt input*3, *4
	V _{ILEX}	-0.3	0.4	V	EXTAL pin*5
Operating temperature	T _{opr}	-10	+75	°C	

*1 AV_{DD} should be the same voltage as V_{DD}.

*2 Normal input port (PC, PD, PF0 to PF3, and PG6 pins), MP pin.

*3 $\overline{\text{SCK0}}$, $\overline{\text{RST}}$, $\overline{\text{INT0}}$, $\overline{\text{EC/INT2}}$, $\overline{\text{SCK1}}$ and $\overline{\text{SI1/INT1}}$ pins

*4 CS0 and SI0 pins

*5 Specified only when the external clock is input.

*6 In case of 3.0 to 3.6V supply voltage (V_{DD}).

*7 In case of 4.5 to 5.5V supply voltage (V_{DD}).

*8 V_{pp} and V_{DD} should be set to the same voltage.

DC Characteristics

Supply voltage ($V_{DD} = 4.5$ to $5.5V$)(Ta = -10 to $+75^{\circ}C$, $V_{SS} = 0V$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PE, PF4 to PF7, SO, SCK, RST	$V_{DD} = 4.5V, I_{OH} = -0.5mA$	4.0			V
			$V_{DD} = 4.5V, I_{OH} = -1.2mA$	3.5			V
Low level output voltage	V_{OL}	(V _{OL} only) PG3 to PG7	$V_{DD} = 4.5V, I_{OL} = 1.8mA$			0.4	V
			$V_{DD} = 4.5V, I_{OL} = 3.6mA$			0.6	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 5.5V, V_{IH} = 5.5V$	0.5		40	μA
	I_{ILE}		$V_{DD} = 5.5V, V_{IL} = 0.4V$	-0.5		-40	μA
	I_{ILR}	\overline{RST}	$V_{DD} = 5.5V, V_{IL} = 0.4V$	-1.5		-400	μA
I/O leakage current	I_{IZ}	PA to PG, MP, \overline{CS} , SI, SO, \overline{SCK} , \overline{RST}	$V_{DD} = 5.5V,$ $V_I = 0, 5.5V$			± 10	μA
Supply current*1	I_{DD1}	V_{DD}	1/2 frequency dividing mode $V_{DD} = 5 \pm 0.5V,$ 16MHz crystal oscillation ($C_1 = C_2 = 15pF$)		20	40	mA
	I_{DDS1}		Sleep mode $V_{DD} = 5 \pm 0.5V,$ 16MHz crystal oscillation ($C_1 = C_2 = 15pF$)		1	5	mA
	I_{DDS3}		Stop mode $V_{DD} = 5.5V,$ termination of 16MHz oscillation				30
Input capacity	C_{IN}	PC, PD, PE0, PE1, PF, PG5 to PG7, \overline{RST} , $\overline{CS0}$, SI0, $\overline{SCK0}$, EXTAL	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 When all output pins are open.

DC Characteristics

Supply voltage ($V_{DD} = 3.0$ to $3.6V$)

(Ta = -10 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PE, PF4 to PF7, SO, SCK, RST	$V_{DD} = 3.0V, I_{OH} = -0.15mA$	2.7			V
			$V_{DD} = 3.0V, I_{OH} = -0.5mA$	2.3			V
Low level output voltage	V_{OL}	(V _{OL} only) PG3 to PG7	$V_{DD} = 3.0V, I_{OL} = 1.2mA$			0.3	V
			$V_{DD} = 3.0V, I_{OL} = 1.6mA$			0.5	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 3.6V, V_{IH} = 3.6V$	0.3		20	μA
	I_{ILE}		$V_{DD} = 3.6V, V_{IL} = 0.3V$	-0.3		-20	μA
	I_{ILR}	RST	$V_{DD} = 3.6V, V_{IL} = 0.3V$	-0.9		-200	μA
I/O leakage current	I_{IZ}	PA to PG, MP, CS, SI, SO, SCK, RST	$V_{DD} = 3.6V, V_I = 0, 3.6V$			± 10	μA
Supply current*1	I_{DD2}	V_{DD}	1/2 frequency dividing mode $V_{DD} = 3.3 \pm 0.3V, 12MHz$ crystal oscillation (C ₁ = C ₂ = 15pF)		10	20	mA
	I_{DDS2}		Sleep mode $V_{DD} = 3.3 \pm 0.3V, 12MHz$ crystal oscillation (C ₁ = C ₂ = 15pF)		0.5	2.5	mA
	I_{DDS3}		Stop mode $V_{DD} = 5.5V, termination of 12MHz$ oscillation			30	μA
Input capacity	C_{IN}	PC, PD, PE0, PE1, PF, PG5 to PG7, RST, CS0, SI0, SCK0, EXTAL	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 When all output pins are open.

AC Characteristics

(1) Clock timing

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit	
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	$V_{DD} = 4.5$ to 5.5V	1	16	MHz
					1	12	
System clock input pulse width	t_{XL} , t_{XH}	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)	$V_{DD} = 4.5$ to 5.5V	28		ns
					37.5		
System clock input rise and fall times	t_{CR} , t_{CF}	EXTAL	Fig. 1, Fig. 2 (External clock drive)		200	ns	
Event count input clock pulse width	t_{EL} , t_{EH}	\overline{EC}	Fig. 3	$4t_{sys}^{*1}$		ns	
Event count input clock rise and fall times	t_{ER} , t_{EF}	\overline{EC}	Fig. 3		20	ms	

*1 t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).

$$t_{sys} [\text{ns}] = 2000/fc \text{ (Upper 2 bits = "00")}, 4000/fc \text{ (Upper 2 bits = "01")}, 16000/fc \text{ (Upper 2 bits = "11")}$$

Fig. 1. Clock timing

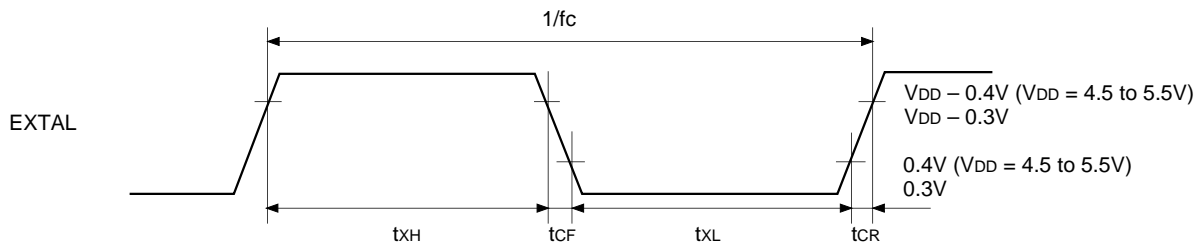


Fig. 2. Clock applied condition

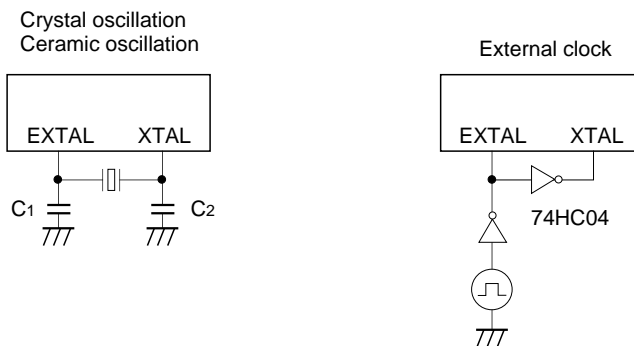
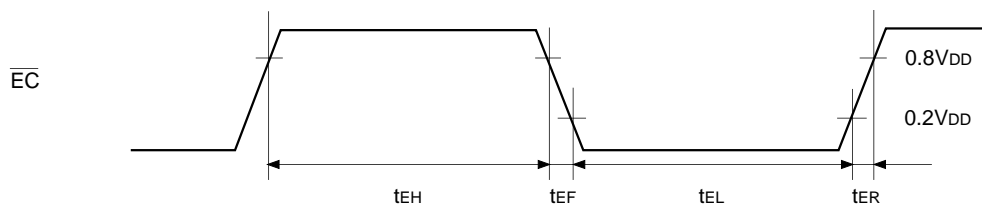


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS}} \downarrow \rightarrow \overline{\text{SCK}}$ delay time	t _{DCSK}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK}}$ = output mode)		t _{sys} + 200	ns
$\overline{\text{CS}} \uparrow \rightarrow \overline{\text{SCK}}$ floating delay time	t _{DCSKF}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK}}$ = output mode)		t _{sys} + 200	ns
$\overline{\text{CS}} \downarrow \rightarrow \text{SO}$ delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{\text{CS}} \downarrow \rightarrow \text{SO}$ floating delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{\text{CS}}$ high level width	t _{WHCS}	$\overline{\text{CS0}}$	Chip select transfer mode	t _{sys} + 200		ns
$\overline{\text{SCK}}$ cycle time	t _{KCY}	$\overline{\text{SCK0}}$	Input mode	2t _{sys} + 200		ns
			Output mode	8000/fc		ns
$\overline{\text{SCK}}$ high and low level widths	t _{KH} t _{KL}	$\overline{\text{SCK0}}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 100		ns
SI input setup time (for $\overline{\text{SCK}} \uparrow$)	t _{SIK}	SI0	$\overline{\text{SCK}}$ input mode	-t _{sys} + 100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI input hold time (for $\overline{\text{SCK}} \uparrow$)	t _{KSI}	SI0	$\overline{\text{SCK}}$ input mode	2t _{sys} + 100		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	t _{KSO}	SO0	$\overline{\text{SCK}}$ input mode		2t _{sys} + 200	ns
			$\overline{\text{SCK}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FE_H) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) $\overline{\text{CS}}$, $\overline{\text{SCK}}$, SI and SO represents $\overline{\text{CS0}}$, $\overline{\text{SCK0}}$, SI0, and SO0, respectively.

Note 3) The load of $\overline{\text{SCK}}$ output mode and SO output delay time is 50pF + 1TTL.

Serial transfer (CH0)

(Ta = -10 to +75°C, V_{DD} = 3.0 to 3.6V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS}} \downarrow \rightarrow \overline{\text{SCK}}$ delay time	t _{DCSK}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK}}$ = output mode)		t _{sys} + 250	ns
$\overline{\text{CS}} \uparrow \rightarrow \overline{\text{SCK}}$ floating delay time	t _{DCSKF}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK}}$ = output mode)		t _{sys} + 200	ns
$\overline{\text{CS}} \downarrow \rightarrow \text{SO}$ delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} + 250	ns
$\overline{\text{CS}} \downarrow \rightarrow \text{SO}$ floating delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{\text{CS}}$ high level width	t _{WHCS}	$\overline{\text{CS0}}$	Chip select transfer mode	t _{sys} + 200		ns
$\overline{\text{SCK}}$ cycle time	t _{KCY}	$\overline{\text{SCK0}}$	Input mode	2t _{sys} + 200		ns
			Output mode	8000/fc		ns
$\overline{\text{SCK}}$ high and low level widths	t _{KH} t _{KL}	$\overline{\text{SCK0}}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 150		ns
SI input setup time (for $\overline{\text{SCK}} \uparrow$)	t _{SIK}	SI0	$\overline{\text{SCK}}$ input mode	-t _{sys} + 100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI input hold time (for $\overline{\text{SCK}} \uparrow$)	t _{KSI}	SI0	$\overline{\text{SCK}}$ input mode	2t _{sys} + 100		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	t _{KSO}	SO0	$\overline{\text{SCK}}$ input mode		2t _{sys} + 250	ns
			$\overline{\text{SCK}}$ output mode		125	ns

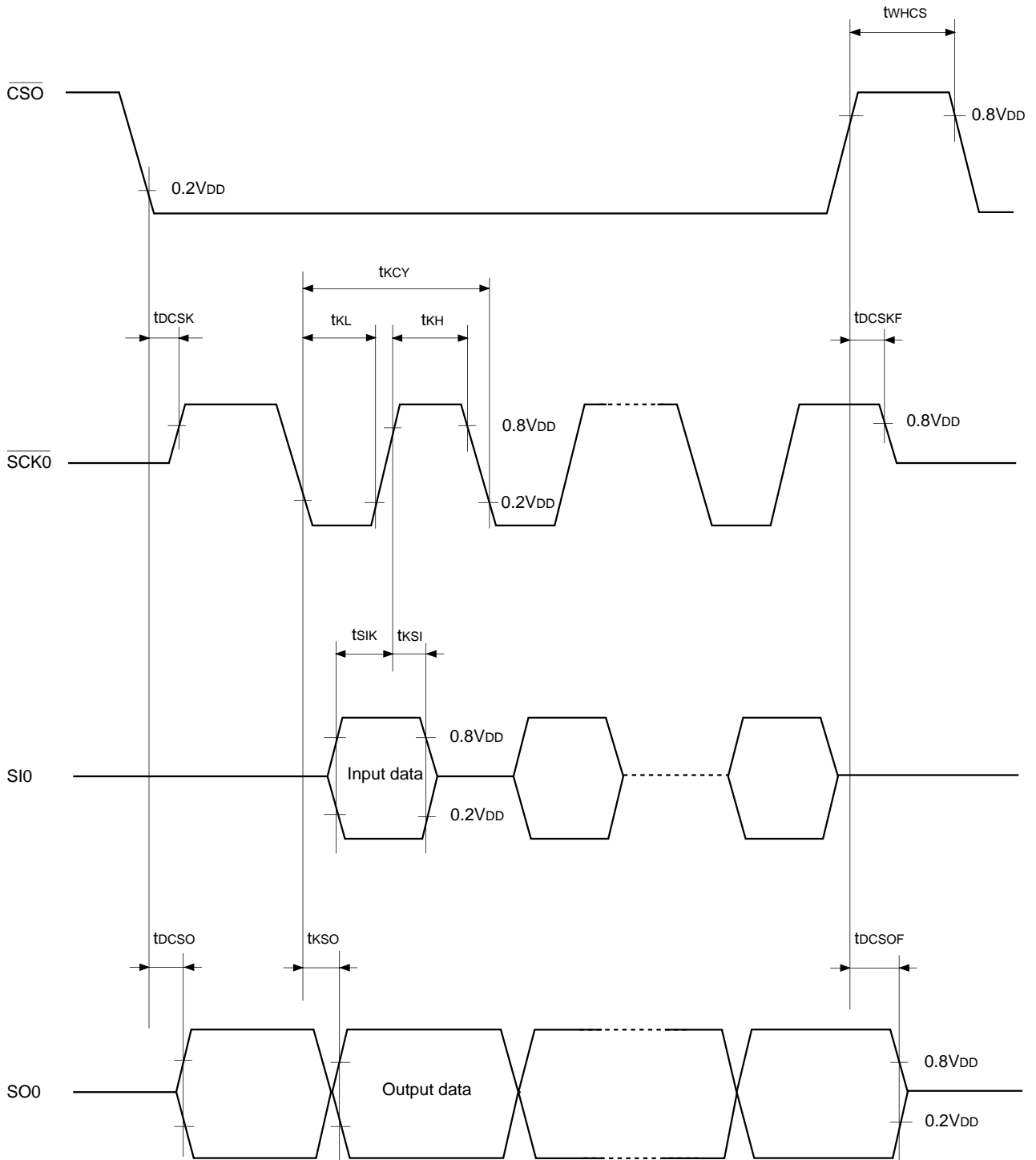
Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FE_H) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) $\overline{\text{CS}}$, $\overline{\text{SCK}}$, SI and SO represents $\overline{\text{CS0}}$, $\overline{\text{SCK0}}$, SI0, and SO0, respectively.

Note 3) The load of $\overline{\text{SCK}}$ output mode and SO output delay time is 50pF.

Fig. 4. Serial transfer timing (CH0)



Serial transfer (CH1) (SIO mode)(Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t _{KCY}	SCK1	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK1}}$ high and low level widths	t _{KH} t _{KL}	SCK1	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 50		ns
SI1 input setup time (for $\overline{\text{SCK1}}$ ↑)	t _{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}}$ ↑)	t _{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	t _{sys} + 200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
SCK1 ↓ → SO1 delay time	t _{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		t _{sys} + 200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF + 1TTL.

Serial transfer (CH1) (SIO mode)(Ta = -10 to +75°C, V_{DD} = 3.0 to 3.6V, V_{SS} = 0V reference)

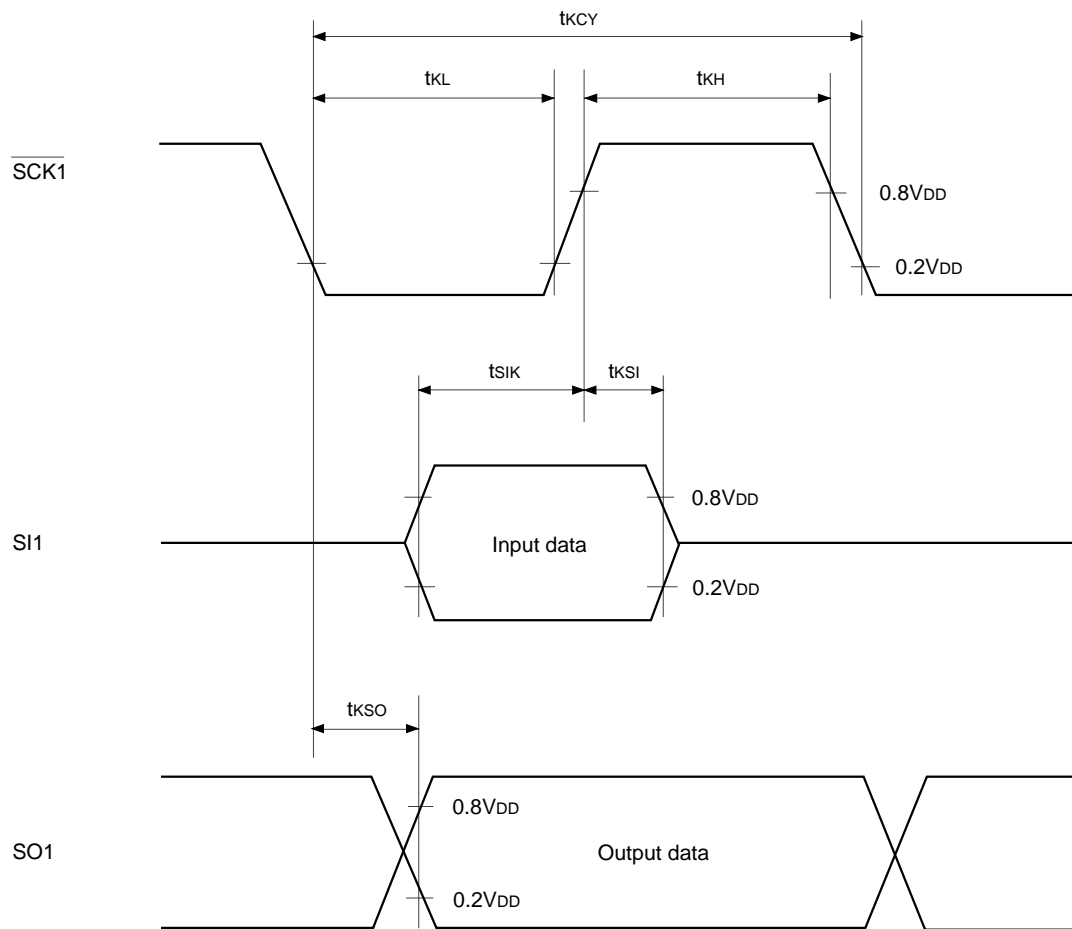
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t _{KCY}	SCK1	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK1}}$ high and low level widths	t _{KH} t _{KL}	SCK1	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 150		ns
SI1 input setup time (for $\overline{\text{SCK1}}$ ↑)	t _{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}}$ ↑)	t _{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	t _{sys} + 200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
SCK1 ↓ → SO1 delay time	t _{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		t _{sys} + 250	ns
			$\overline{\text{SCK1}}$ output mode		125	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF.

Fig. 5. Serial transfer CH1 timing (SIO mode)



Serial transfer (CH1) (Special mode) ($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	t_{LCY}	SO1 SI1	*1		104		μs
SI1 data setup time	t_{LSU}	SI1		2			μs
SI1 data hold time	t_{LHD}	SI1		2			μs

*1 t_{LCY} is specified only when serial mode register (CH1) (SIOM1: 01FAH) lower 2 bits (SO1 clock selection) is set at $104\mu\text{s}$ according to the system clock frequency.

Note) The load of SO1 pin is $50\text{pF} + 1\text{TTL}$.

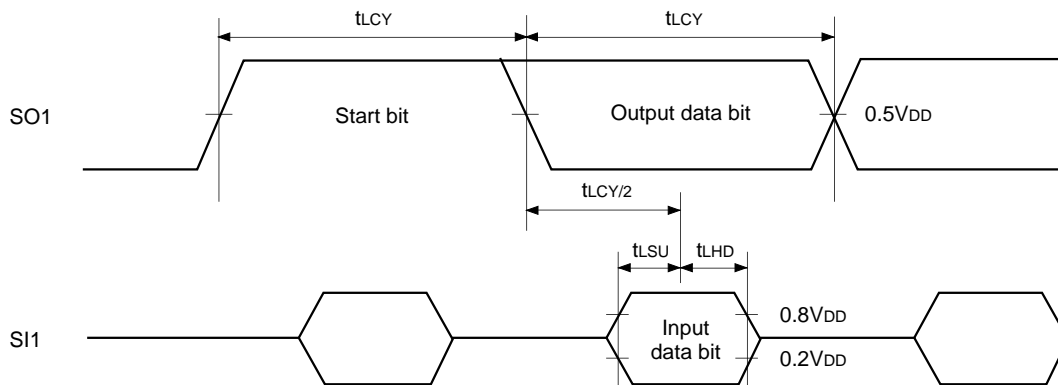
Serial transfer (CH1) (Special mode) ($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 3.6V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	t_{LCY}	SO1 SI1	*1		104		μs
SI1 data setup time	t_{LSU}	SI1		2			μs
SI1 data hold time	t_{LHD}	SI1		2			μs

*1 t_{LCY} is specified only when serial mode register (CH1) (SIOM1: 01FAH) lower 2 bits (SO1 clock selection) is set at $104\mu\text{s}$ according to the system clock frequency.

Note) The load of SO1 pin is 50pF .

Fig. 6. Serial transfer CH1 timing (Special mode)



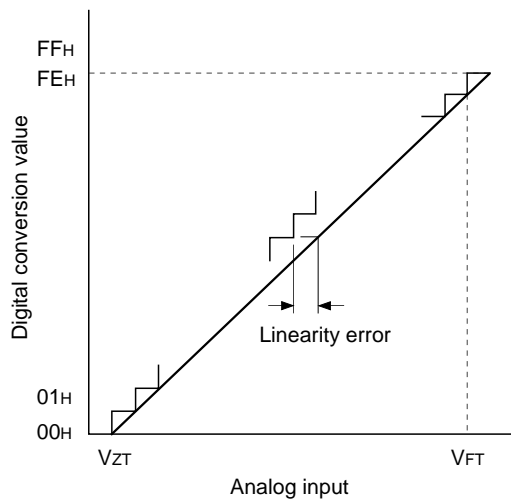
(3) A/D converter characteristics ($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = 4.5$ to 5.5V , $AV_{REF} = 4.0$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation $T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			± 1	LSB
Absolute error						± 2	LSB
Conversion time	t_{CONV}			$160/f_{ADC}^{*1}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^{*1}$			μs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 4.5$ to 5.5V	$AV_{DD} - 0.5$		AV_{DD}	V
Analog input voltage	V_{IAN}	$AN0$ to $AN7$		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode $AV_{REF} = 4.0$ to 5.5V		0.6	1.0	mA
			Sleep mode Stop mode			10	μA

A/D converter characteristics ($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = 3.0$ to 3.6V , $AV_{REF} = 2.7$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation $T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 3.3\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			± 1	LSB
Absolute error						± 2	LSB
Conversion time	t_{CONV}			$160/f_{ADC}^{*1}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^{*1}$			μs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 3.0$ to 3.6V	$AV_{DD} - 0.3$		AV_{DD}	V
Analog input voltage	V_{IAN}	$AN0$ to $AN7$		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode $AV_{REF} = 2.7$ to 3.6V		0.4	0.7	mA
			Sleep mode Stop mode			10	μA

Fig. 7. Definitions of A/D converter terms



*1 The value of f_{ADC} is as follows by interruption selection/
ADC operation clock selection register (MSC: 01FFH)
bit 0 (ADCCK).

When PS2 is selected, $f_{ADC} = f_c/2$

When PS1 is selected, $f_{ADC} = f_c$

(4) Interruption, reset input (Ta = -10 to +75°C, VDD = 3.0 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t _{IH}	$\overline{\text{INT0}}$		1		μs
	t _{IL}	$\overline{\text{INT1}}$ $\overline{\text{INT2}}$ PJ0 to PJ7				
Reset input low level width	t _{RSL}	$\overline{\text{RST}}$		32/fc		μs

Fig. 8. Interruption input timing

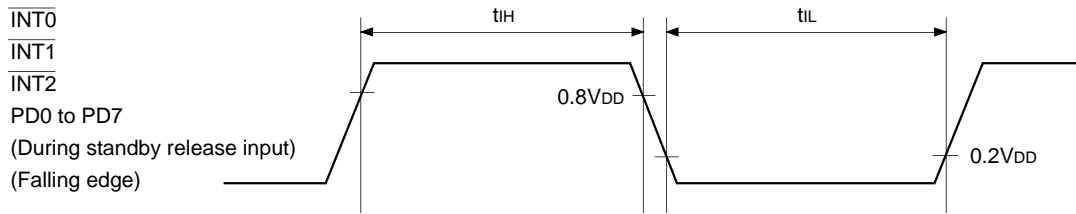
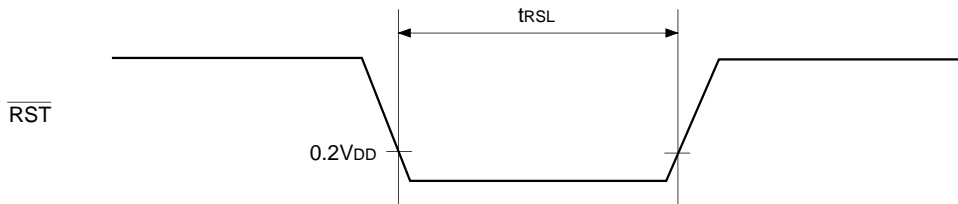


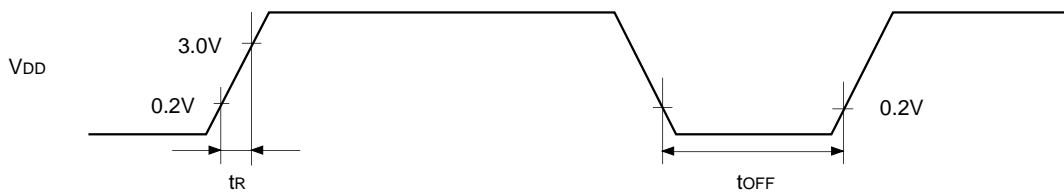
Fig. 9. Reset input timing



(5) Power-on reset (Ta = -10 to +75°C, VDD = 3.0 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t _R	V _{DD}	Power-on reset	0.05	30	ms
Power supply cut-off time	t _{OFF}		Repetitive power-on reset	1		ms

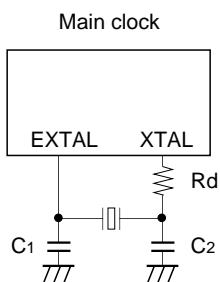
Fig. 10. Power-on reset



The power supply should be turned on smoothly.

Appendix

Fig. 11. SPC700 Series recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	22 (15)	22 (15)	0	(i)
		10.00				
		12.00	15	15		
		16.00	12	12		

Mask Option Table

Item	Content	CXP811P24R-1-□□□	CXP811P24Q-1-□□□
Reset pin pull-up resistor	Non-existent/existent	Existent	Existent
Power-on reset circuit	Non-existent/existent	Existent	Existent

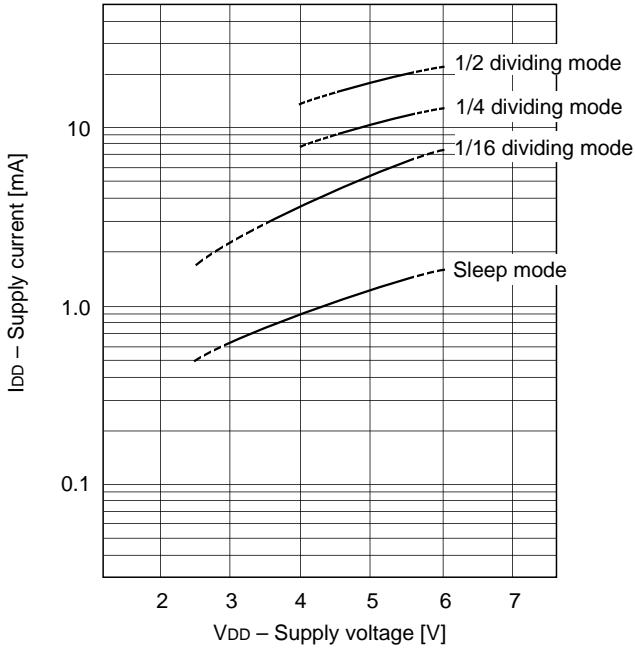
Writing to EPROM

See the "How to write the program into OTP, FLASH, EPROM" for reference.

Characteristics Curve

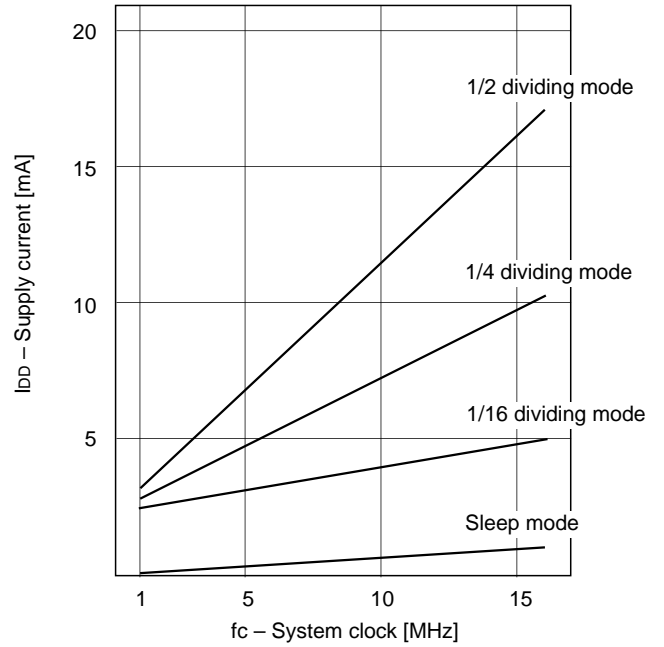
I_{DD} vs. V_{DD}

(f_c = 16MHz, T_a = 25°C, Typical)



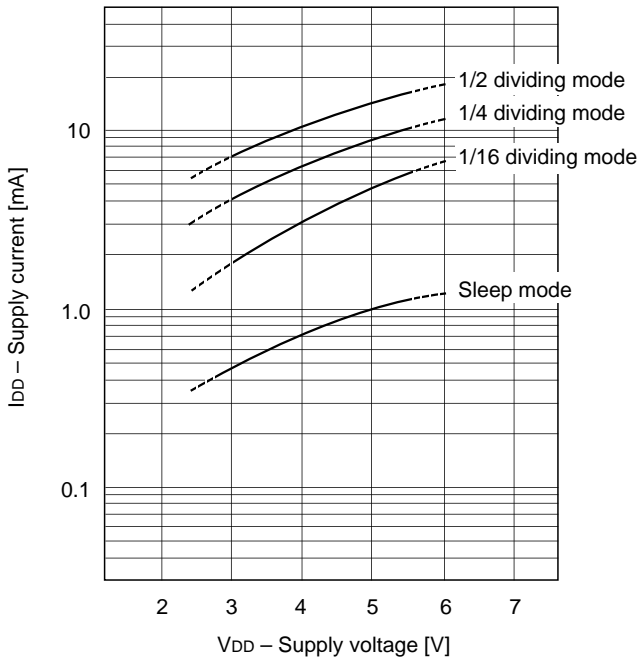
I_{DD} vs. f_c

(V_{DD} = 5.0V, T_a = 25°C, Typical)



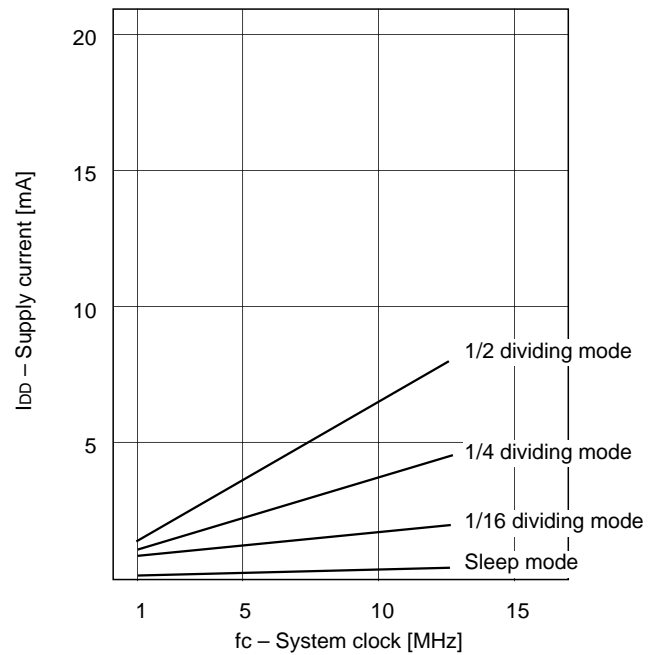
I_{DD} vs. V_{DD}

(f_c = 12MHz, T_a = 25°C, Typical)



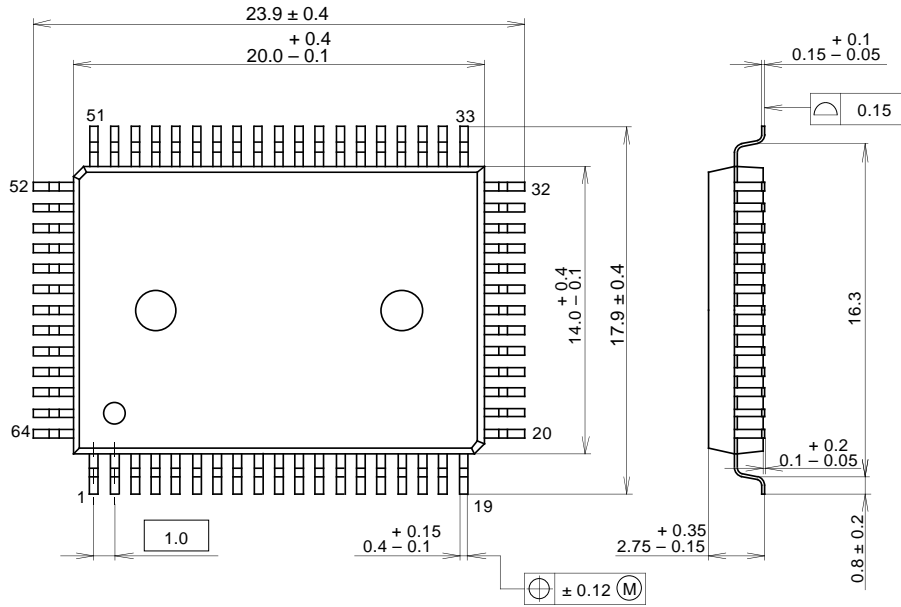
I_{DD} vs. f_c

(V_{DD} = 3.3V, T_a = 25°C, Typical)



Package Outline Unit: mm

64PIN QFP(PLASTIC)

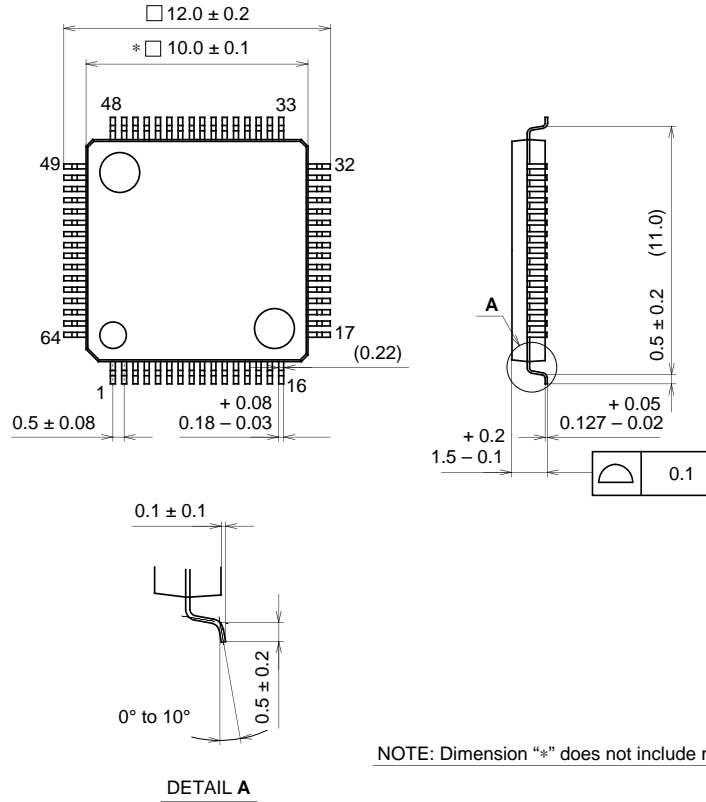


PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	QFP064-P-1420
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

64PIN LQFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	LQFP-64P-L01
EIAJ CODE	LQFP064-P-1010
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.3g