NEC Electronics Inc.

NEC

ADVANCE PRODUCT INFORMATION DATA SHEET

November 1986

μPD3520D

CCD, Single-Board Color Image Sensor

CCD SINGLE-BOARD COLOR IMAGE SENSOR
(NTSC COMPLEMENTARY COLOR TYPE)

The μPD3520D is a highly sensitive color image sensor employing CCD shift registers in its scanning unit. The image size is 1/2 inch and it is suitable for application to video cameras of the NTSC system.

The μPD3520D consists of photodiodes arranged in two dimensions, 427 horizontally and 492 vertically. Each diode has a PN junction of high sensitivity to visible light and visual persistence is practically nil.

The μPD3520D has a newly developed color filter of the complementary color type with a high transmission factor, and the generated image is quite bright and clear.

In particular, the μPD3520D has excellent linearity and uniformity and no skew is produced in the images, and this feature is effective in minimizing adjustment circuits and in reducing man-hours.

The pitch of a pixel is 15.3 μm in the horizontal and 9.9 μm in the vertical directions. The μPD3520D is in a 20-pin ceramic dual in-line package (DIP) of the shrunken type (1.778 mm pitch) suitable for minimizing weight and dimensions.

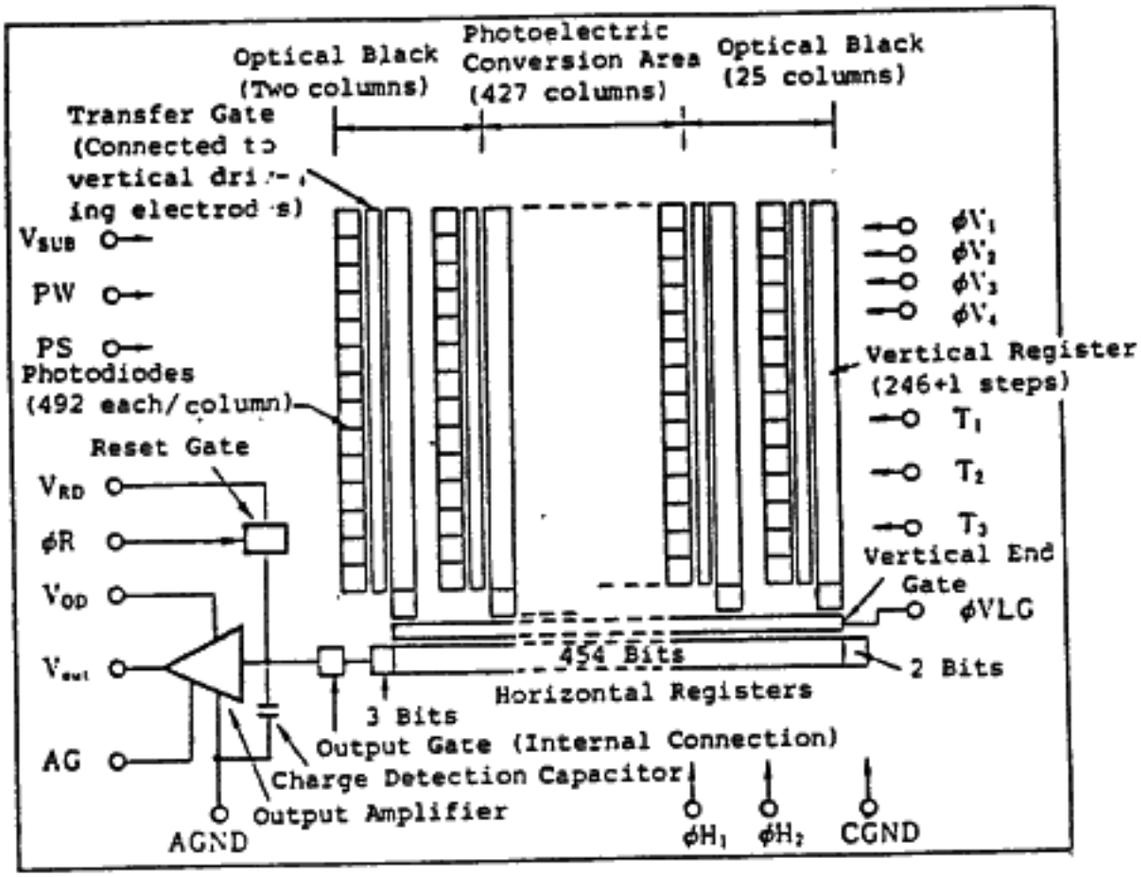
FEATURES

- High sensitivity. The minimum intensity of illumination required on the surface of subjects: 8 lux (F1.2, AGC:12dB).
- Field-period reading system of high dynamic resolution.
- Low visual persistence without commet tail, and bright images for low intensity of illumination.
- No baking.
- Shielding against magnetism allows placement near speakers.
- Vibration-hardened, and no microphonic noises are generated.
- It may be stored for a long time without degradation.
- A digital clock system is employed for perfect color separation for low intensity of illumination.
- Resolution 280 TV lines horizontally
  350 TV lines vertically
- 1/2 inch image size (6.40 mm x 4.80 mm)

APPLICATION

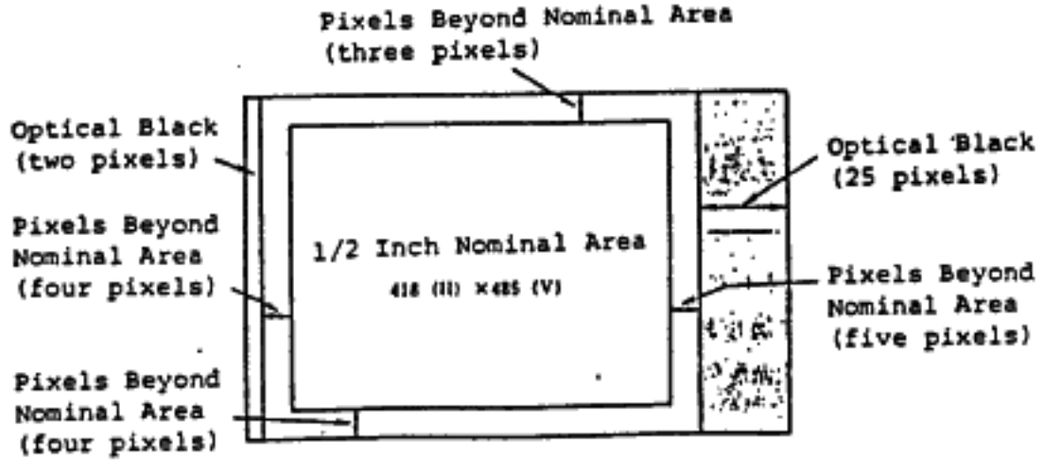
- Color video cameras
- Color image input equipment

BLOCK DIAGRAM



Vertical Register:	No photodiode	1 step
	With photodiode	246 steps
Horizontal Register:	No vertical register	3 bits
	With vertical register	454 bits
	No vertical register	2 bits

PICTURE ELEMENT CONFIGURATION



TYPICAL CHARACTERISTICS

Number of pixels in photo-electric conversion area	427 H x 492 V	
Optical black	Two pixels before and 25 pixels after nominal area in each line	
Number of pixels in nominal area	418 H x 485 V	
Nominal area	6.395 4 H x 4.801 5 V	mm
Photoelement pitch	15.3 H x 9.9 V	μm
Source clock for synchroniza-tion and scanning systems	15.891 6 (1010 f_H)	MHz
PLL comparison frequency	15.734 265 (f_H=4 f_{sc}/910)	kHz

Items	Designed Value	Standards	Unit
Horizontal scanning period	63.555 6	63.555 6	μs
Horizontal nominal area scanning time	52.606 4	52.656±0.2	μs
Horizontal returning time	10.949 2	10.9±0.2	μs

NTSC STANDARDS (REFERENCE)

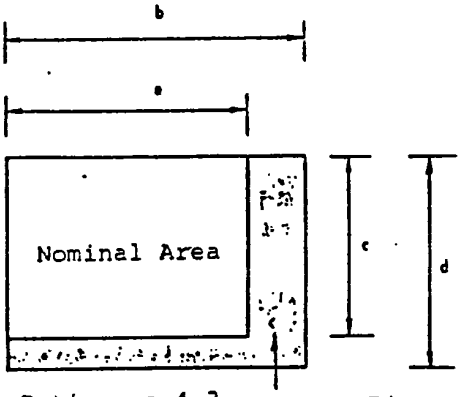
f_{SC} = 3.579 545 MHz

$f_H = 2f_{SC}/455$

$f_V = 2f_H/525$

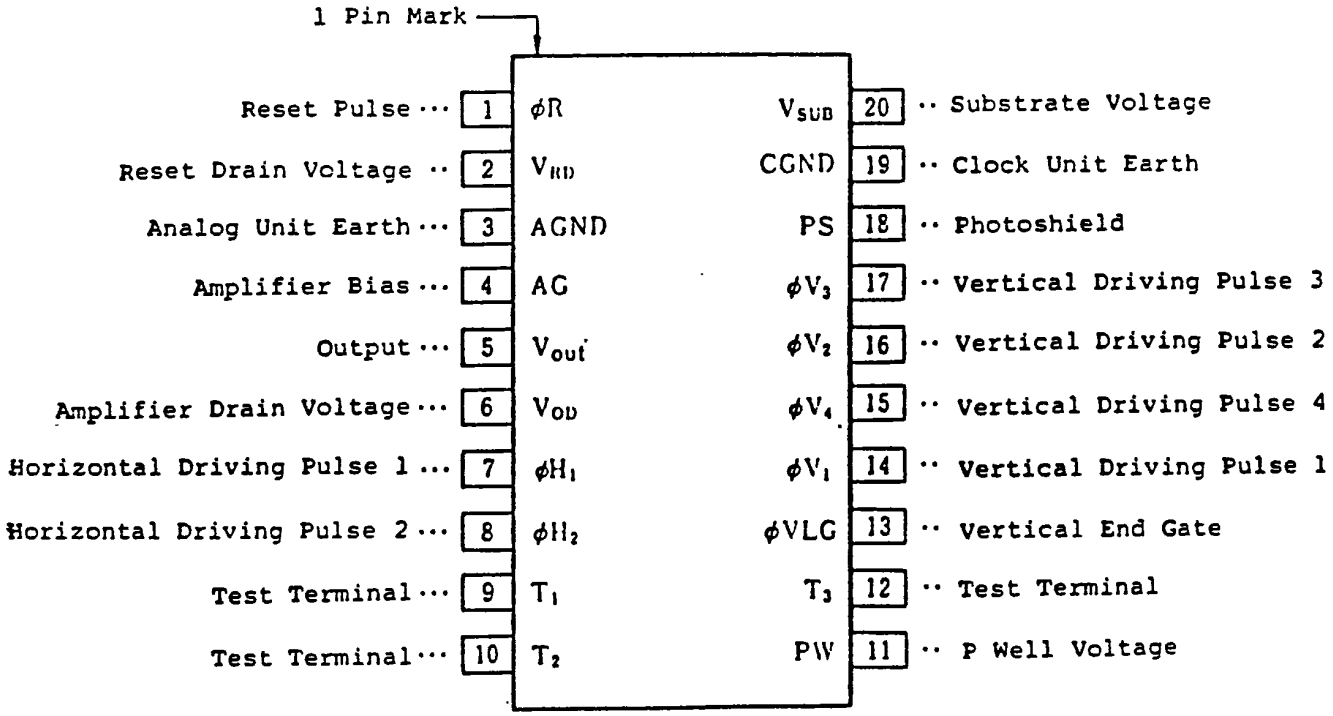
The figure below b = 63.555 555 63 μs, d = 16.683 335 455 5 ms

a = 52.656 ± .2 μs, c = d × 485/525 = 15.412 224 19 ms



Aspect Ratio a:c=4:3 Blanking Time

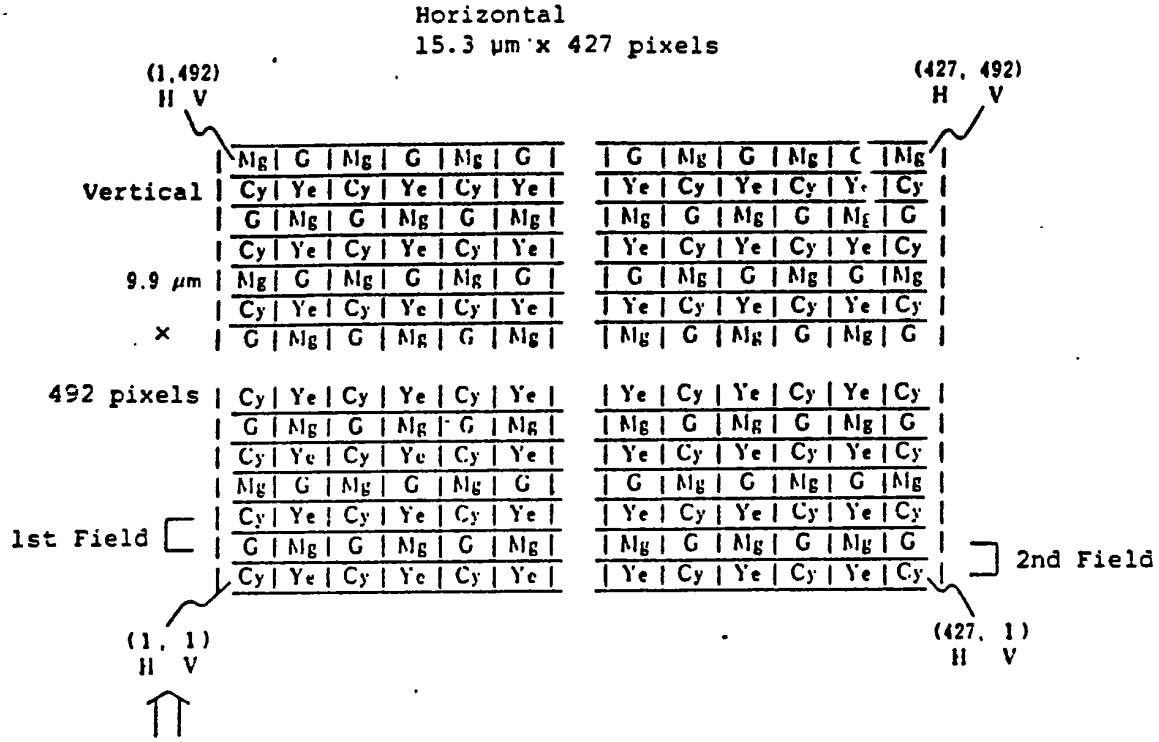
TERMINAL CONNECTIONS (TOP VIEW)



TERMINAL FUNCTIONS

No.	Symbols	Terminal Functions
1	ϕR	Gate driving pulse for neutralizing signal charges of charge detection capacitor
2	V_{RD}	Power supply for reset gate
3	AGND	Earth terminal for output amplifier unit
4	AG	Bias voltage of output amplifier
5	V_{out}	Output
6	V_{OD}	Power supply for output amplifier
7	ϕH_1	Driving pulse for horizontal register
8	ϕH_2	Driving pulse for horizontal register
9	T_1	Test terminal
10	T_2	Test terminal
11	PW	P well bias voltage for element separation
12	T_3	Test terminal
13	ϕVLG	Gate transferring signals from vertical registers to horizontal registers
14	ϕV_1	Driving pulse for horizontal register, transfer gate pulse (ϕPG) is overridden
15	ϕV_4	Driving pulse for horizontal register
16	ϕV_2	Driving pulse for horizontal register
17	ϕV_3	Driving pulse for horizontal register, transfer gate pulse (ϕPG) is overridden
18	PS	Electrode for light protection
19	CGND	Earth for driving unit
20	V_{SUB}	Substrate Bias voltage

COLOR FILTER ARRANGEMENT

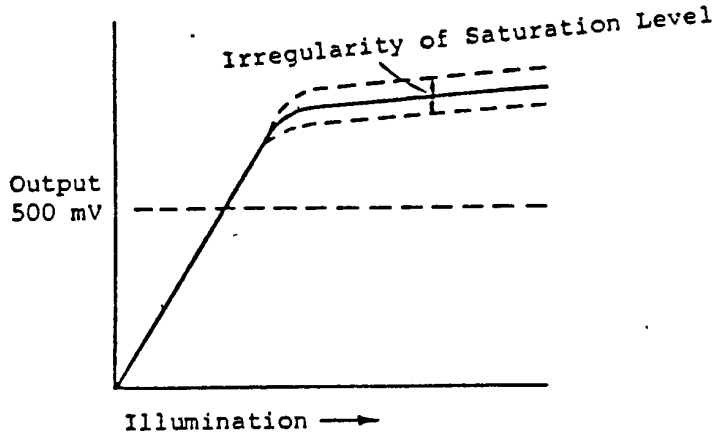


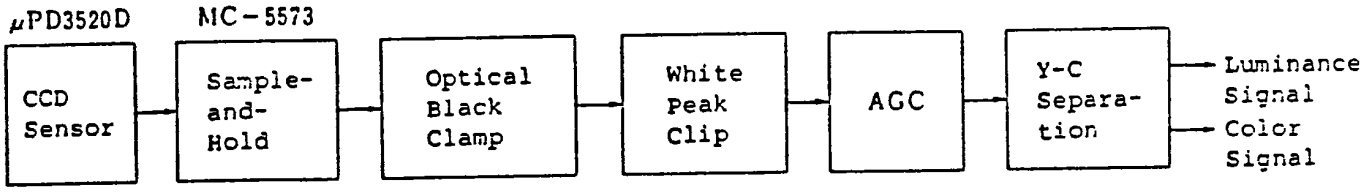
Compatible Color Temperature 4300 K
Recommended Infrared Cut Filter HOYA C-500 with thickness of 1 mm.

REMARKS ON OUTPUT SIGNAL PROCESSING

At the saturation point of the output of the CCD sensors, an irregularity in saturation level may appear in the images. CCD sensors shall be used with their peak clipped after Sample-and-Hold processing by the MC-5573.

The clip point shall be fixed at 500 mV or shall be adjusted individually.





ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Items	Symbols	Ratings	Unit
Amplifier drain voltage	V_{OD}	0 to +18	V
Reset unit drain voltage	V_{RD}	0 to V_{OD}	V
Photoshield voltage	V_{PS}	0 to V_{OD}	V
Vertical end gate voltage	$V_{\phi VLG}$	V_{PW} to V_{OD}	V
Amplifier gate voltage	V_{AG}	0 to 5.0	V
Substrate voltage	V_{SUB}	0 to +20	V
P well voltage	V_{PW}	-8.3 to +0.5	V
Test terminal T1 voltage	V_{T1}	0 to V_{OD}	V
Test terminal T2 voltage	V_{T2}	0 to V_{OD}	V
Test terminal T3 voltage	V_{T3}	0 to V_{OD}	V
Horizontal transfer pulse voltage	$V_{\phi H}$	-0.3 to V_{OD}	V
Vertical transfer pulse voltage	$V_{\phi V}$	V_{PW} to V_{OD}	V
Reset pulse voltage	$V_{\phi R}$	-0.3 to V_{OD}	V
Operational temperature	T_{opt}	-10 to +55	°C
Storage temperature	T_{stg}	-20 to +80	°C

RECOMMENDED OPERATION TEMPERATURE (Ta=-10 to +45°C)

Items	Symbols	MIN.	TYP.	MAX.	Unit
Infrared cut filter	IRF	C-500 with thickness of 1 mm			
Operation temperature	T_{opt}	0	+25	+45	°C
Amplifier drain voltage	V_{OD}	14.5	15.0	15.5	V
Reset unit drain voltage	V_{RD}	V_{OD}-0.2	V_{OD}	V_{OD}	V
Photoshield voltage	V_{PS}	1.00	1.25	1.50	V
Amplifier gate voltage	V_{AG}	2.7	3.0	3.3	V
Upper limit of adjustable range of substrate voltage	$V_{UL(SUB)}$	18		20	V
Lower limit of adjustable range of substrate voltage	$V_{LL(SUB)}$	4.0	4.5	5.0	V
P well voltage	V_{PW}	-8.2	$V_{L\phi V}$-1.0	$V_{L\phi V}$-0.7	V
Test terminal T1 voltage	V_{T1}		0		V
Test terminal T2 voltage	V_{T2}	V_{OD}-3.0	V_{OD}	V_{OD}	V
Test terminal T3 voltage	V_{T3}		0		V
High level voltage of vertical transfer pulse	$V_{H\phi V}$		0		V
Low level voltage of vertical transfer pulse	$V_{L\phi V}$	-7.5	-7.0	-6.8	V
Transfer gate ON voltage *1	$V_{\phi TG}$	11.5	12.0	12.5	V
High level voltage of horizontal transfer pulse	$V_{H\phi H}$	7.7	8.0	10.0	V
Low level voltage of horizontal transfer pulse	$V_{L\phi H}$	0		0.7	V
High level voltage of reset pulse	$V_{H\phi R}$	8.7	9.0	13.0	V
Low level voltage of reset pulse	$V_{L\phi H}$	0		0.7	V
High level voltage of vertical end gate	$V_{H\phi VLG}$		0		V
Low level voltage of vertical end gate	$V_{L\phi VLG}$		$V_{L\phi V}$		V

*1: Clock peak voltage to be added on the vertical transfer clock.

PHOTOELECTRIC CHARACTERISTICS
(Ta=25°C, infrared cutting with HOYA C-500 of 1 mm thickness)

No.	Items	Symbols	Condition	MIN.	TYP.	MAX.	Unit
1	Saturated output voltage	V_{sat}	20 times light	500	800		mV
2	Average standard output	VO	Subject luminance: 82 nt	200	250		mV
3	Sensitivity	S	*3	283	354		V/ Lumen
4	Averaged output in darkness	ADS	Ta=25°C		1.5	5.0	mV
5	Blooming suppression substrate voltage	V_{BLM}	100 times light *4	5		18	V
6	Smear	SMR	1/10 pattern of vertical direction			0.10	%

Note: *1, *4: In both cases, the light shall have an intensity 20 or 100 times that of the intensity when the output from the sensor is 250 mV.

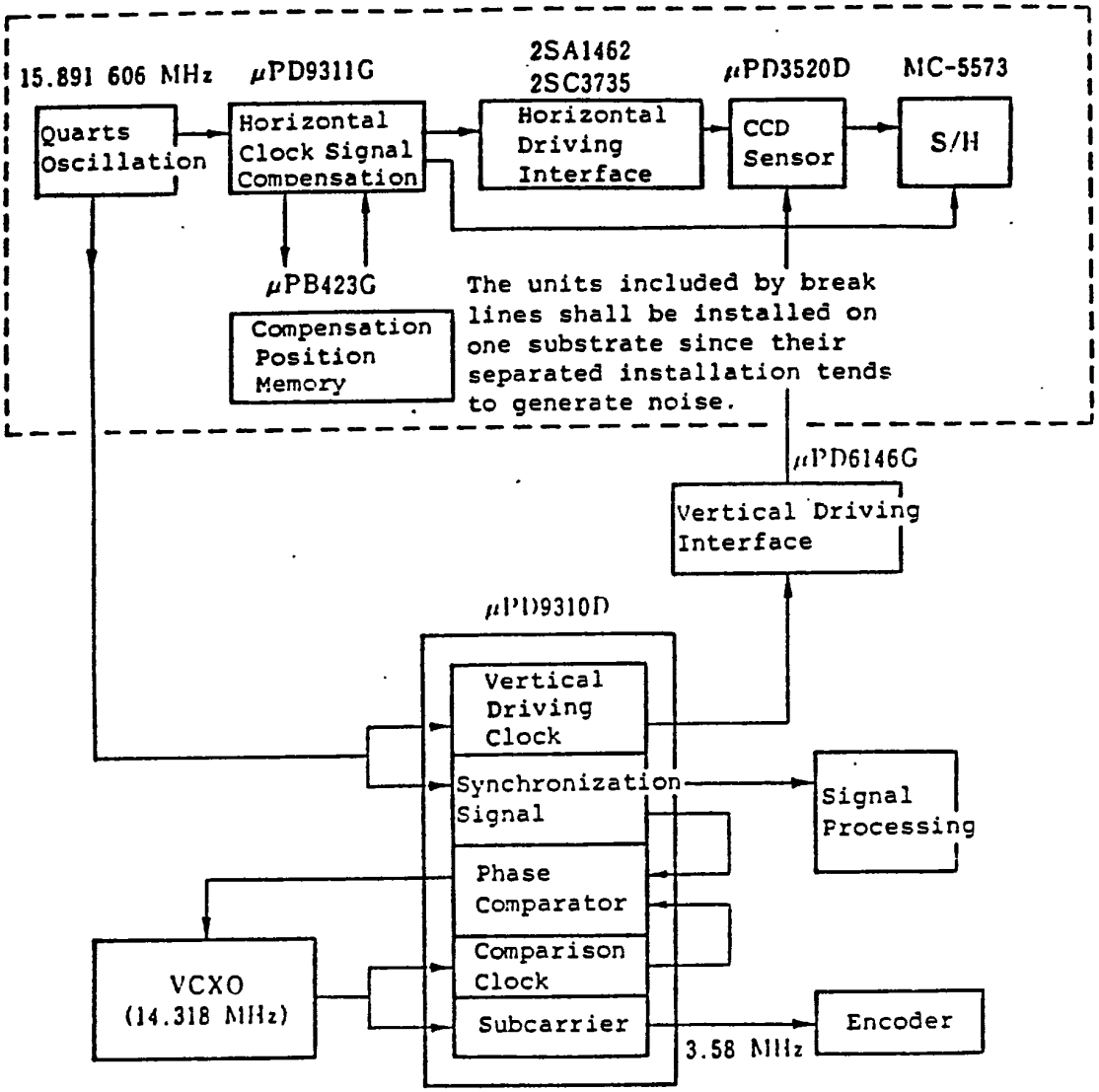
*2: Fujinon CF25L (f=25 mm, F0.85) is used as the lens with its exposure scale set at F1.4. It corresponds to 23 lx on the surface of the sensor. For obtaining the intensity of illumination on the surface of subjects, the following formula is used.

Luminance (nt) = Intensity of illumination (lx) x Reflection Ratio (%)

*3: Sensitivity value is defined to the light volume input to the nominal area so that is can be compared with sensors of different image sizes direct.

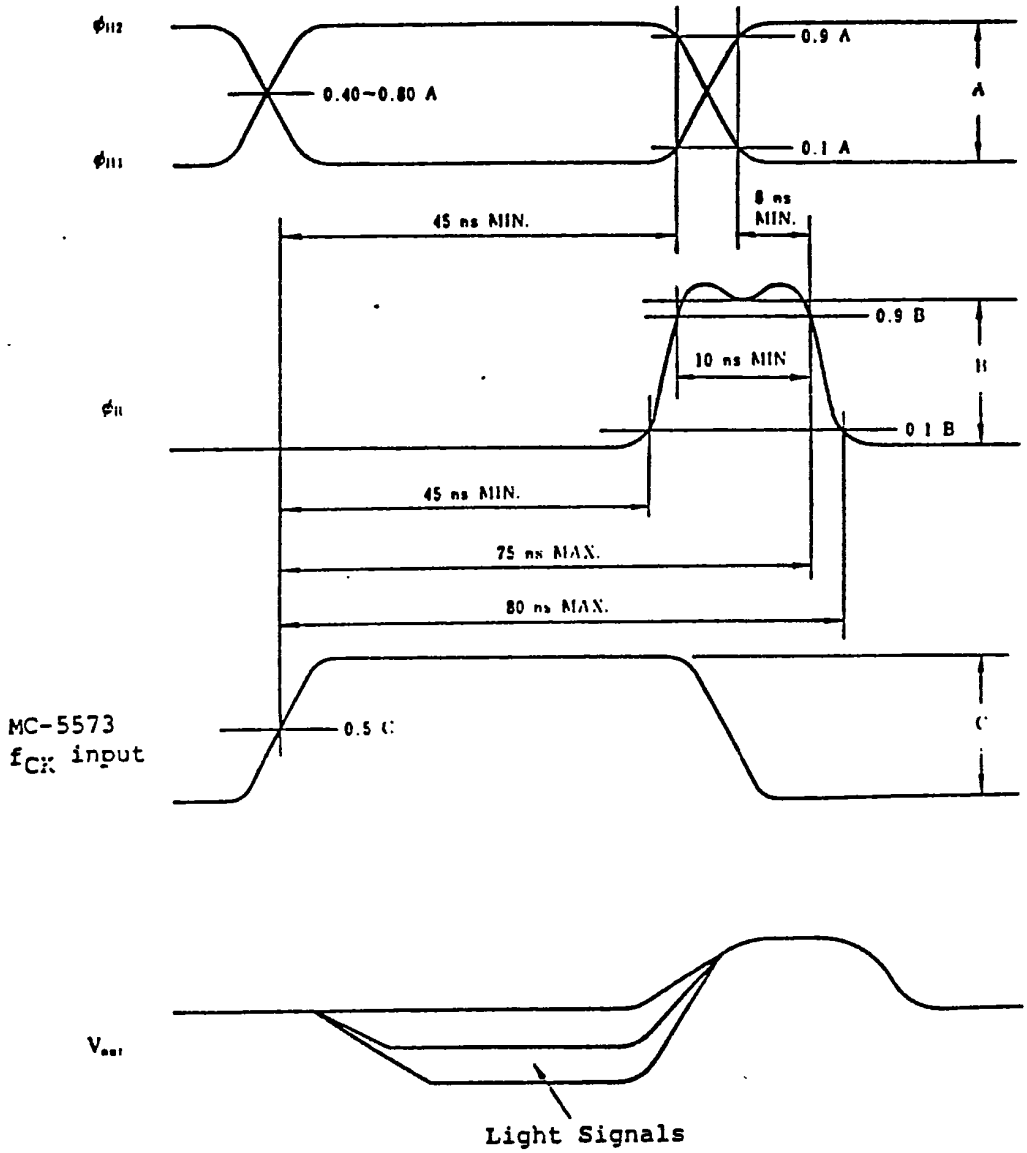
$$\text{Sensitivity (V/lumen)} = \frac{\text{Output (V)}}{\text{Intensity on chip surface (lx)} \times \text{Area of nominal area } (m^2)}$$

SURROUNDING KIT BLOCK DIAGRAM (NTSC)



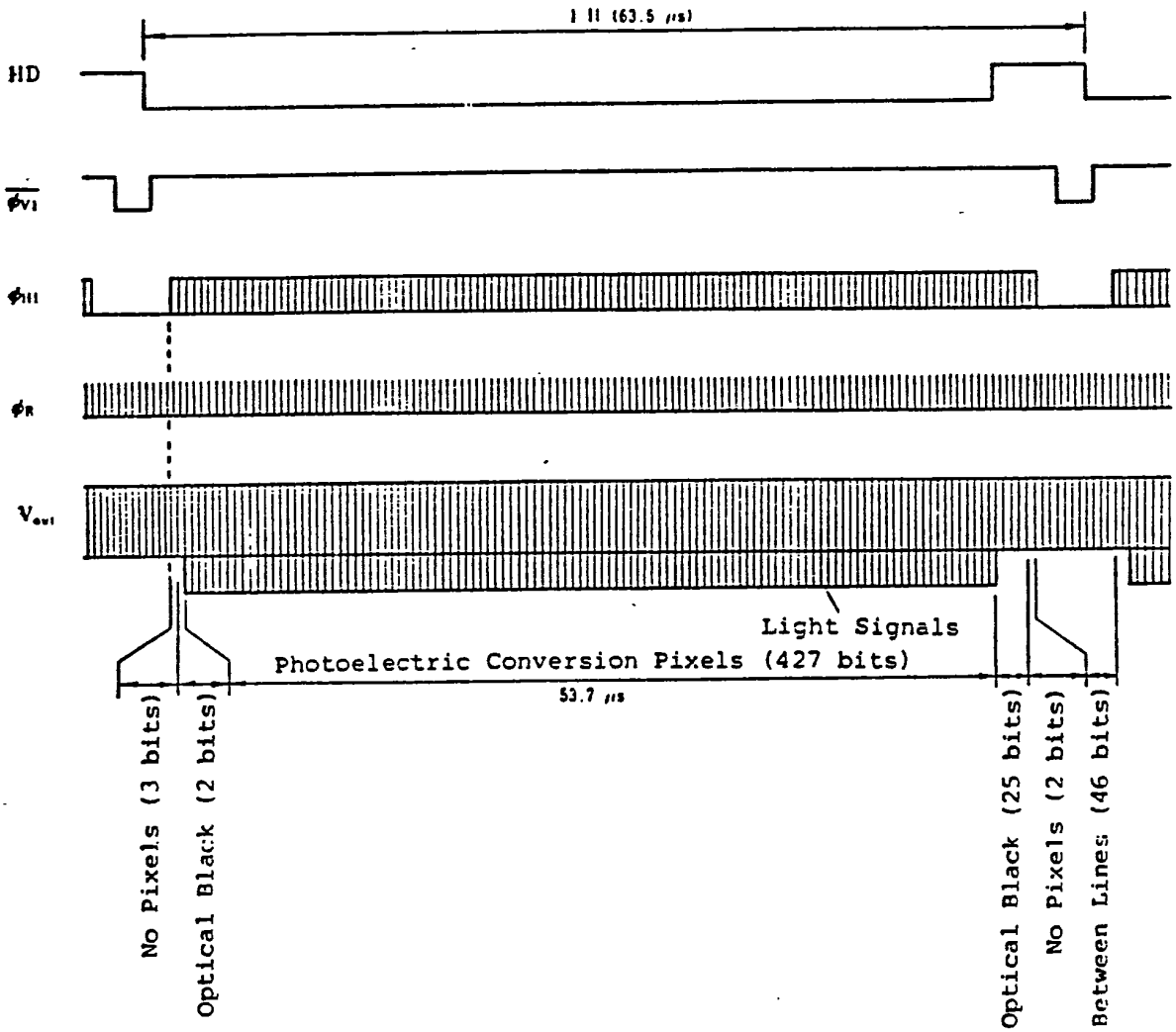
TIMING CHART

Horizontal Transfer/Reset Timing

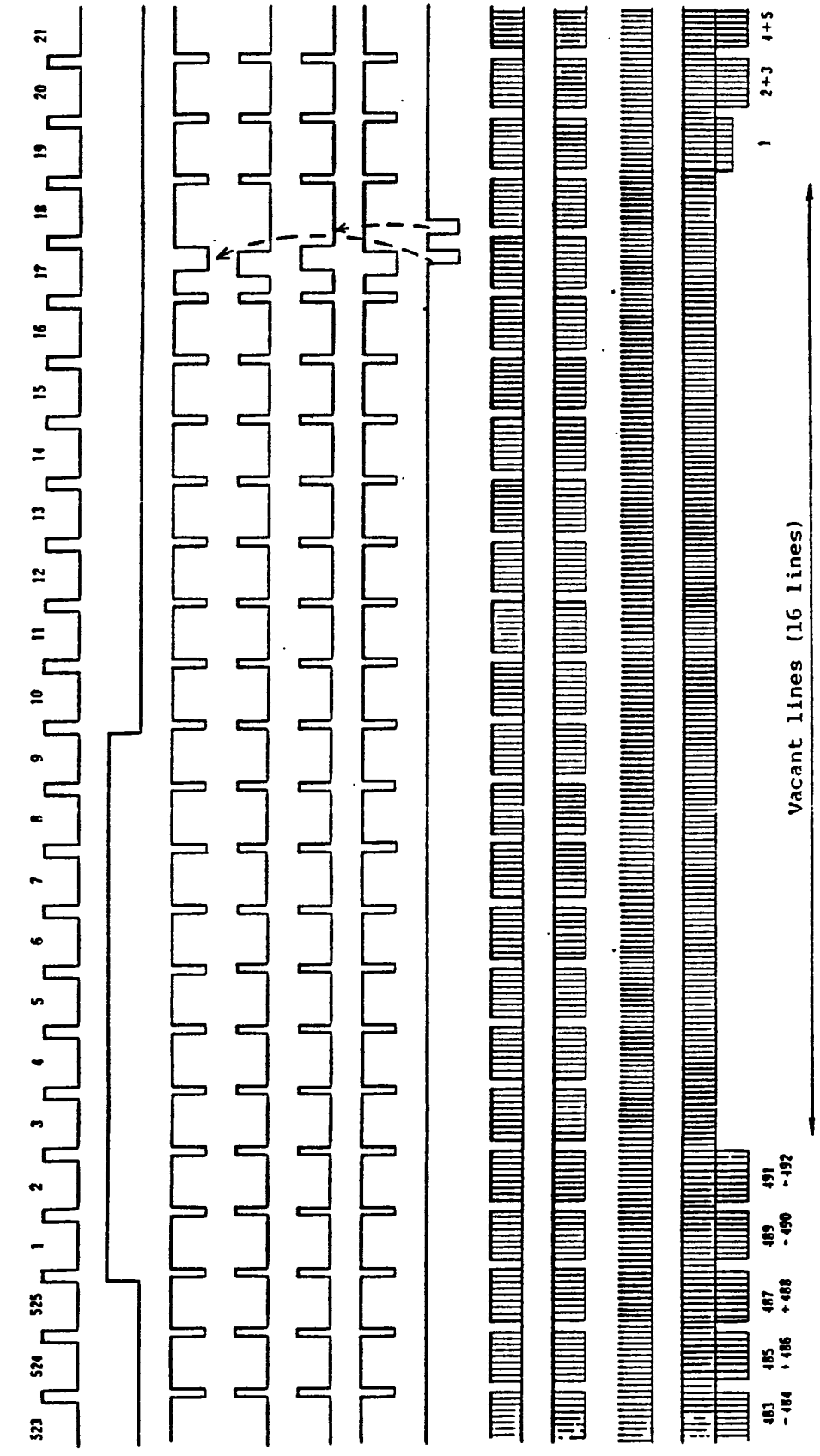


Ringing shall be minimized at the ϕ_H, and also shooting to negative voltage shall be avoided.

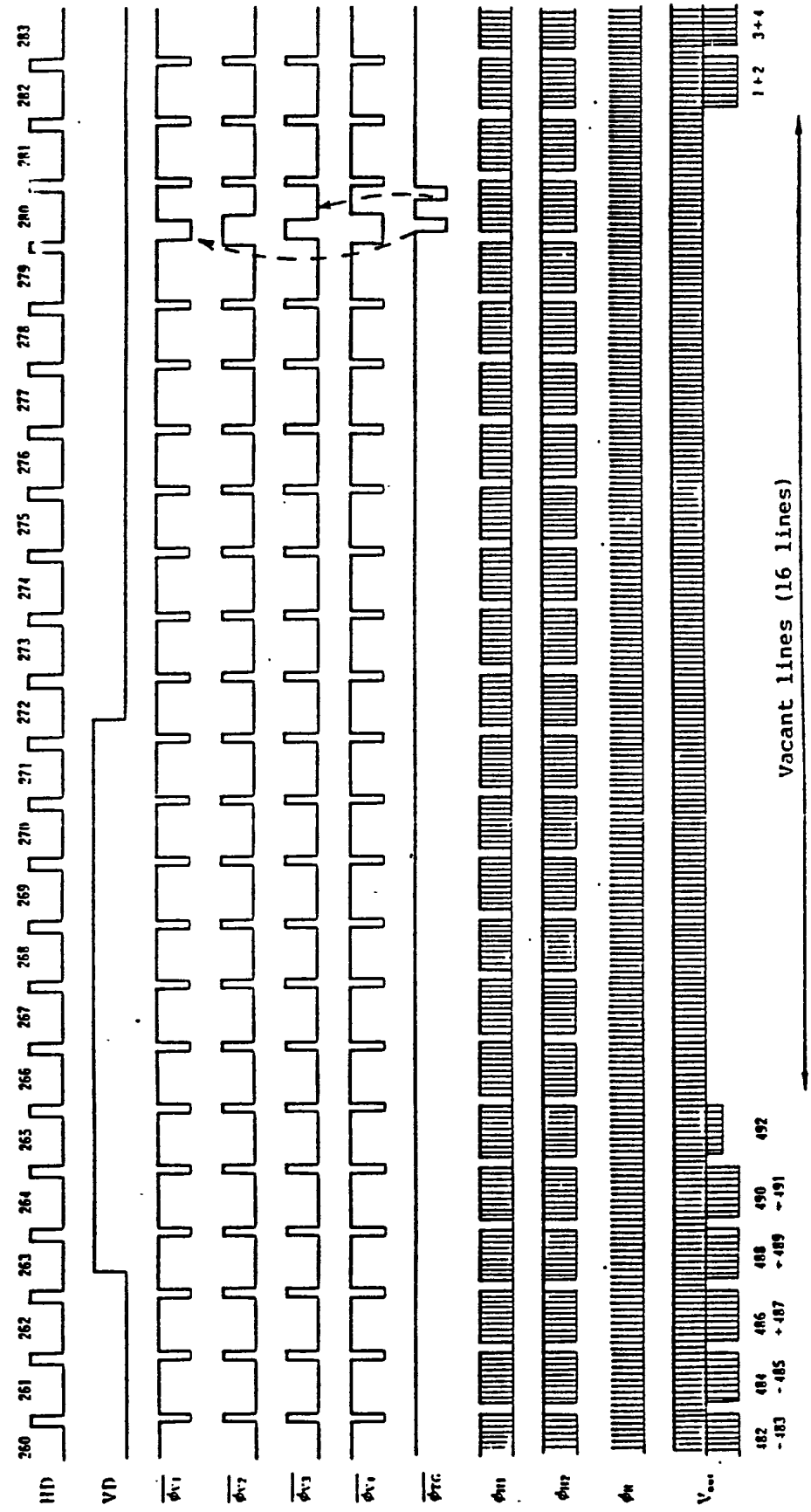
OUTPUT TIMING (ONE LINE)



TIMING BETWEEN 1ST AND 2ND FIELDS

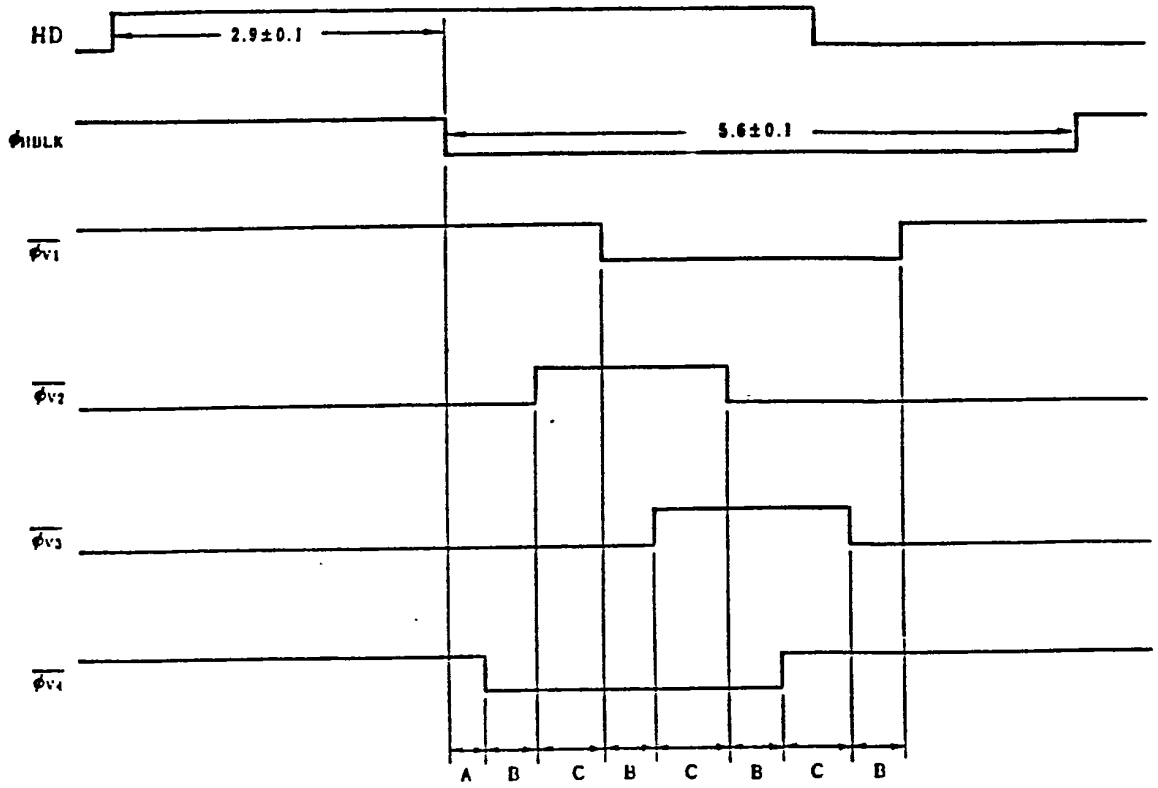


TIMING BETWEEN 1ST AND 2ND FIELDS



VERTICAL TRANSFER TIMING

Unit: μs

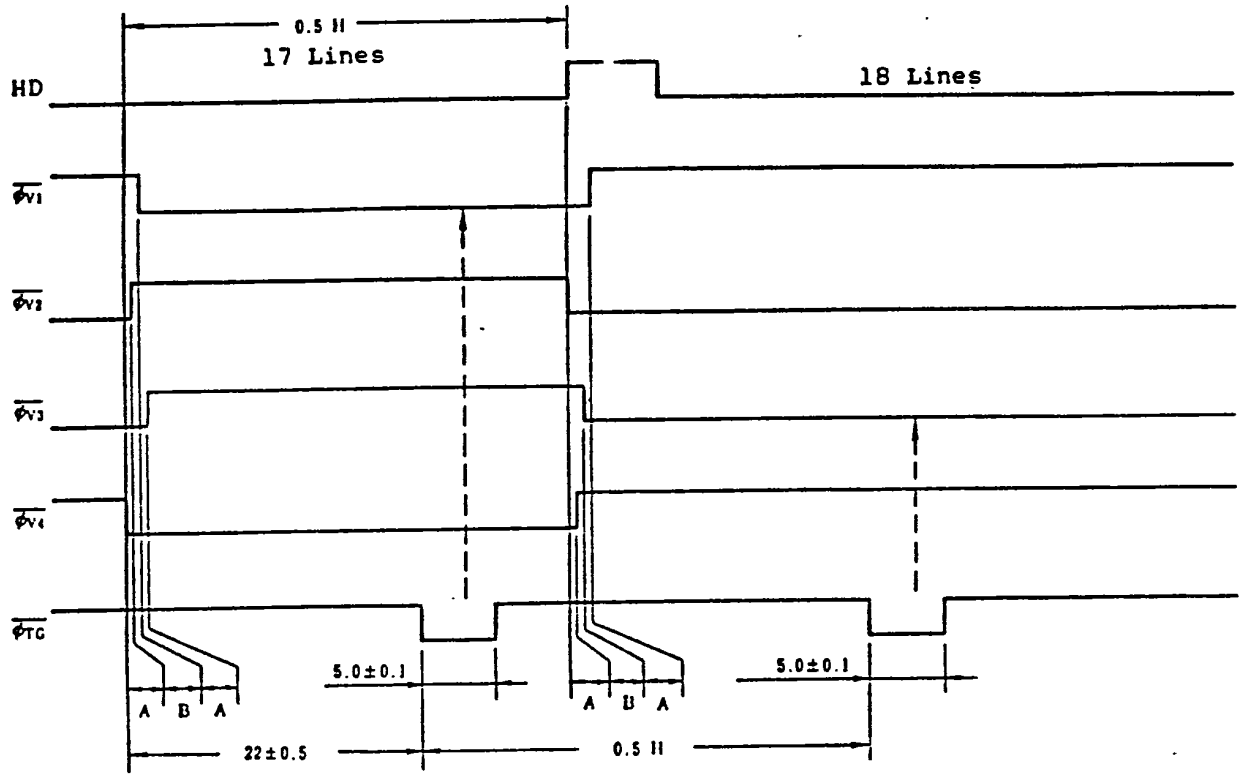


A : 0.30±0.05 B : 0.50±0.05 C : 0.60±0.05

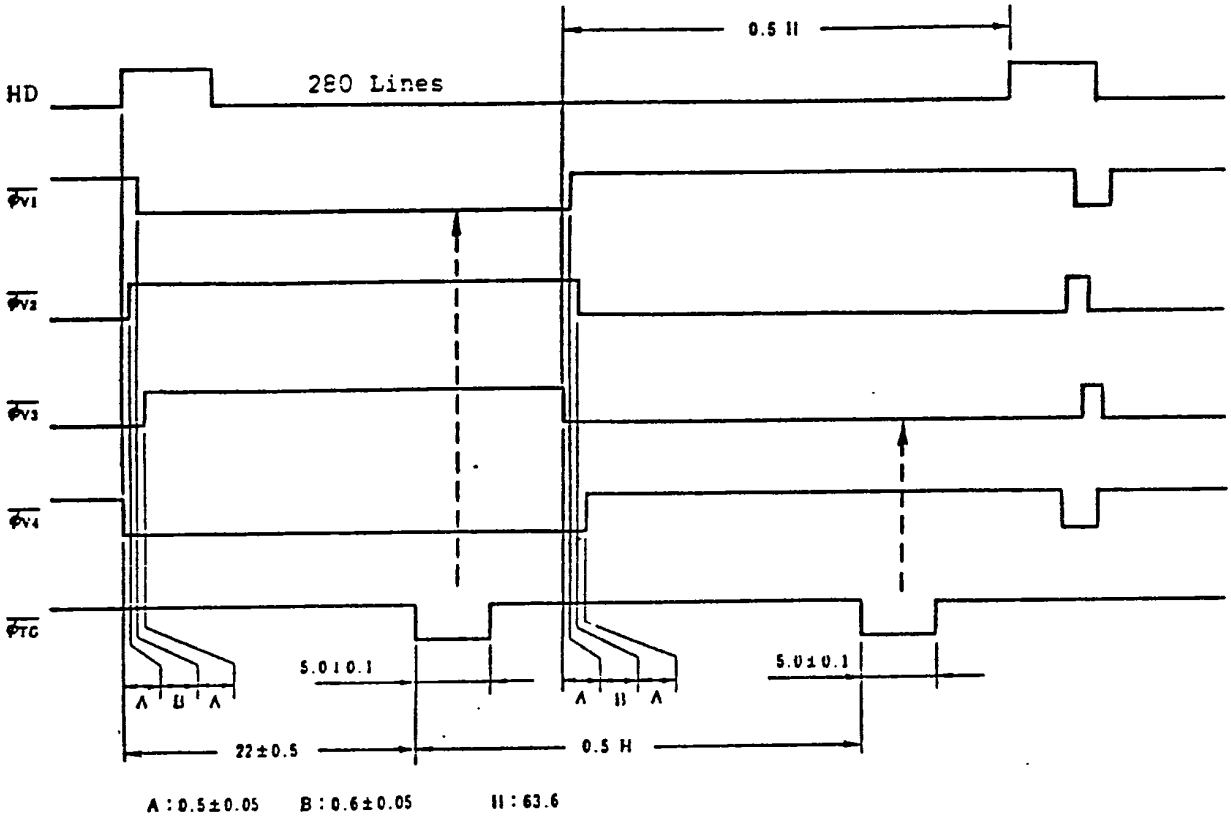
PHOTODIODE READING TIMING

1st Field

Unit: μs

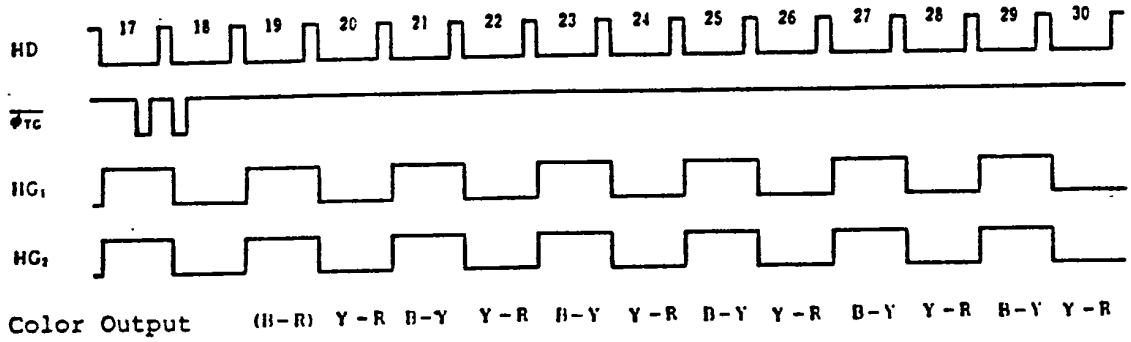


2nd Field

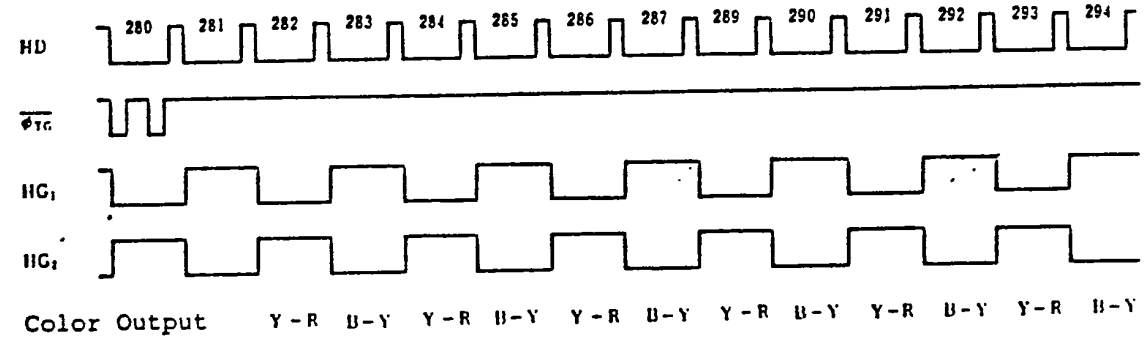

0.5 H
HD
280 Lines
$\overline{\phi V1}$
$\overline{\phi V2}$
$\overline{\phi V3}$
$\overline{\phi V4}$
$\overline{\phi TG}$
5.0±0.1
5.0±0.1
A B A
A B A
22±0.5
0.5 H
A : 0.5±0.05 B : 0.6±0.05 H : 63.6

COLOR SIGNAL OUTPUT TIMING

(1) 1st Field



(2) 2nd Field

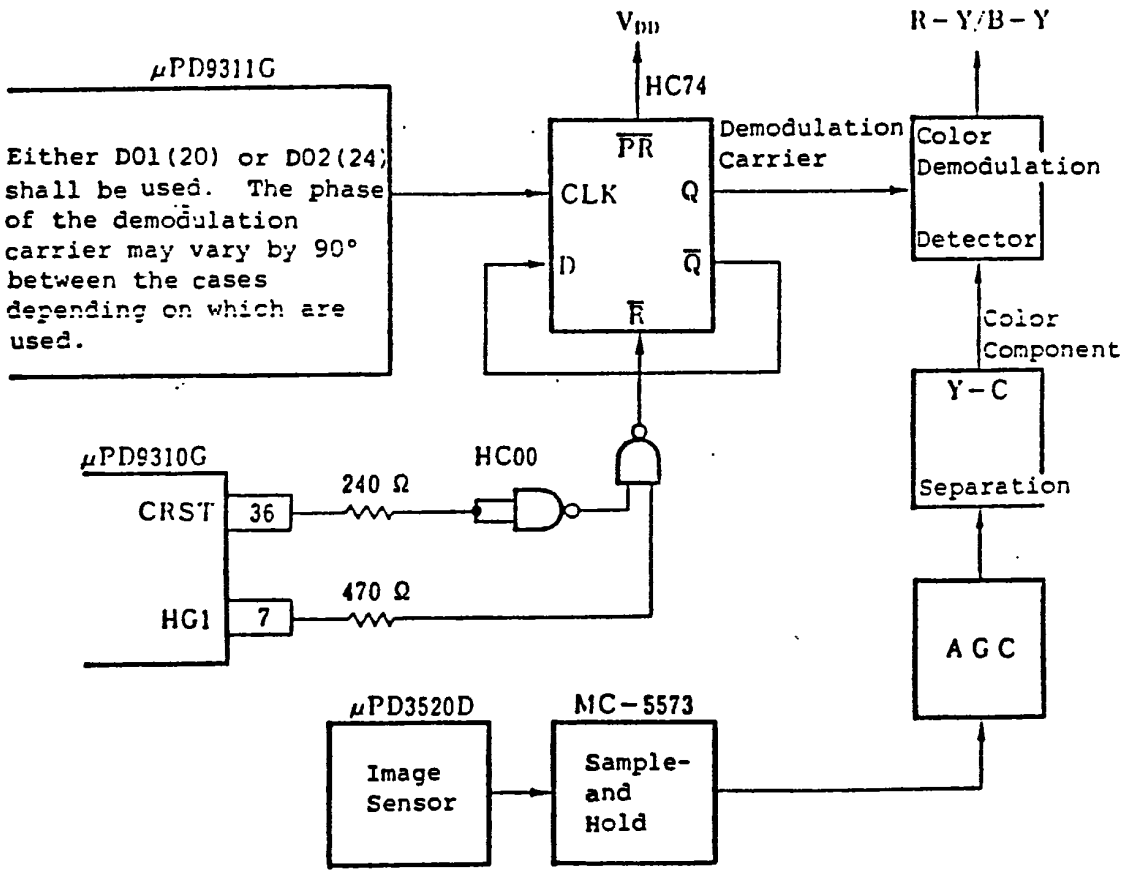


REMARKS ON COLOR SIGNALS

In the above timing diagram, color output is expressed by Y-R and B-Y instead of R-Y and B-Y. The reason is that, if the carrier clock phase for color demodulation is matched with the scanning start of each line, the polarities of demodulated output of the R-Y component and the B-Y component are different.

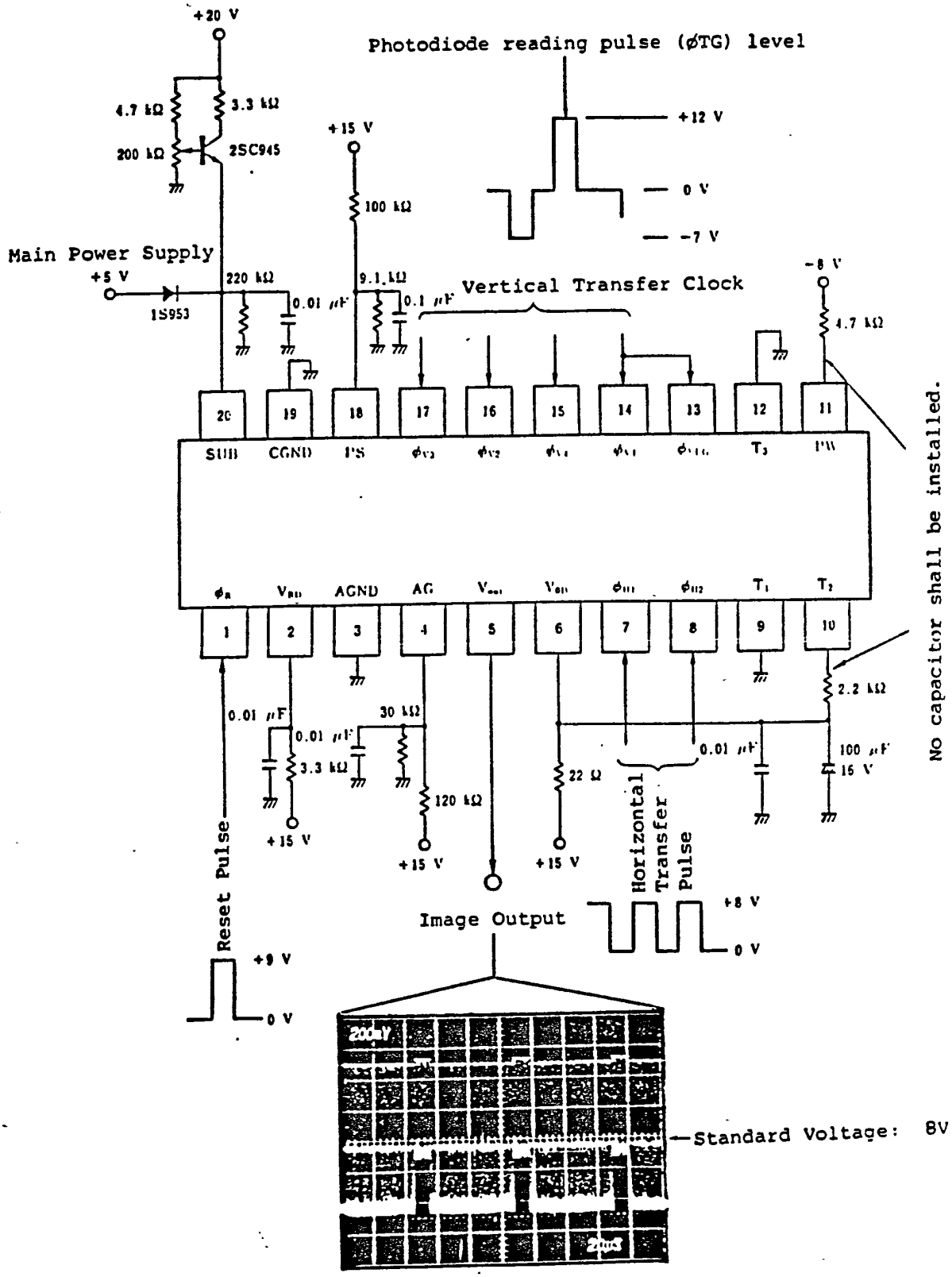
For avoiding such a discrepancy, the carrier clock phases for color demodulation shall be reversed at every other line.

If you use the μPD9310G or the μPD9311G, CRST shall be placed at every other line, as shown in the figure below.



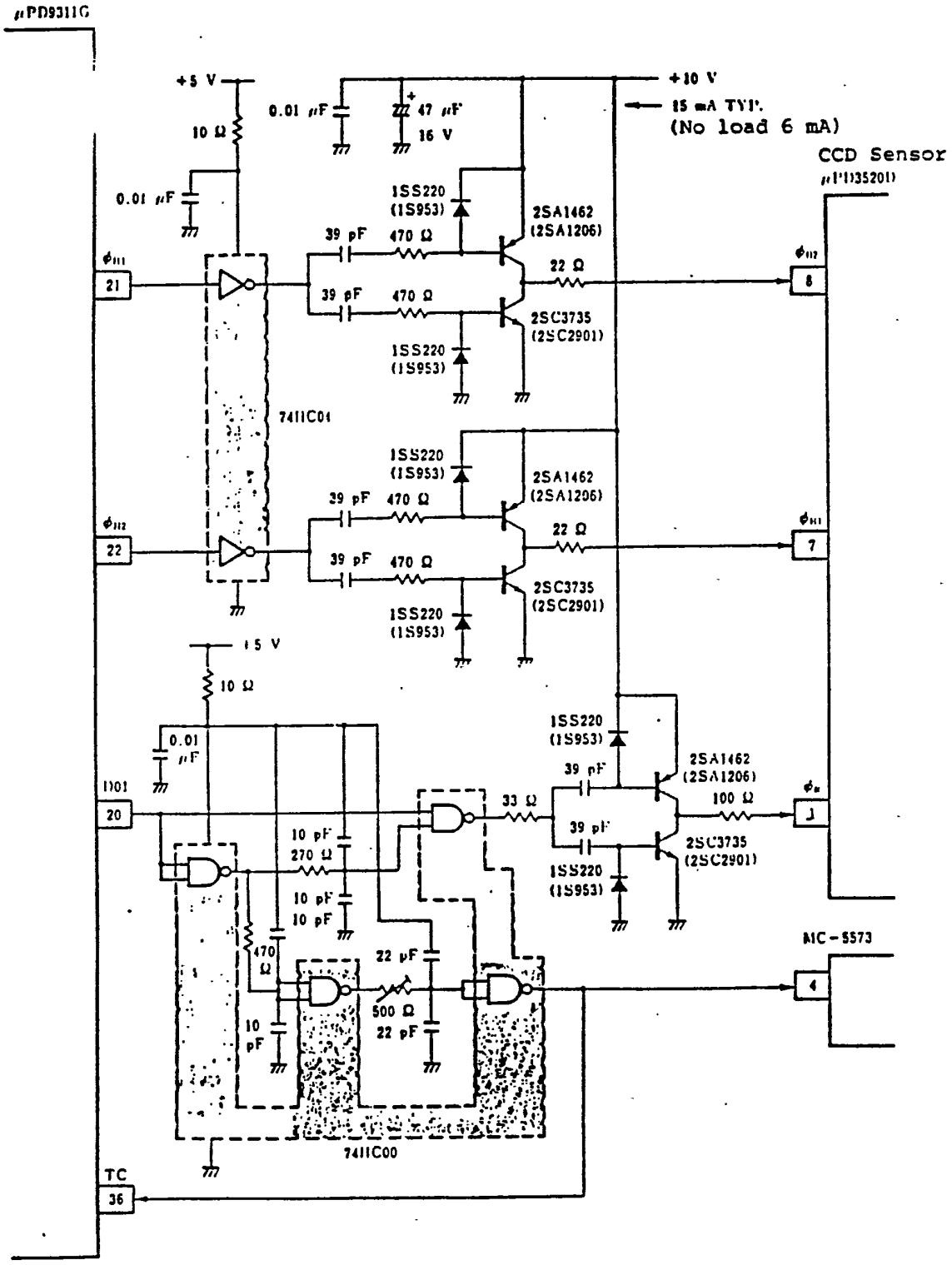
BIAS CIRCUIT

The sequence for turning on the power supply is SUB voltage (+5V is acceptable) → +15V → -8V.



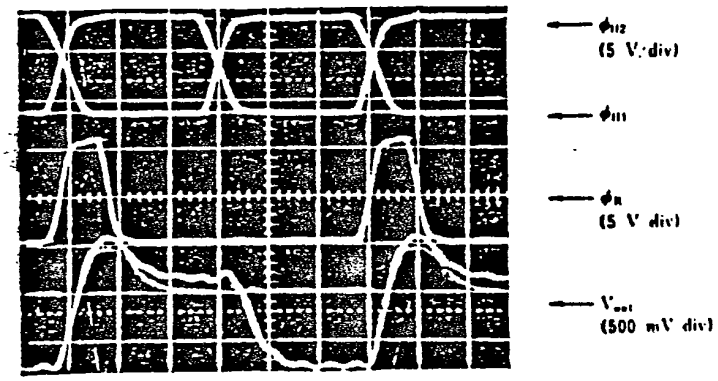
ϕ_H, ϕ_D DRIVING INTERFACE AND MC-5573 CLOCK

Please pay enough attention to the connection diagram, since enough consideration is not given to clock noises etc. there.

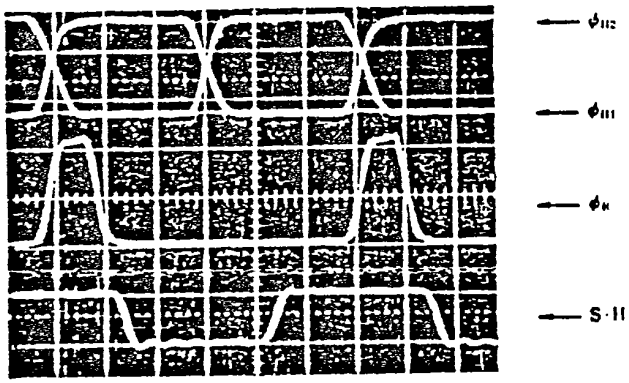


μPD3520D ϕ_H, ϕ_D TIMING

Horizontal: 20 ns/div

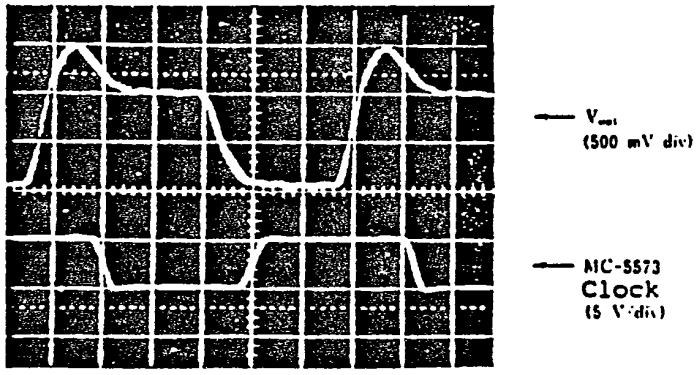


Vertical: 5V/div
Horizontal: 20 ns/div

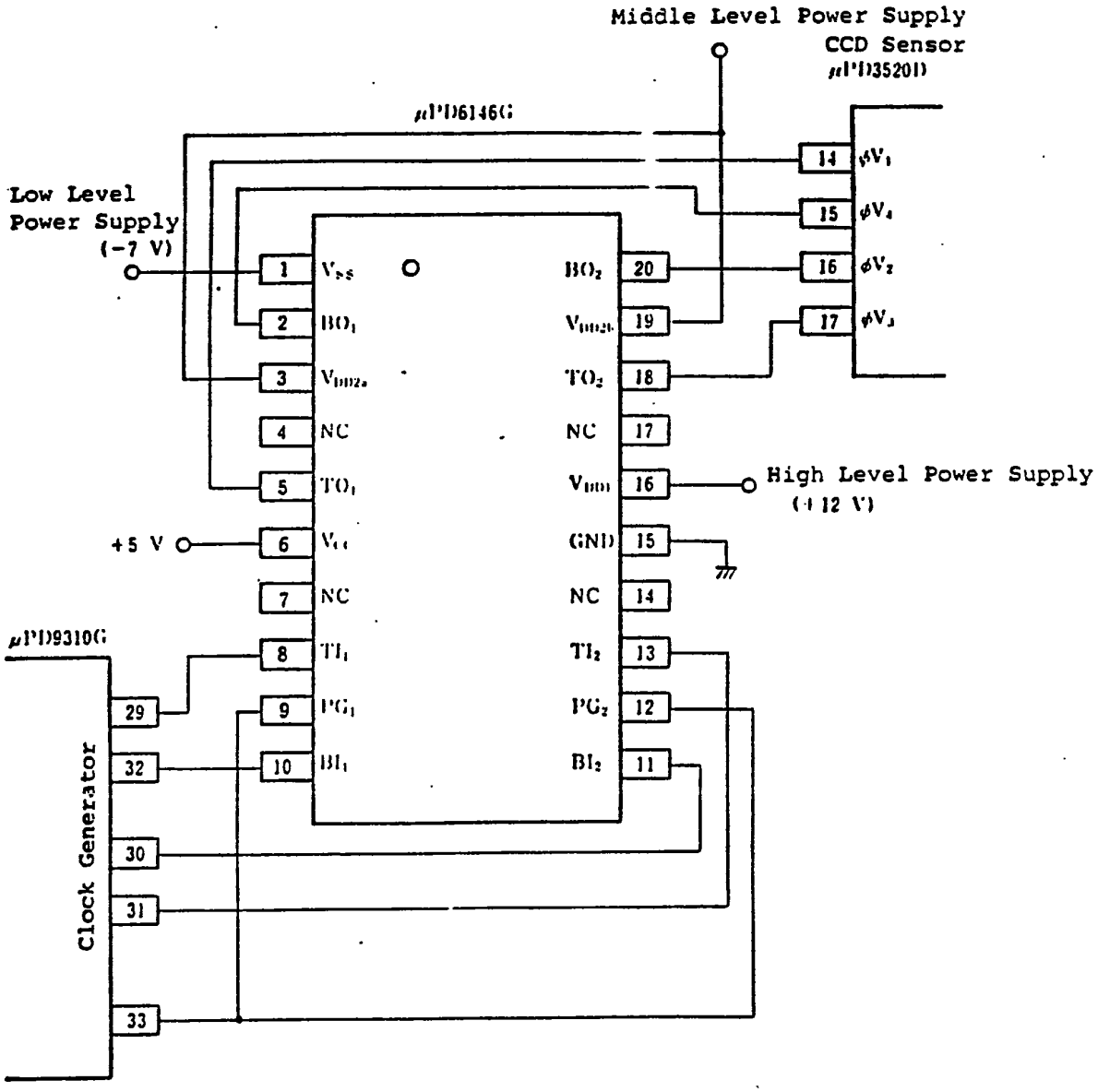


MC-5573 CLOCK TIMING

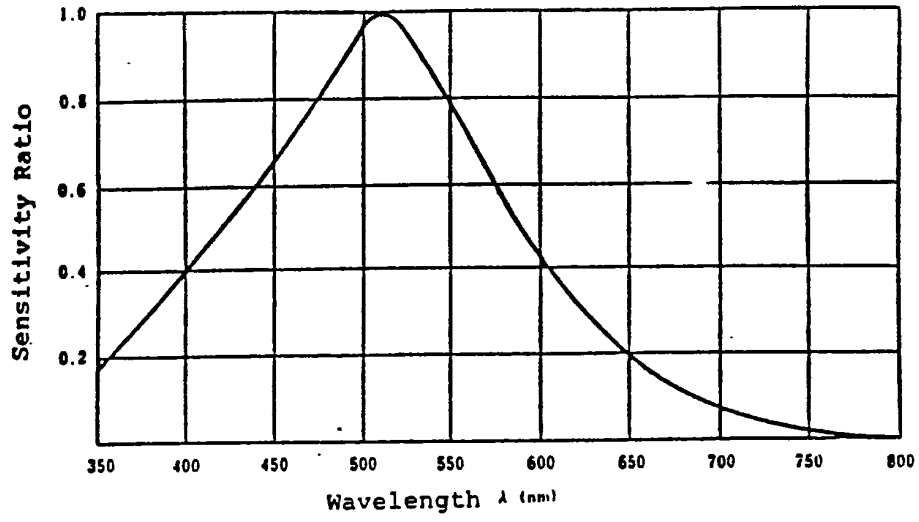
Horizontal: 20 ns/div



ϕ_V DRIVING INTERFACE

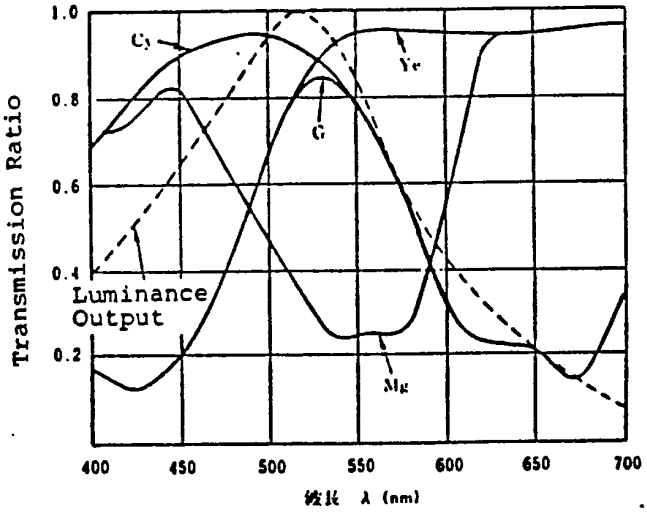


Luminance Spectrum Sensitivity
(IR Cut, C-500 of 1 mm in thickness is used)

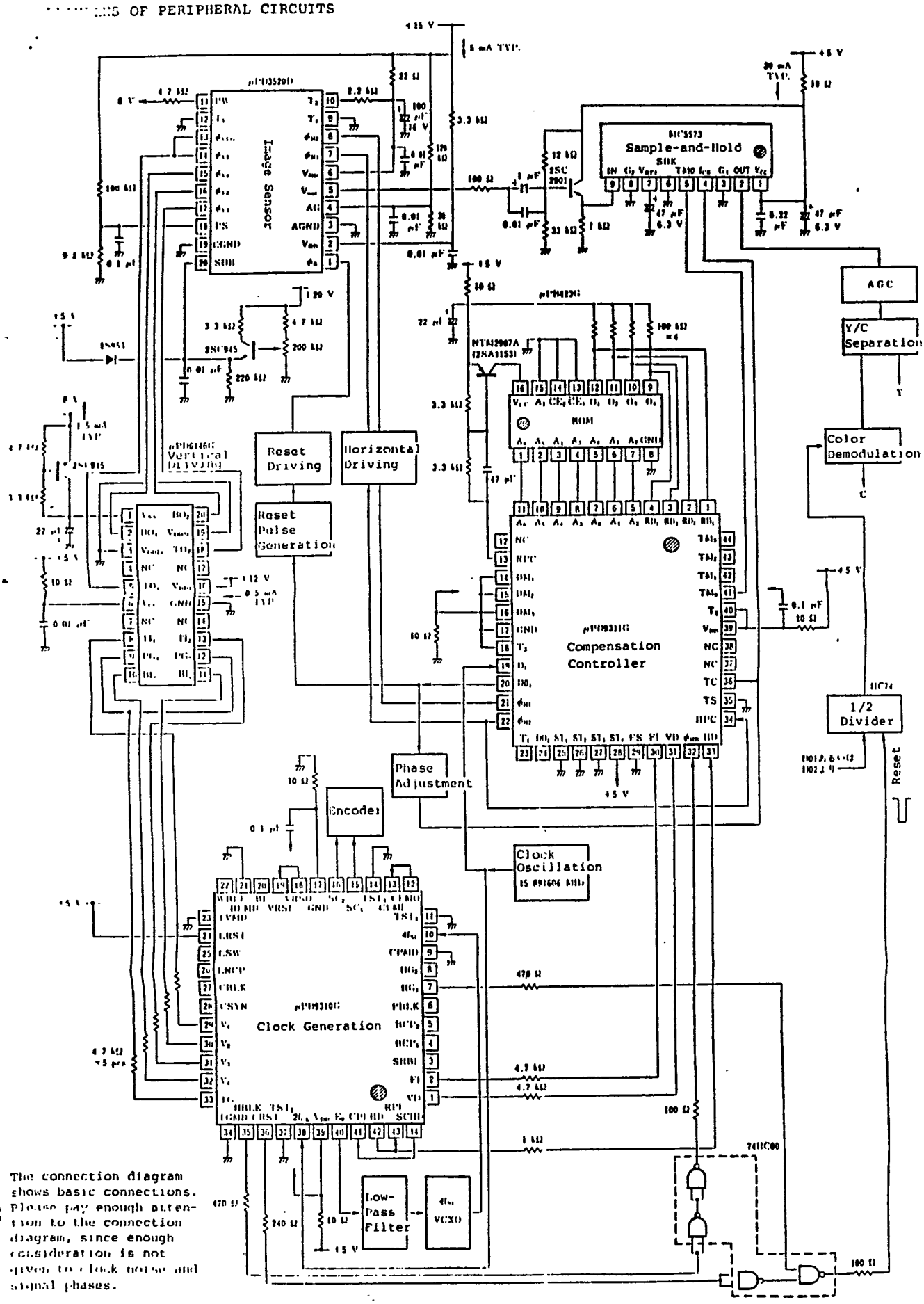


Ultraviolet	Visible	Infrared

Color Filter Spectrum Characteristics

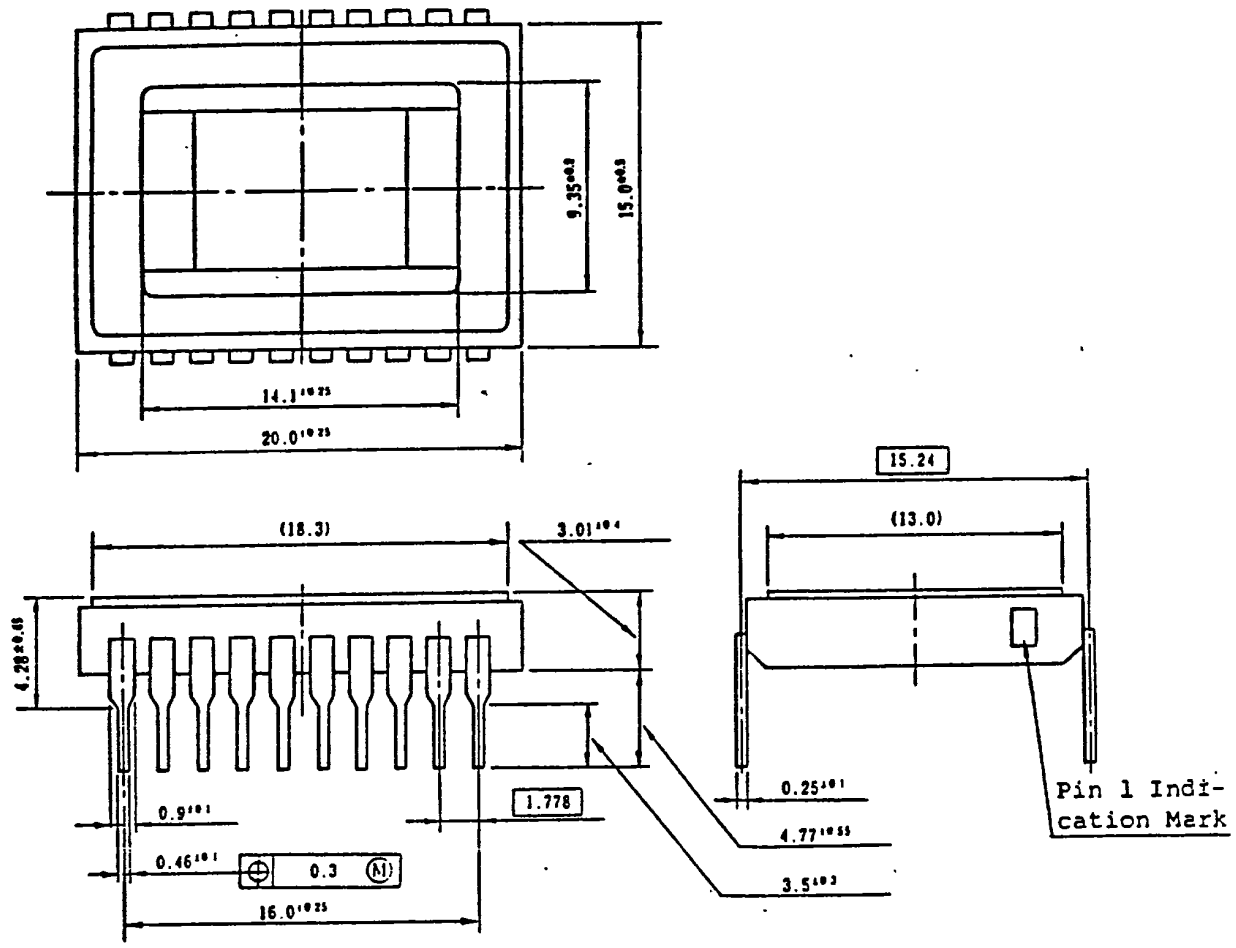


Blue-violet	Blue	Green	Yellow	Red

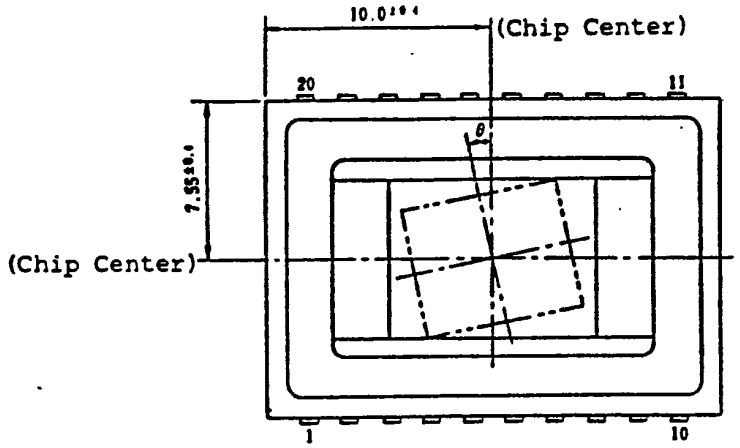


The connection diagram shows basic connections. Please pay enough attention to the connection diagram, since enough consideration is not given to clock noise and signal phases.

EXTERNAL DIMENSION DIAGRAM UNIT: mm

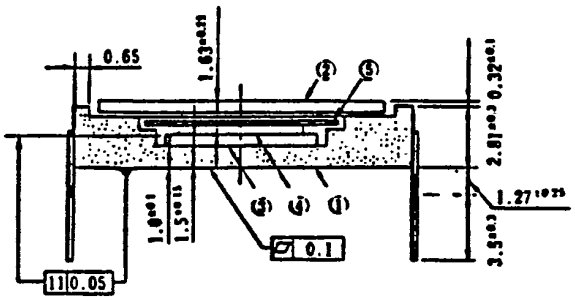


CHIP POSITION DIAGRAM UNIT: mm



Chip inclination θ	$\pm 2^{\circ}$
Chip size	8.00 x 6.47
Image size	1/2 inch (6.4 x 4.8)

SECTIONAL VIEW UNIT: mm



①	Package
②	Shield glass
③	Chip
④	Color separation filter
⑤	Douser

Part Name	Required Size	Remarks
Glass	$0.7^{\pm 0.05}$	Refractire index 1.5
Filter	$0.5^{\pm 0.1}$	Refractire index 1.5