HMCS402 Series/ HMCS404 Series/ HMCS408 Series

Description

The HMCS402/404/408 Series are HMCS400 series CMOS 4-bit single-chip microcomputers. Each device incorporates a ROM, RAM, I/O, serial interface, two timer/counters, and high-voltage I/O pins including high-current output pins to directly drive fluorescent display tubes.

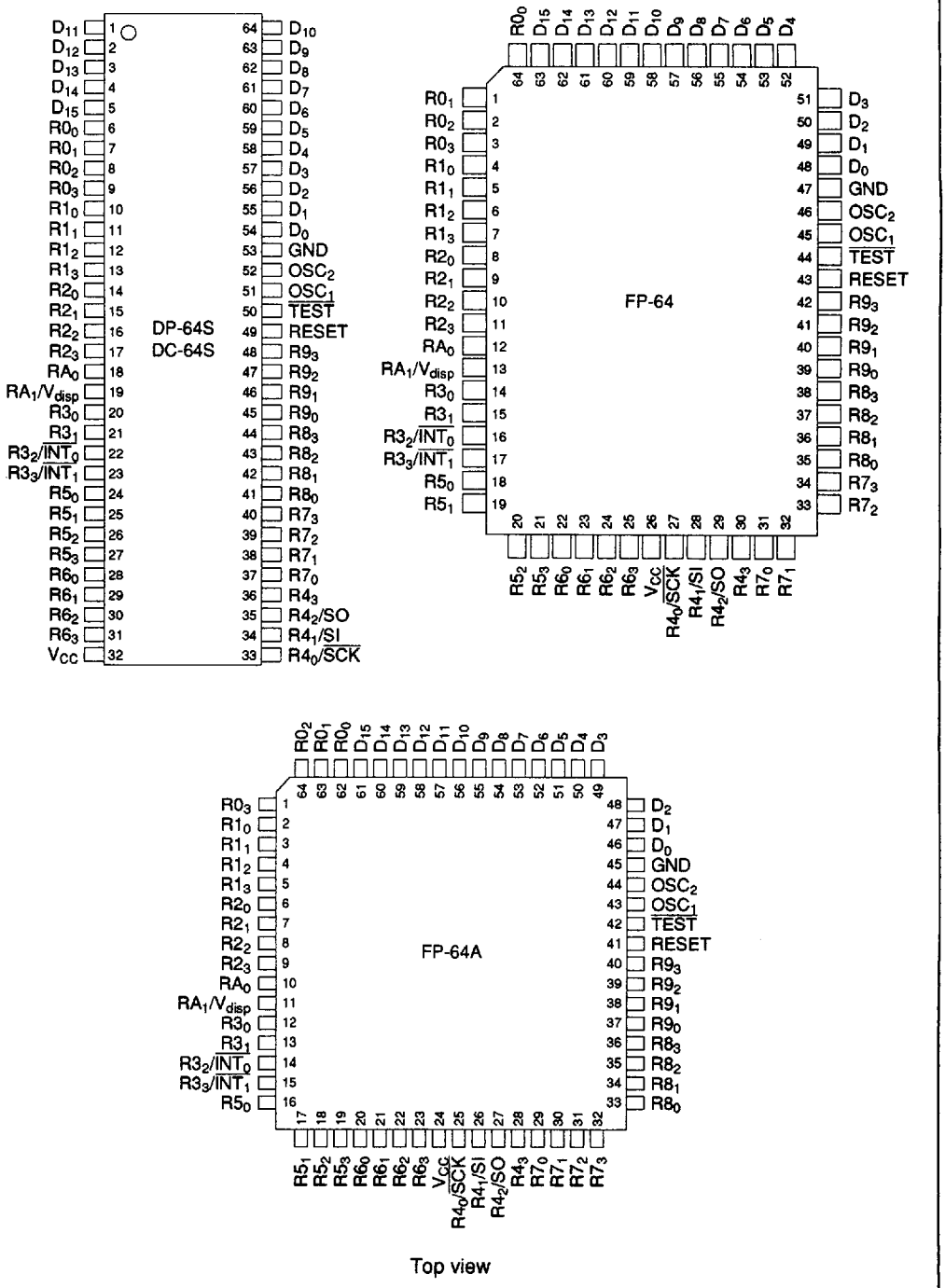
Features

- 2048-word × 10-bit ROM (HMCS402)
  4096-word × 10-bit ROM (HMCS404)
  8192-word × 10-bit ROM (HMCS408)
- 160-digit × 4-bit RAM (HMCS402)
  256-digit × 4-bit RAM (HMCS404)
  512-digit × 4-bit RAM (HMCS408)
- 58 I/O pins, including 26 high-voltage I/O pins (V_{CC}–40 V max.)
- Two timer/counters
  — 8-bit free-running timer
  — 8-bit auto-reload timer/event counter
- Clock-synchronous 8-bit serial interface
- Five interrupt sources
  — Two by external sources
  — Two by timer/counters
  — One by serial interface
- Subroutine stack up to 16 levels, including interrupts
- Low-power dissipation modes
  — Standby mode
  — Stop mode
- On-chip oscillator
  — Crystal or ceramic oscillator (an external clock also possible)
  — Resistor (HMCS402C/HMCS404C)
- C-type: 5-V operation version
  CL-type: 3-V operation version
  AC-type: high-speed operation version
- Package
  — 64-pin shrink dual-inline plastic package
  — 64-pin flat plastic package
- ZTAT™ versions
  (HD4074008, HD4074019)

Ordering Information

Series Name	Product Name	Model Name	Package
HMCS402	HMCS402C	HD614023S	DP-64S
		HD614023F	FP-64
	HMCS402CL	HD614026S	DP-64S
		HD614026F	FP-64
	HMCS402AC	HD614029S	DP-64S
		HD614029F	FP-64
HMCS404	HMCS404C	HD614043S	DP-64S
		HD614043F	FP-64
	HMCS404CL	HD614046S	DP-64S
		HD614046F	FP-64
	HMCS404AC	HD614049S	DP-64S
		HD614049F	FP-64
HMCS408	HMCS408C	HD614081S	DP-64S
		HD614081F	FP-64
		HD614081H	FP-64A
	HMCS408CL	HD614086S	DP-64S
		HD614086F	FP-64
		HD614086H	FP-64A
	HMCS408AC	HD614089S	DP-64S
		HD614089F	FP-64
		HD614089H	FP-64A

Pin Arrangement



Pin Functions

GND, V_{CC}, V_{disp} (Power): These are the power supply pins for the MCU. Connect GND to ground (0 V) and apply the V_{CC} power supply voltage to the V_{CC} pin. The V_{disp} pin (multiplexed with RA_1) is a power supply for high-voltage I/O pins with a maximum voltage of 40 V (V_{CC} – 40 V). For details, see the Input/Output section.

$\overline{TEST}$ (Test): $\overline{TEST}$ is for test purposes only. Connect it to V_{CC}.

RESET (Reset): RESET resets the MCU. For details, see the Reset section.

OSC_1, OSC_2 (Oscillator Connections): OSC_1 and OSC_2 are input pins for the internal oscillator circuit. They can be connected to a crystal, ceramic, or external oscillator circuits. For details, see the Internal Oscillator Circuit section.

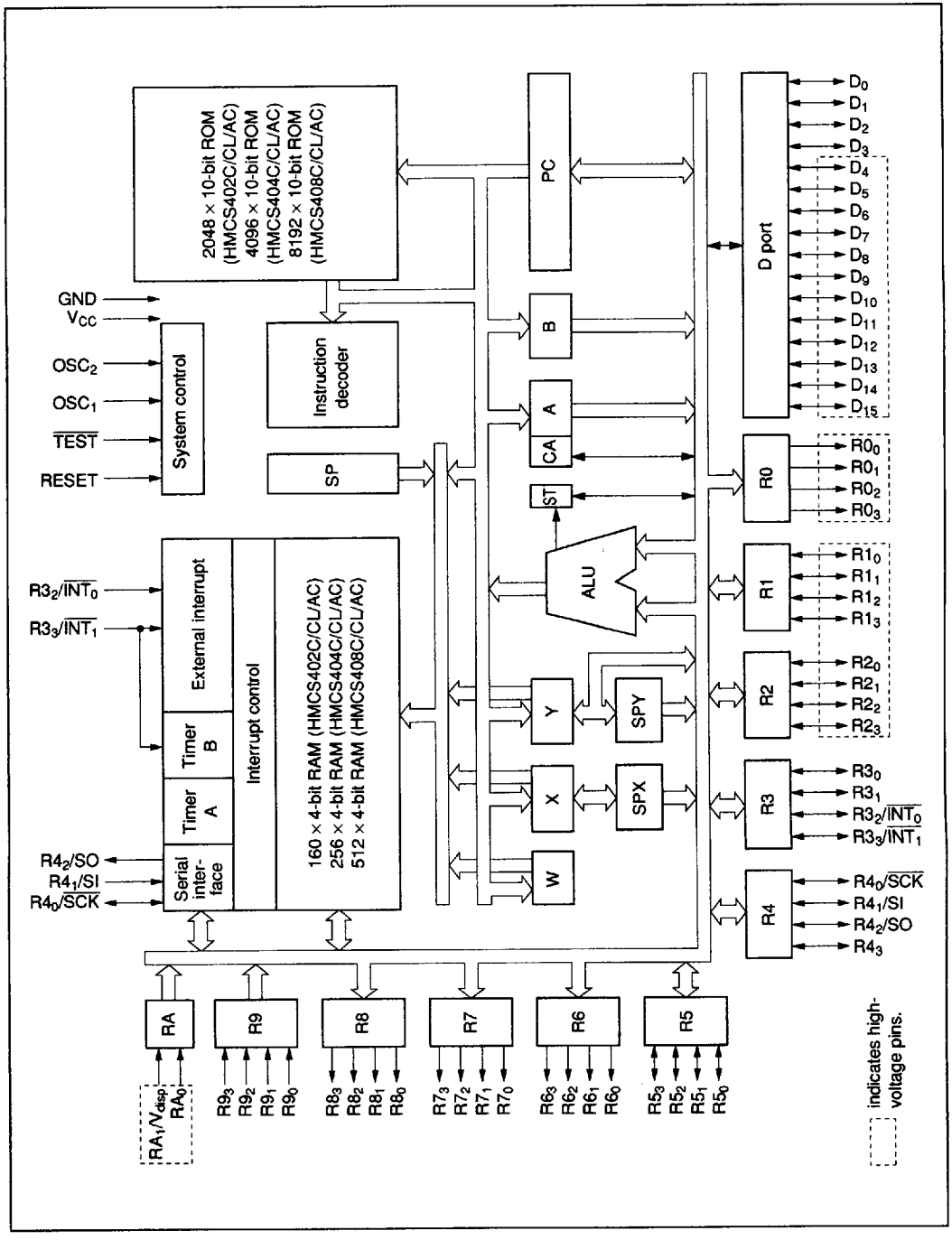
D_0 to D_{15} (D Port): The D port is an input/output port addressed by its bits. These 16 pins are all input/output pins. D_0 to D_3 are standard, and D_4 to D_{15} are high-voltage pins. The circuit type for each pin can be selected using a mask option. For details, see the Input/Output section.

$R0_0$ to $R0_3$, $R1_0$ to $R1_3$, $R2_0$ to $R2_3$, $R3_0$ to $R3_3$, $R4_0$ to $R4_3$, $R5_0$ to $R5_3$, $R6_0$ to $R6_3$, $R7_0$ to $R7_3$, $R8_0$ to $R8_3$, $R9_0$ to $R9_3$, RA_0, RA_1 (R Ports): R0 to R9 are 4-bit I/O ports. RA is a 2-bit port. R0, R6, R7, and R8 are output ports, R9 and RA are input ports, and R1 to R5 are I/O ports. R0, R1, R2, and RA are high-voltage ports, and R3 to R9 are standard ports. Each pin has a mask option which selects its circuit type. The pins $R3_2$, $R3_3$, $R4_0$, $R4_1$, and $R4_2$ are multiplexed with $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI, and SO, respectively. For details, see the Input/Output section.

$\overline{INT_0}$, $\overline{INT_1}$ (Interrupts): $\overline{INT_0}$ and $\overline{INT_1}$ are external interrupts for the MCU. $\overline{INT_1}$ can be used as an external event input pin for timer B. $\overline{INT_0}$ and INT_1 are multiplexed with $R3_2$ and $R3_3$, respectively. For details, see Interrupt section.

$\overline{SCK}$, SI, SO (Serial Interface): The transmit clock I/O pin ($\overline{SCK}$), serial data input pin (SI), and serial data output pin (SO) are used for serial interface. $\overline{SCK}$, SI, and SO are multiplexed with $R4_0$, $R4_1$, and $R4_2$, respectively. For details, see the Serial Interface section.

Block Diagram



Memory Map

ROM Memory Map

The MCU includes the following ROM size shown in table 1. The ROM is described in the following paragraphs with the ROM memory map shown in figure 1.

Vector Address Area ($0000 to $000F): Locations $0000 through $000F are reserved for JMPL instructions to branch to the starting address of the initialization program and of the interrupt programs. After reset or an interrupt, the program is executed from the vector address.

Zero-Page Subroutine Area ($0000 to $003F): Locations $0000 through $003F are reserved for subroutines. The CAL instruction branches to subroutines.

Pattern Area $0000 to $07FF (HMCS402C/CL/AC); $0000 to $0FFF (HMCS404C/CL/AC, HMCS408C/CL/AC): These locations are reserved for ROM data. The P instruction allows reference to ROM data as a pattern.

Program Area $0000 to $07FF (HMCS402C/CL/AC); $0000 to $0FFF (HMCS404C/CL/AC); $0000 to $1FFF (HMCS408C/CL/AC): These locations can be used for program code.

Table 1 ROM Size

Series Name	ROM Size
HMCS402C/CL/AC	2048-word × 10-bit
HMCS404C/CL/AC	4096-word × 10-bit
HMCS408C/CL/AC	8192-word × 10-bit

Table 2 RAM Size

Series Name	RAM Size
HMCS402C/CL/AC	160-digit × 4-bit
HMCS404C/CL/AC	256-digit × 4-bit
HMCS408C/CL/AC	512-digit × 4-bit

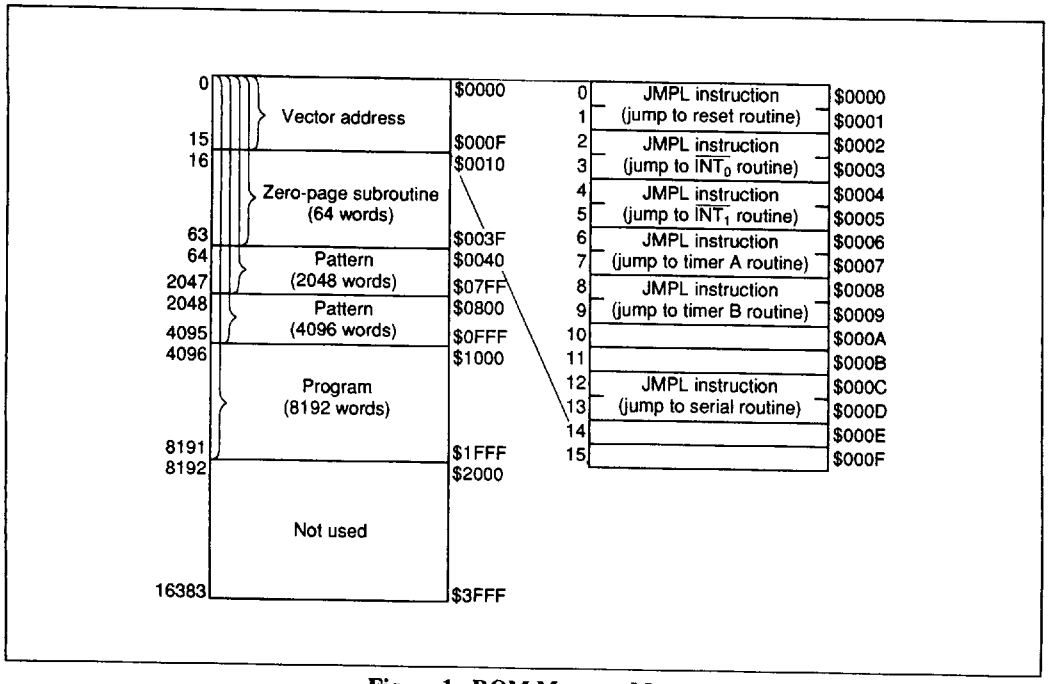


Figure 1 ROM Memory Map

RAM Memory Map

The MCU also contains the following RAM size shown in table 2 as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bits Area ($000 to $003): The interrupt control bits area (figure 3) is used for interrupt control. It is accessible only by RAM bit manipulation instructions. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area ($004 to $00B): The special function registers are the mode or data registers for the external interrupt, the serial interface, and the timer/counters. These registers are classified into three types: write-only, read-only, and read/write, as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions.

Data Area (HMCS402C/CL/AC: $020 to $07F, HMCS404C/CL/AC: $020 to $0DF, HMCS408C/CL/AC: $020 to $1DF): The 16 digits of $020 through $02F are called memory registers (MR) and are accessible by the LAMR and XMRA instructions (figure 4).

Stack Area ($3C0 to $3FF): Locations $3C0 through $3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status flag (ST), and carry flag (CA) when subroutine calls (CAL or CALL instruction) and interrupts are processed. This area can be used as a 16-level nesting stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by the RTN and RTNI instructions. Status and carry flags are restored only by the RTNI instruction. This area, when not used as a stack, is available as a data area.

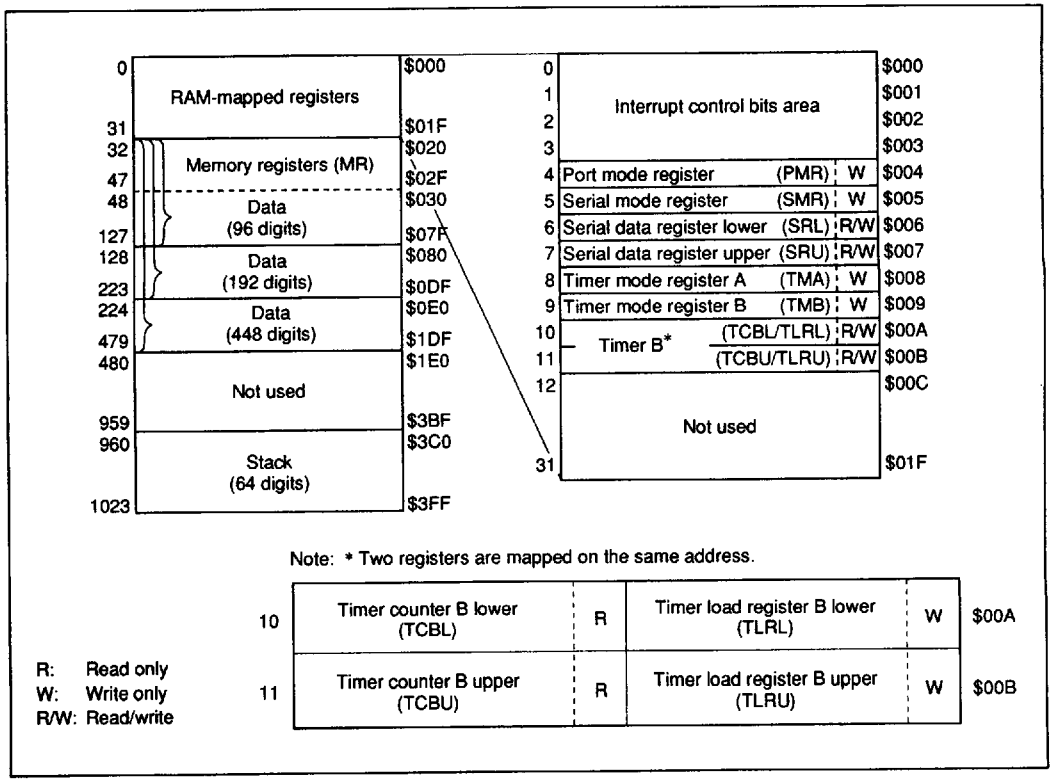


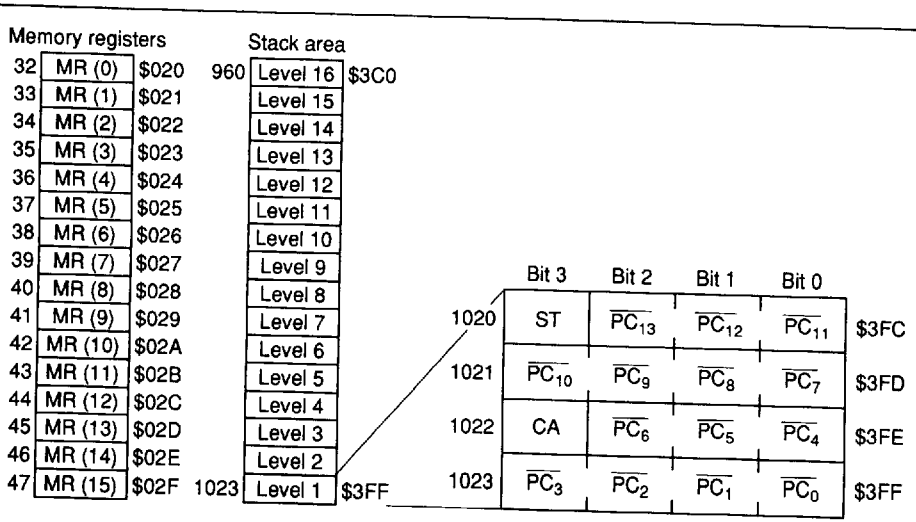
Figure 2 RAM Memory Map

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)	$000
1	IMTA (IM of timer A)	IFTA (IF of timer A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	Not used	Not used	IMTB (IM of timer B)	IFTB (IF of timer B)	$002
3	Not used	Not used	IMS (IM of serial)	IFS (IF of serial)	$003

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Note: Each bit of the interrupt control bits area is set by the SEM/SEMD instruction, reset by the REM/REMD instruction, and tested by the TM/TMD instruction. It is not affected by other instructions. Furthermore, the interrupt request flag is not affected by the SEM/SEMD instruction.
The value of the status flag becomes invalid when unusable bits are tested and the RSP bit is tested by the TM or TMD instruction.

Figure 3 Configuration of Interrupt Control Bits Area



PC_{13} to PC_0: Program counter
ST: Status flag
CA: Carry flag

Notes: 1. Since HMCS402C/CL/AC have 2-k ROM, PC_{11}, PC_{12} and PC_{13} are not used.
2. Since HMCS404C/CL/AC have 4-k ROM, PC_{12} and PC_{13} are not used.
3. Since HMCS408C/CL/AC have 8-k ROM, PC_{13} is not used.

Figure 4 Configuration of Memory Registers, Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for the CPU operations (figure 5).

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results of the arithmetic logic unit (ALU), and transfer data to/from memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The W register is a 2-bit write-only register, and the X and Y registers are 4-bit registers used for indirect addressing of RAM. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY are used to assist the X and Y registers, respectively.

Carry Flag (CA): The carry flag (CA) stores the overflow from the ALU generated by an arithmetic operation. It is also affected by the SEC, REC, ROTL, and ROTR instructions.

During an interrupt, the carry is pushed onto the stack. It is restored by the RTNI instruction, but not by the RTN instruction.

Status Flag (ST): The status flag (ST) holds the ALU overflow, non-zero, and the results of a bit test instruction for the arithmetic or compare instruction. It is a branch condition of the BR, BRL, CAL, or CALL instruction. The value of the status flag remains unchanged until the next arithmetic, compare, or bit test instruction is executed. The status flag becomes a 1 after the BR, BRL, CAL, or CALL instruction is either executed or skipped. During an interrupt, the status flag is pushed onto the stack and restored back from the stack by the RTNI instruction, but not by the RTN instruction.

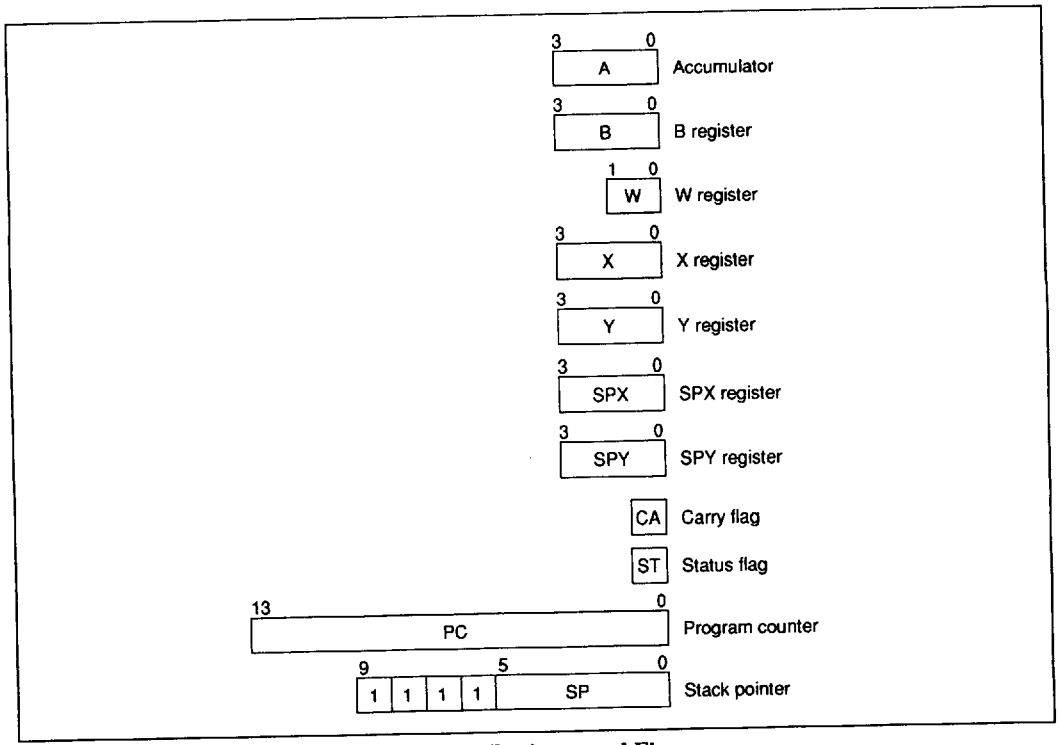


Figure 5 Registers and Flags

Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) is used to point to the address of the next stacking area (up to 16 levels).

The stack pointer is initialized to RAM address $3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels deep because the upper 4 bits of the stack pointer are fixed at 1111.

The stack pointer is initialized to $3FF either by MCU reset or by the RSP bit reset from the REM/REMD instruction.

Interrupts

Five interrupt sources are available on the MCU: external requests ($\overline{INT_0}$, $\overline{INT_1}$), timer/counters (timers A and B), and the serial interface. For each source, an interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control interrupt operations.

Interrupt Control Bits and Interrupt Processing: The interrupt control bits are mapped on $000 through $003 of the RAM space. They are accessible by RAM bit manipulation instructions. The interrupt request flag (IF) cannot be set by software. The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 3 shows the interrupt priority and vector addresses, and table 4 shows the interrupt conditions corresponding to each interrupt source.

Table 3 Vector Addresses and Interrupt Priority

Reset/Interrupt	Priority	Vector Addresses
RESET	—	$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
Timer A	3	$0006
Timer B	4	$0008
Serial	5	$000C

Table 4 Interrupt Conditions

	Interrupt Source				
Interrupt Control Bit	$\overline{INT_0}$	$\overline{INT_1}$	Timer A	Timer B	Serial
IE	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0
IFTA · $\overline{IMTA}$	*	*	1	0	0
IFTB · $\overline{IMTB}$	*	*	*	1	0
IFS · $\overline{IMS}$	*	*	*	*	1

Note: * Don't care

The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt source.

Figure 7 shows the interrupt processing sequence, and figure 8 shows the interrupt processing flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry flag, status flag, and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after jumping to the vector address.

At each vector address, program the JMPL instruction to branch to the starting address of the interrupt program. The IF which caused the interrupt must be reset by software in the interrupt program.

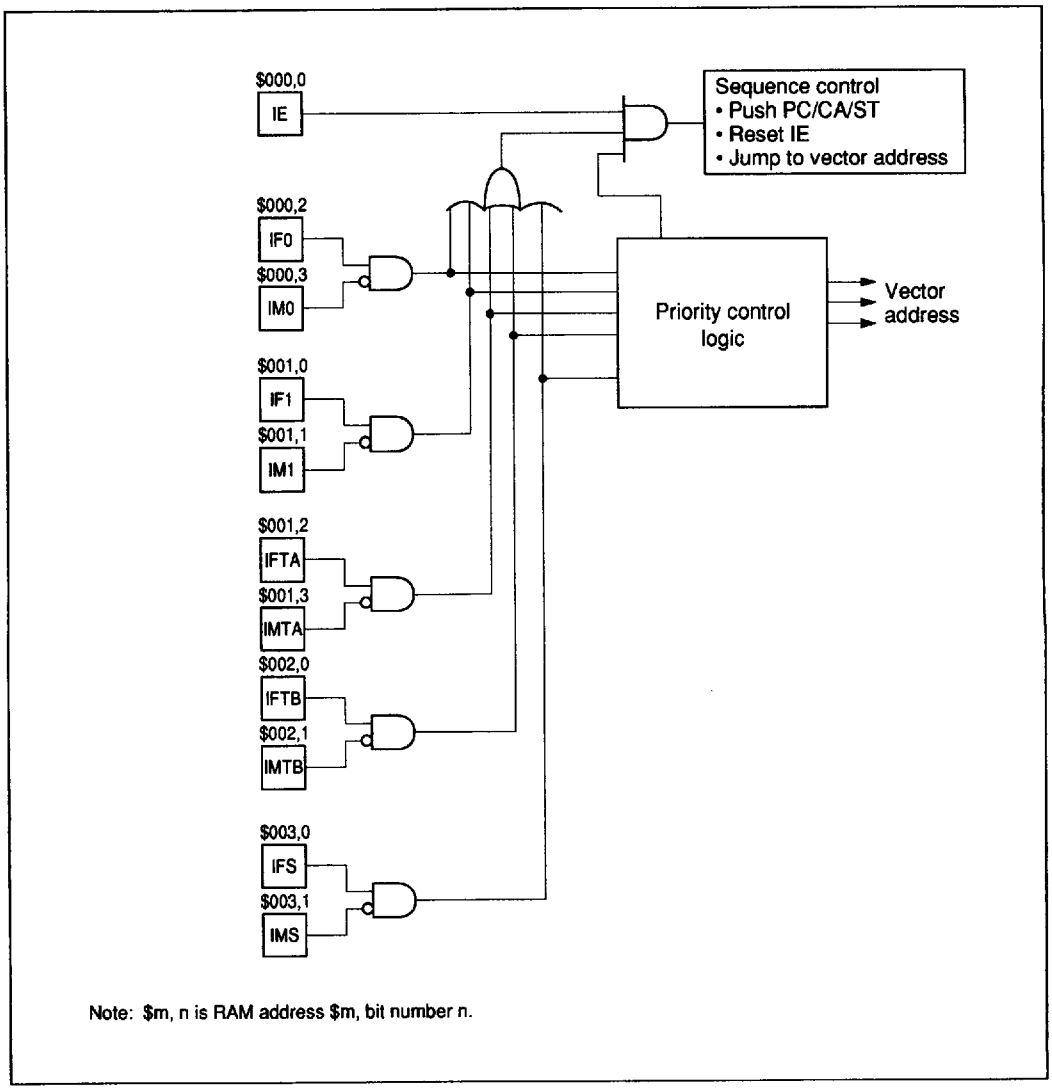


Figure 6 Interrupt Control Circuit Block Diagram

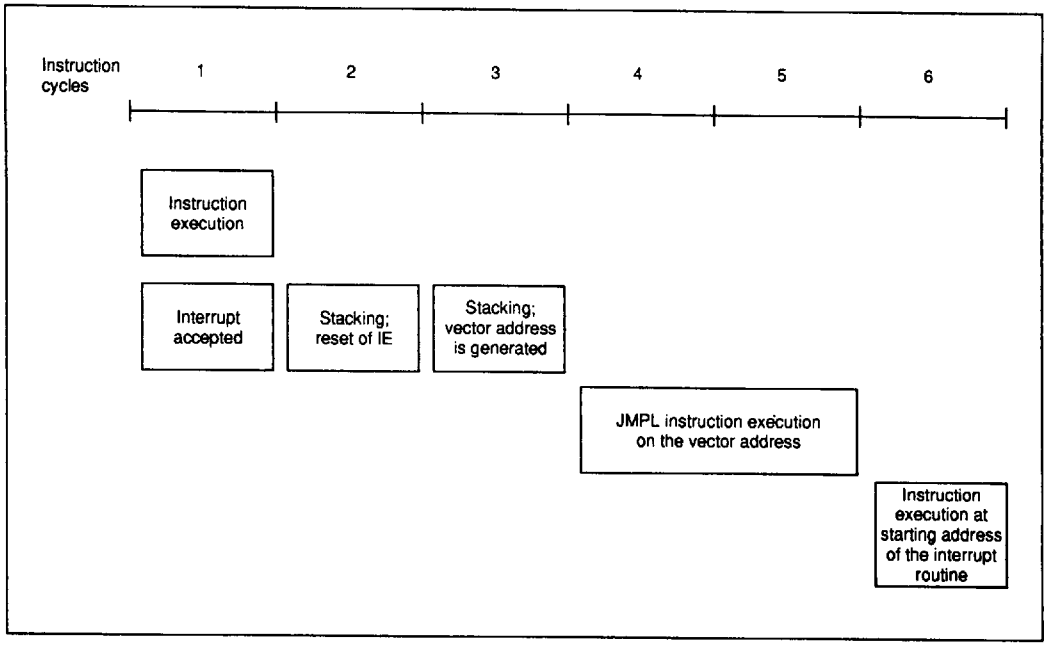


Figure 7 Interrupt Processing Sequence

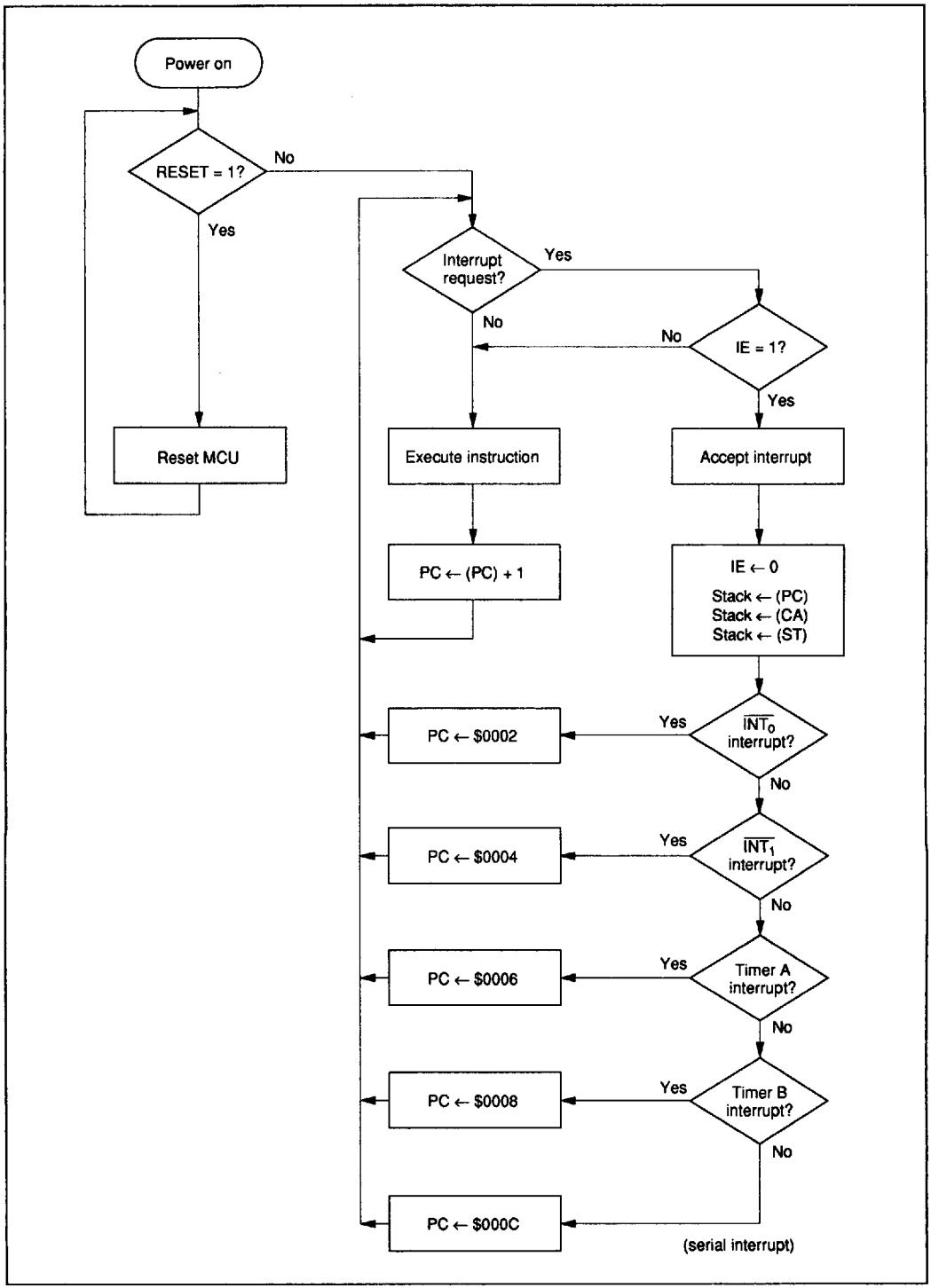


Figure 8 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 5. It is reset by an interrupt and set by the RTNI instruction.

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): The external interrupt request inputs ($\overline{INT_0}$, $\overline{INT_1}$) can be selected by the port mode register (PMR: $004). Setting bit 3 and bit 2 of PMR causes the $R3_3/\overline{INT_1}$ and $R3_2/\overline{INT_0}$ pins to be used as $\overline{INT_1}$ and $\overline{INT_0}$, respectively.

The external interrupt request flags (IF0, IF1) are set at the falling edge of $\overline{INT_0}$ and $\overline{INT_1}$ inputs. (Refer to table 6.)

The $\overline{INT_1}$ input can be used as a clock signal input to timer B, in which timer B counts up at each falling edge of the $\overline{INT_1}$ input. When using $\overline{INT_1}$ as the timer B external event input, the external interrupt mask (IM1) has to be set so that the interrupt request by $\overline{INT_1}$ will not be accepted. (Refer to table 7.)

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the $\overline{INT_0}$ and $\overline{INT_1}$ inputs, respectively.

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: $004): The port mode register is a 4-bit write-only register which controls the $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$, $R4_1$/SI, and $R4_2$/SO pins as shown in table 8. The port mode register will be initialized to $0 by MCU reset. These pins are therefore initially used as ports.

Table 5 Interrupt Enable Flag

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

Table 6 External Interrupt Request Flags

IF0, IF1	Interrupt Requests
0	No
1	Yes

Table 7 External Interrupt Masks

IM0, IM1	Interrupt Requests
0	Enabled
1	Disabled (masked)

Table 8 Port Mode Register

PMR3	$R3_3/\overline{INT_1}$ Pin
0	Used as $R3_3$ port input/output pin
1	Used as $\overline{INT_1}$ input pin

PMR2	$R3_2/\overline{INT_0}$ Pin
0	Used as $R3_2$ port input/output pin
1	Used as $\overline{INT_0}$ input pin

PMR1	$R4_1$/SI Pin
0	Used as $R4_1$ port input/output pin
1	Used as SI input pin

PMR0	$R4_2$/SO Pin
0	Used as $R4_2$ port input/output pin
1	Used as SO output pin

Serial Interface

The serial interface is used to transmit/receive 8-bit data serially. This consists of the serial data register, the serial mode register, the octal counter, and the multiplexer as illustrated in figure 9. Pin $R4_0/\overline{SCK}$ and the transmit clock signal are controlled by the serial mode register. The contents of the serial data register can be written into or read out by software. The data in the serial data register can be shifted synchronously with the transmit clock signal.

The STS instruction is used to initiate serial interface operations and to reset the octal counter to $0. The counter starts to count at the falling edge of the transmit clock signal ($\overline{SCK}$) and increments by one at the rising edge of $\overline{SCK}$. When the octal counter is reset to $0 after eight transmit clock signals, or when a transmit/receive operation is discontinued by resetting the octal counter, the serial interrupt request flag will be set.

Serial Mode Register (SMR: $005): The 4-bit write-only serial mode register controls $R4_0/\overline{SCK}$, the prescaler divide ratio, and the transmit clock source as shown in table 9.

The write signal to the serial mode register controls the operating state of the serial interface.

The write signal to the serial mode register stops the serial data register and octal counter from applying the transmit clock, and it also resets the octal counter to $0 simultaneously. Therefore, when the serial interface is in the transfer state, the write signal causes the serial mode register to cease the data transfer and to set the serial interrupt request flag.

The contents of the serial mode register will be changed on the second instruction cycle after writing into the serial mode register. Therefore, it will be necessary to execute the STS instruction after the data in the serial mode register has been changed completely. The serial mode register will be reset to $0 by MCU reset.

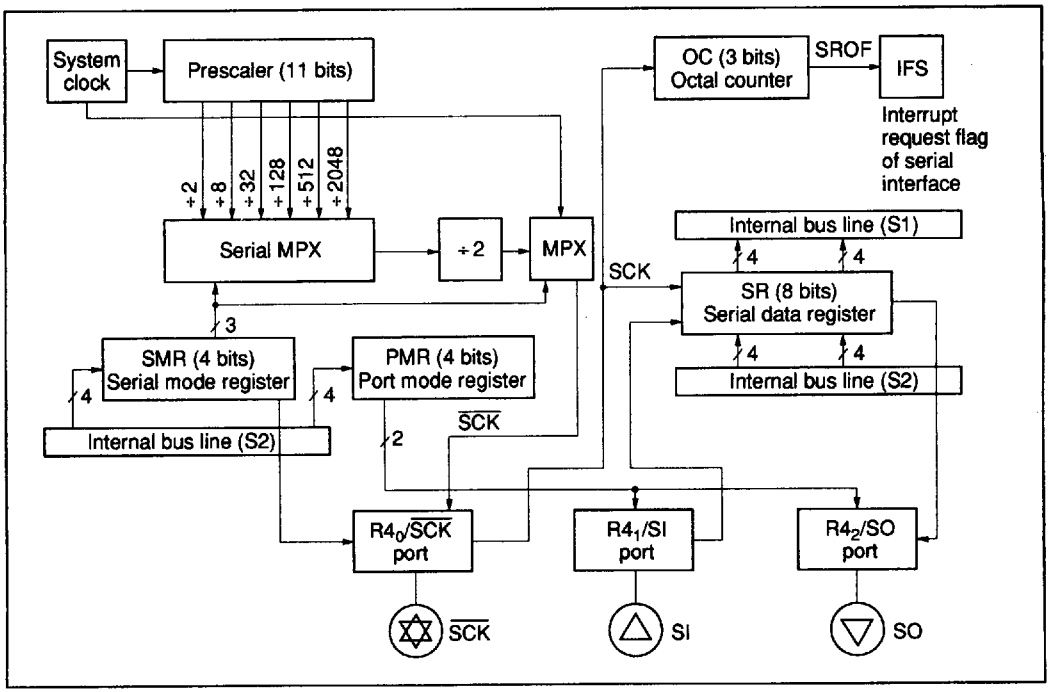


Figure 9 Serial Interface Block Diagram

Serial Data Register (SDR: $006, SRU: $007): The 8-bit read/write serial data register consists of a low-order digit (SRL: $006) and a high-order digit (SRU: $007).

The data in the serial data register will be output from the SO pin, from LSB to MSB, synchronously with the falling edge of the transmit clock signal. At the same time, external data will be input from the SI pin to the serial data register, to MSB first, synchronously with the rising edge of the transmit clock. Figure 10 shows the I/O timing chart for the transmit clock signal and the data.

The read/write operations of the serial data register should be performed after the completion of data transmit/receive. Otherwise the data may not be guaranteed.

Table 9 Serial Mode Register

SMR3	$R4_0/\overline{SCK}$
0	Used as $R4_0$ port input/output pin
1	Used as $\overline{SCK}$ input/output pin

				Transmit Clock		
SMR2	SMR1	SMR0	$R4_0/\overline{SCK}$ Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	$\overline{SCK}$ output	Prescaler	÷ 2048	÷ 4096
0	0	1	$\overline{SCK}$ output	Prescaler	÷ 512	÷ 1024
0	1	0	$\overline{SCK}$ output	Prescaler	÷ 128	÷ 256
0	1	1	$\overline{SCK}$ output	Prescaler	÷ 32	÷ 64
1	0	0	$\overline{SCK}$ output	Prescaler	÷ 8	÷ 16
1	0	1	$\overline{SCK}$ output	Prescaler	÷ 2	÷ 4
1	1	0	$\overline{SCK}$ output	System clock	—	÷ 1
1	1	1	$\overline{SCK}$ input	External clock	—	—

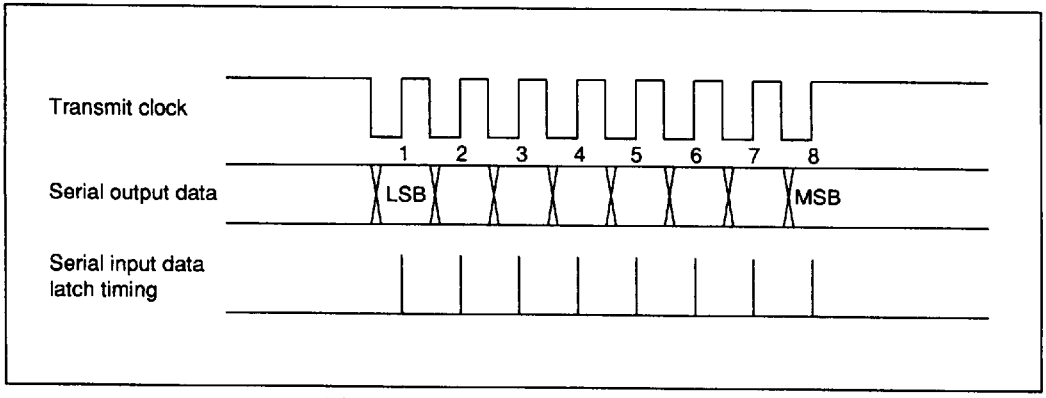


Figure 10 Serial Interface I/O Timing

Serial Interrupt Request Flag (IFS: $003, Bit 0): The serial interrupt request flag will be set when the octal counter counts eight transmit clock signals, or when data transfer is discontinued by resetting the octal counter. Refer to table 10.

Serial Interrupt Mask (IMS: $003, Bit 1): The serial interrupt mask masks the interrupt request. Refer to table 11.

Selection and Change of the Operation Mode: Table 12 shows the serial interface operation modes which are determined by a combination of the value in the port mode register and that in the serial mode register. Initialize the serial interface by the write signal to the serial mode register, when the operation mode is changed.

Operating State of Serial Interface: The serial interface has three operating states: the STS waiting state, transmit clock wait state, and transfer state, as shown in figure 11.

The STS waiting state is the initialization state of the serial interface internal state. The serial interface enters this state in one of two ways: either by changing the operation mode through a data change in the port mode register, or by writing data into the serial mode register. In this state, the serial interface does not operate even if the transmit clock is applied. If the STS instruction is executed, the serial interface shifts to transmit clock wait state.

In this state the falling edge of the first transmit clock causes the serial interface to shift to transfer state, initializing the octal counter to count up and the serial data register to shift simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in transmit clock wait state while the transmit clock outputs continuously.

The octal counter becomes 000 again after 8 transmit clocks or by the execution of the STS instruction, so that the serial interface returns to transmit clock wait state, and the serial interrupt request flag is set simultaneously.

When the internal transmit clock is selected, the transmit clock output is triggered by the execution of the STS instruction, and stops after 8 clocks.

Example of Transmit Clock Error Detection: The serial interface functions abnormally when the transmit clock is disturbed by external noise. In this case, transmit clock error can be detected by the procedure shown in figure 12.

If more than 8 transmit clocks are applied in the transmit clock wait state, the state of the serial interface shifts in the following sequence: transfer state, transmit clock wait state, and transfer state. The serial interrupt flag should be reset before entering into the STS state by writing data to SMR. This procedure causes the serial interface request flag to be set again.

Table 10 Serial Interrupt Request Flag

IFS	Interrupt Request
0	No
1	Yes

Table 11 Serial Interrupt Mask

IMS	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 12 Serial Interface Operation Mode

SMR3	PMR1	PMR2	Serial Interface Operating Mode
1	0	0	Clock continuous output mode
1	0	1	Transmit mode
1	1	0	Receive mode
1	1	1	Transmit/receive mode

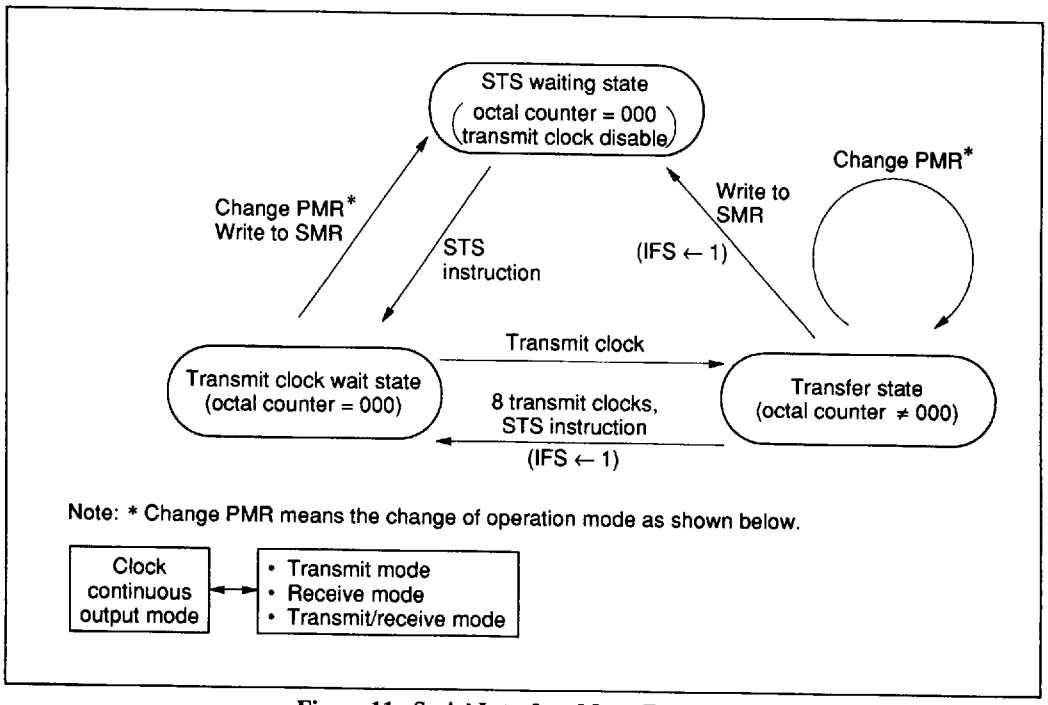


Figure 11 Serial Interface Mode Transition

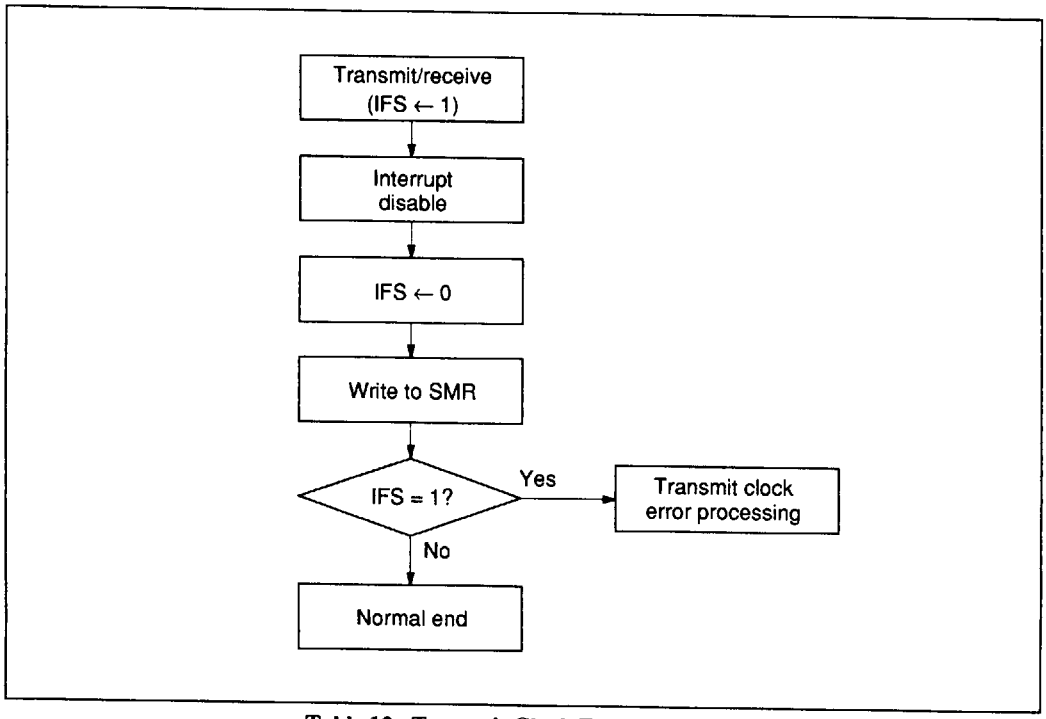


Table 12 Transmit Clock Error Detection

Timers

The MCU contains a prescaler and two timer/counters (timers A and B) (figure 13) whose functions are the same as the HMCS404C's. The prescaler is an 11-bit binary counter, timer A is an 8-bit free running timer, and timer B is an 8-bit auto-reload timer/event counter.

Prescaler: The input to the prescaler is a system clock signal. The prescaler is initialized to $000 by MCU reset, and it starts to count up the system clock signal as soon as RESET input goes to logic 0. The prescaler keeps counting up except at MCU reset and stop mode. The prescaler provides clock signals to timer A, timer B, and the serial interface. The prescaler divide ratio is selected by timer mode register A (TMA), timer mode register B (TMB), and serial mode register (SMR).

Timer A Operation: After timer A is initialized to $00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after timer A is counted up to $FF, timer A is set to $00 again and an overflow output is generated. This leads to setting the timer A interrupt request flag (IFTA: $001, bit 2) to 1. Therefore, this timer can function as an interval timer which periodically generates overflow output at every 256th clock signal input.

The clock input signals to timer A are selected by timer mode register A (TMA: $008).

Timer B Operation: Timer mode register B (TMB: $009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select $R3_3/\overline{INT_1}$ as $\overline{INT_1}$ and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

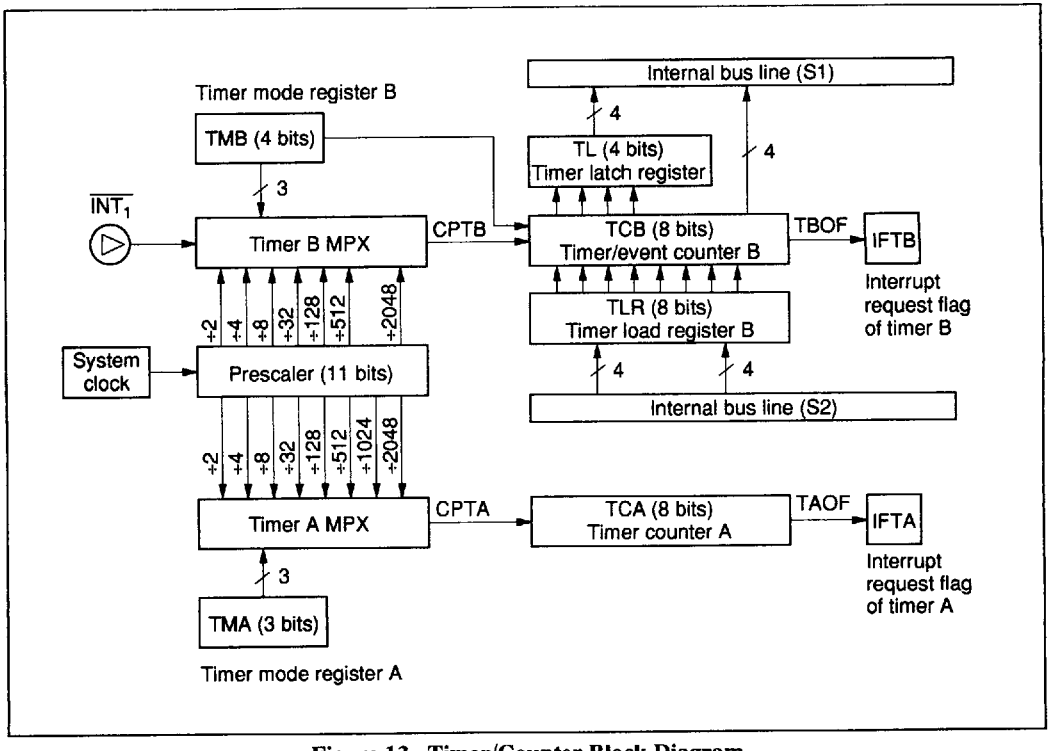


Figure 13 Timer/Counter Block Diagram

Timer B is initialized according to the data written into timer load register B by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to $FF, it will generate an overflow output. In this case, if the auto-reload function is selected, timer B is initialized according to the value of timer load register B. If it is not selected, timer B goes to $00. The timer B interrupt request flag (IFTB: $002, bit 0) will be set as this overflow is output.

Timer Mode Register A (TMA: $008): Timer mode register A is a 3-bit write-only register. The TMA controls the prescaler divide ratio of the timer A clock input as shown in table 13.

Timer mode register A is initialized to $0 by MCU reset.

Timer Mode Register B (TMB: $009): Timer mode register B (TMB) is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 14. Timer mode register B is initialized to $0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after timer mode register B is written to. The initialization of timer B by writing data into timer load register B should be performed after the contents of TMB are changed. The configuration and function of timer mode register B is shown in figure 14.

Timer B (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B): Timer B consists of an 8-bit write-only timer load register, and an 8-bit read-only timer counter. Each of them has a low-order digit (TCBL: $00A, TLRL: $00A) and a high-order digit (TCBU: $00B, TLRU: $00B). (Refer to figure 2.)

Timer counter B can be initialized by writing data into timer load register B. In this case, write the low-order digit first, and then the high-order digit. The timer counter is initialized when the high-order digit is written. The timer load register is initialized to $00 by MCU reset.

The counter value of timer B can be obtained by reading timer counter B. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched at the timer when the high-order digit is read.

Table 13 Timer Mode Register A

TMA2	TMA1	TMA0	Prescaler Divide Ratio
0	0	0	÷ 2048
0	0	1	÷ 1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Table 14 Timer Mode Register B

TMB3	Auto-Reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{INT_1}$ (external event input)

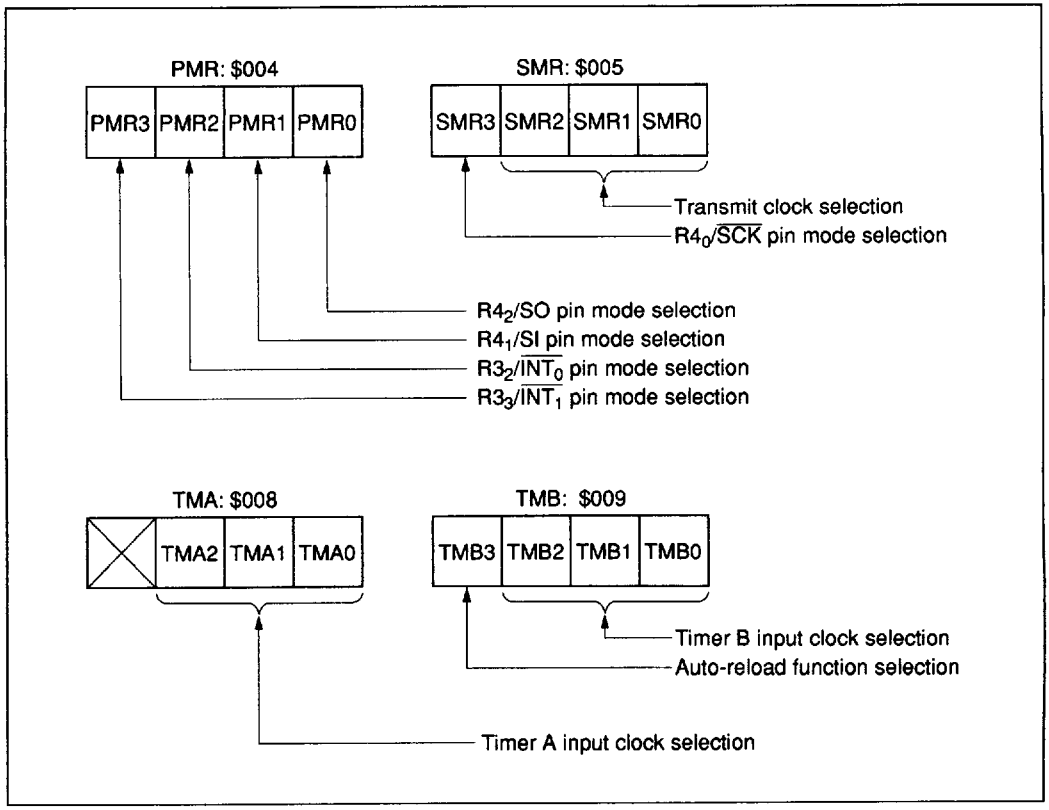


Figure 14 Mode Register Configuration and Function

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): The timer A interrupt request flag is set by the overflow output of timer A (table 15).

Timer A Interrupt Mask (IFTA: $001, Bit 3): The timer A interrupt mask prevents an interrupt request from being generated by the timer A interrupt request flag (table 16).

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 17).

Timer B Interrupt Mask (IMTB: $002, Bit 1): The timer B interrupt mask prevents an interrupt request from being generated by the timer B interrupt request flag (table 18).

Table 15 Timer A Interrupt Request Flag

IFTA	Interrupt Request
0	No
1	Yes

Table 16 Timer A Interrupt Mask

IMTA	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 17 Timer B Interrupt Request Flag

IFTB	Interrupt Request
0	No
1	Yes

Table 18 Timer B Interrupt Mask

IMTB	Interrupt Request
0	Enabled
1	Disabled (masked)

Input/Output

The MCU has 58 I/O pins, 32 standard and 26 high voltage. One of three circuit types can be selected by mask option for each standard pin: CMOS, with pull-up MOS, and without pull-up MOS (NMOS open drain); and one of two circuit types can be selected for each high-voltage pin: with pull-down MOS and without pull-down MOS (PMOS open drain). Since the pull-down MOS is connected to the internal V_{disp} line, the RA_1/V_{disp} pin must be selected as V_{disp} via the mask option when at least one high-voltage pin is selected as with pull-down MOS. See table 19 for I/O pin circuit types.

When every input/output pin is used as an input pin, the mask option and output data must be selected in the manner specified in table 20.

Output Circuit Operation of With Pull-Up MOS Standard Pins: In the standard pin option with pull-up MOS, the circuit shown in figure 15 is used to shorten the rise time of output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on and shorten the rise time. The write pulse keeps PMOS in the on state for one-eighth of the instruction cycle time. While the write pulse is 0, a high output level is maintained by the pull-up MOS (C).

When the $\overline{HLT}$ signal becomes 0 in the stop mode, MOS (A), (B), and (C) turn off.

D Port: The D Port is an I/O port which has 16 discrete I/O pins, each of which can be addressed independently. It can be set/reset through the SED/RED and SEDD/REDD instructions, and can be tested through the TD and TDD instructions. See table 19 as for the classification of standard pin, high-voltage pin, and the I/O pin circuit types.

R Ports: The eleven R ports in the HMCS408 are composed of 20 I/O pins, 16 output-only pins, and 6 input-only pins. Data is input through the LAR and LBR instructions and output through the LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, While invalid data will be read by reading from the output-only and/or non-existing ports.

The $R3_2$, $R3_3$, $R4_0$, $R4_1$, and $R4_2$ pins are multiplexed with the $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI, and SO pins, respectively. See table 19 as for the classification of standard pins, high-voltage pins, and selectable circuit types of these I/O pins.

Unused I/O Pins: If any unused I/O pins are left floating, the LSI may malfunction due to noise. The I/O pins should be fixed as follows to prevent malfunction.

High-voltage pins: Select as without pull-down MOS (PMOS open drain) via the mask option and connect to V_{CC} on the printed circuit board.

Standard pins: Select as without pull-up MOS (NMOS open drain) via the mask option and connect to GND on the printed circuit board.

$R4_0/\overline{SCK}$ and $R4_2$/SO should be used as $R4_0$ and $R4_2$ by the serial mode register and port mode register, respectively.

Reset

Bringing the RESET pin high resets the MCU. At power-on or when cancelling the stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instruction cycles are required for the MCU to be reset.

Table 21 shows the components initializes by MCU reset, and the status of each.

Table 19 I/O Pin Circuit Types

Standard Pins

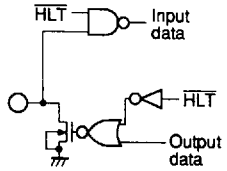
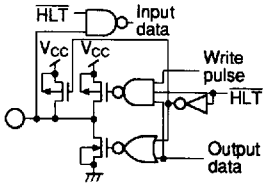
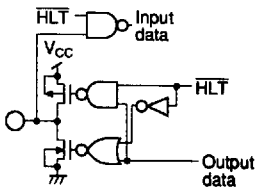
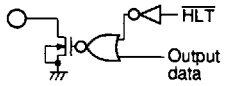
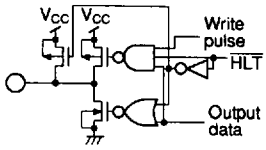
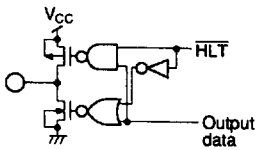
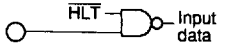
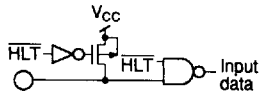
	Without Pull-Up MOS (NMOS Open Drain) (A)	With Pull-Up MOS (B)	CMOS (C)	Pins
I/O common pins				D_0 to D_3, $R3_0$ to $R3_3$, $R4_0$ to $R4_3$, $R5_0$ to $R5_3$
Output pins				$R6_0$ to $R6_3$, $R7_0$ to $R7_3$, $R8_0$ to $R8_3$
Input pins				$R9_0$ to $R9_3$

Table 19 I/O Pin Circuit Types (cont)

High Voltage Pins

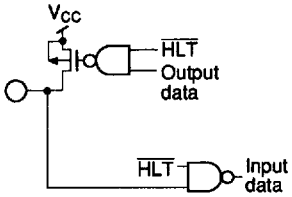
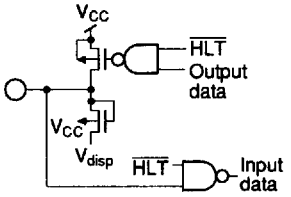
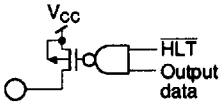
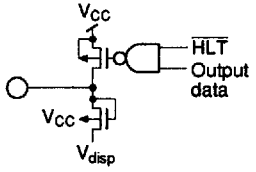
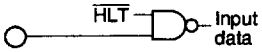
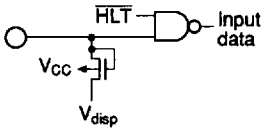
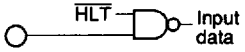
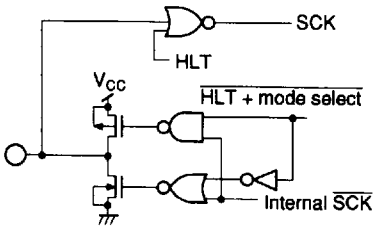
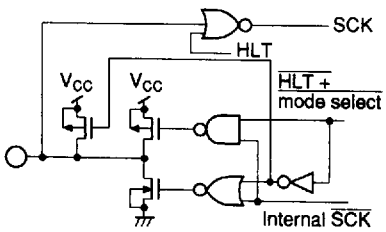
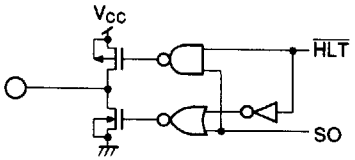
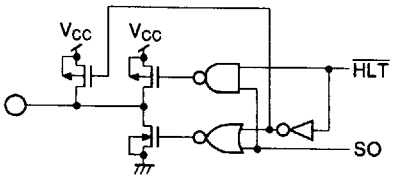
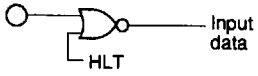
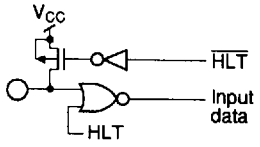
	Without Pull-Down MOS (PMOS Open Drain) (D)	With Pull-Down MOS (E)	Pins
I/O common pins			D_4 to D_{15}, $R1_0$ to $R1_3$, $R2_0$ to $R2_3$
Output pins			$R0_0$ to $R0_3$
Input pins			RA_0
Input pins			RA_1

Table 19 I/O Pin Circuit Types (cont)

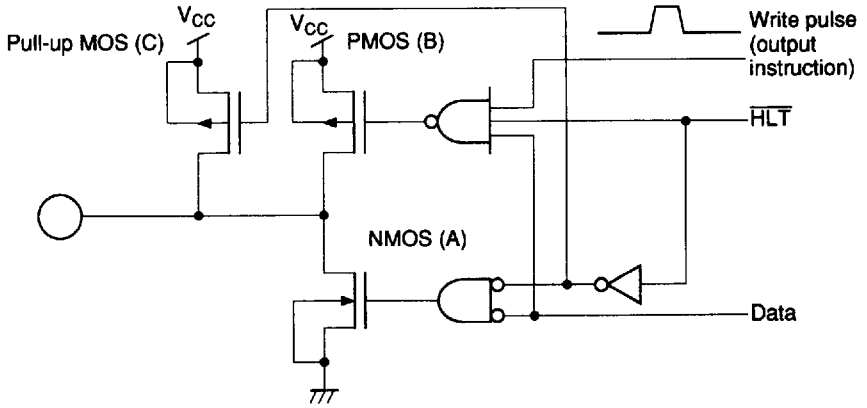
Standard Pins

	Without Pull-Up MOS (NMOS Open Drain) or CMOS (A or C)	With Pull-Up MOS (B)	Pins
I/O common pins			SCK* (output mode)
Output pins			SO
Input pins			INT_0, INT_1, SI, SCK (input mode)

Note: In the stop mode, HLT is 0, HLT is 1, and the I/O pins are in high impedance.
* If the MCU is interrupted by the serial interface in the external clock input mode, the SCK terminal becomes input only.

Table 20 Data Input from Common Input/Output Pins

I/O Pin Circuit Type		Input Possible	Input Pin State
Standard pins	CMOS	No	—
	Without pull-up MOS (NMOS open drain)	Yes	1
	With pull-up MOS	Yes	1
High voltage pins	Without pull-down MOS (PMOS open drain)	Yes	0
	With pull-down MOS	Yes	0



MOS Buffer	On-Resistance Value HMCS402C, HMCS402AC HMCS404C, HMCS404AC	 HMCS402CL, HMCS404CL
A	Approx. 250 Ω	Approx. 1 kΩ
B	Approx. 1 kΩ	Approx. 5 kΩ
C	Approx. 40 kΩ to 160 kΩ (V_{CC} = 5 V)	Approx. 75 kΩ to 1 MΩ (V_{CC} = 3 V) Approx. 40 kΩ to 160 kΩ (V_{CC} = 5 V)

MOS Buffer	On-Resistance Value HMCS408C, HMCS408AC	 HMCS408CL
A	Approx. 250 Ω	Approx. 1 kΩ
B	Approx. 1 kΩ	Approx. 1.7 kΩ
C	Approx. 30 kΩ to 160 kΩ (V_{CC} = 5 V)	Approx. 60 kΩ to 1 MΩ (V_{CC} = 3 V), approx. 30 kΩ to 160 kΩ (V_{CC} = 5 V)

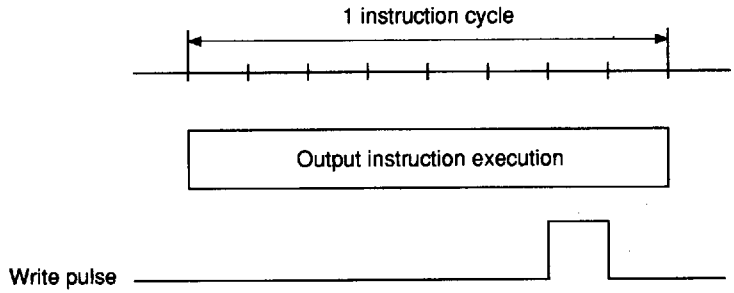


Figure 15 Output Circuit Operation of With Pull-Up MOS Standard Pins

Table 21 Initial Values After MCU Reset

Item			Initial Value	Contents
Program counter (PC)			$0000	Execute the program from the top of ROM address
Status flag (ST)			1	Enable to branch with conditional branch instructions
Stack pointer (SP)			$3FF	Stack level is 0
I/O pins, output register	Standard pins	(A) Without pull-up MOS	1	Enable to input
		(B) With pull-up MOS	1	Enable to input
		(C) CMOS	1	—
	High voltage pins	(D) Without pull-down MOS	0	Enable to input
		(E) With pull-down MOS	0	Enable to input
Interrupt flags/ mask	Interrupt enable flag (IE)		0	Inhibit all interrupts
	Interrupt request flag (IF)		0	No interrupt request
	Interrupt mask (IM)		1	Mask interrupt request
Mode registers	Port mode register (PMR)		0000	See Port Mode Register section
	Serial mode register (SMR)		0000	See Serial Mode Register section
	Timer mode register A (TMA)		000	See Timer Mode Register A section
	Timer mode register B (TMB)		0000	See Timer Mode Register B section
Timer/counters	Prescaler		$000	—
	Timer counter A (TCA)		$00	—
	Timer counter B (TCB)		$00	—
	Timer load register (TLR)		$00	—
	Octal counter		000	—

Note: MCU reset affects the other registers as shown on the next page.

Table 21 Initial Values After MCU Reset

Item		After MCU Reset to Recover from Stop Mode	After MCU Reset to Recover from Other Modes
Carry flag	(CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX registers	(X/SPX)		
Y/SPY registers	(Y/SPY)		
Serial data register	(SR)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	Same as above for RAM.

Internal Oscillator Circuit

Figure 16 outlines the internal oscillator circuit. Through the mask option, either a crystal oscillator or ceramic oscillator can be selected as the oscillator type. Refer to table 23 for the selection type. In addition, see figure 17 for the layout of the crystal or ceramic oscillator. In all cases, an external clock operation is available. Three divide ratios, 1/16, 1/8 and 1/4, are selectable via the mask option (table 22).

Table 22 Internal Oscillation Circuit Mask Option

	Oscillation			Divider		
Series Name	**Crystal**	**Ceramic**	**Resistor**	**1/16**	**1/8**	**1/4**
HMCS402C	Available	Available	Available	—	Available	—
HMCS402CL	Available	Available	—	—	Available	—
HMCS402AC	Available	Available	—	—	Available	—
HMCS404C	Available	Available	Available	—	Available	—
HMCS404CL	Available	Available	—	—	Available	—
HMCS404AC	Available	Available	—	—	Available	—
HMCS408C	Available	Available	—	—	Available	Available
HMCS408CL	Available	Available	—	Available	Available	—
HMCS408AC	Available	Available	—	—	Available	Available
HD4074008	Available	Available	—	—	Available	—
HD404019	Available	Available	—	—	—	Available
HD4074019	Available	Available	—	—	—	Available

Note: — implies not available

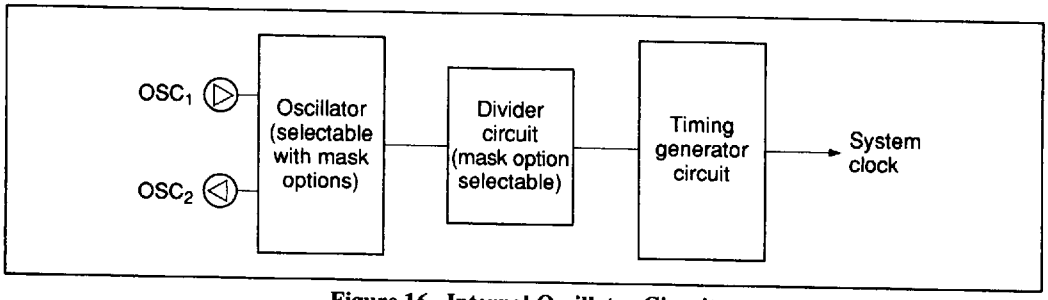


Figure 16 Internal Oscillator Circuit

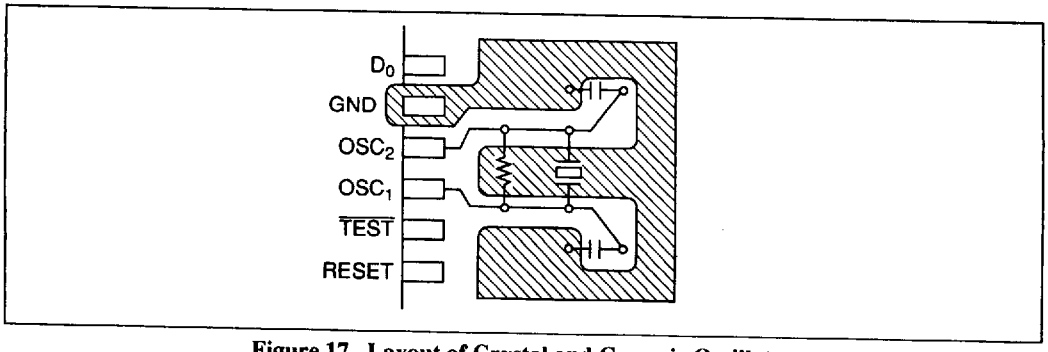
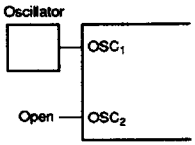
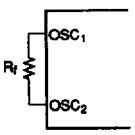
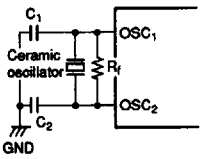
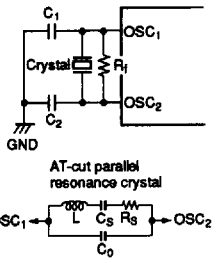
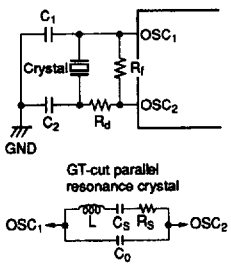


Figure 17 Layout of Crystal and Ceramic Oscillator

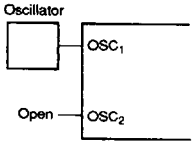
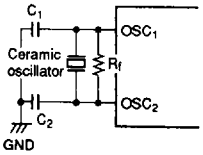
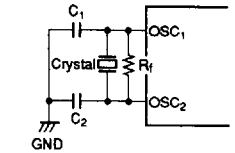
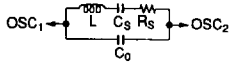
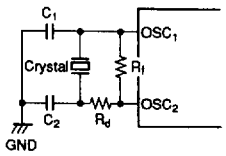
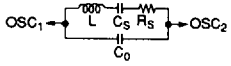
Table 23 Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants HMCS402C HMCS404C	HMCS402CL HMCS404CL	HMCS402AC HMCS404AC
External clock operation				
Resistor oscillator		R_f = 20 kΩ ±2%	—	—
Ceramic oscillator		Ceramic oscillator CSA 4.00MG (Murata) R_f: 1 MΩ ±2% C_1: 30 pF ±20% C_2: 30 pF ±20%	Ceramic oscillator CSA 2.000MK (Murata) R_f: 1 MΩ ±2% C_1: 30 pF ±20% C_2: 30 pF ±20%	Ceramic oscillator CSA 6.00MG (Murata) R_f: 1 MΩ ±2% C_1: 30 pF ±20% C_2: 30 pF ±20%
Crystal oscillator		R_f: 1 MΩ ±2% C_1: 10 pF to 22 pF ±20% C_2: 10 pF to 22 pF ±20% Crystal: Equivalent to bottom circuit C_0: 7 pF max. R_S: 60 Ω max. f: 2.0 MHz to 4.5 MHz	—	R_f: 1 MΩ ±2% C_1: 10 pF to 22 pF ±20% C_2: 10 pF to 22 pF ±20% Crystal: Equivalent to bottom circuit C_0: 7 pF max. R_S: 100 Ω max. f: 2.0 MHz to 6.2 MHz
		—	R_f: 2 MΩ ±2% C_1: 10 pF to 22 pF ±20% C_2: 10 pF to 22 pF ±20% Crystal: Equivalent to bottom circuit C_0: 7 pF max. R_S: 100 Ω max. f: 2.0 MHz to 2.25 MHz	—

Notes: 1. The circuit parameters written above are recommended by the crystal or ceramic oscillator manufacture. The circuit parameters are affected by the crystal, ceramic resonator, and the floating capacitance when designing the board. When using the resonator, consult with the crystal or ceramic oscillator manufacture to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, and other elements should be as short as possible, and avoid crossing other wires. Refer to the recommended layout of the crystal and ceramic oscillator (figure 17).

Table 23 Examples of Oscillator Circuits (cont)

	Circuit Configuration	Circuit Constants HMCS408C	HMCS408CL	HMCS408AC
External clock operation				
Ceramic oscillator		Ceramic oscillator CSA 4.00MG CSA 2.000MK (Murata) R_f: 1 MΩ ±20% C_1: 30 pF ±20% C_2: 30 pF ±20%	Ceramic oscillator CSA 2.000MK (Murata) R_f: 1 MΩ ±20% C_1: 30 pF ±20% C_2: 30 pF ±20%	Ceramic oscillator CSA 8.00MT CSA 4.00MG (Murata) R_f: 1 MΩ ±20% C_1: 30 pF ±20% C_2: 30 pF ±20%
Crystal oscillator	 AT-cut parallel resonance crystal 	R_f: 1 MΩ ±20% C_1: 10 pF to 22 pF ±20% C_2: 10 pF to 22 pF ±20% Crystal: Equivalent to bottom circuit C_0: 7 pF max. R_s: 100 Ω max. f: 1.0 MHz to 4.5 MHz	—	R_f: 1 MΩ ±20% C_1: 10 pF to 22 pF ±20% C_2: 10 pF to 22 pF ±20% Crystal: Equivalent to bottom circuit C_0: 7 pF max. R_s: 100 Ω max. f: 1.0 MHz to 9.0 MHz
	 GT-cut parallel resonance crystal 	—	R_f: 1 MΩ ±20% C_1: 10 pF to 22 pF ±20% C_2: 10 pF to 22 pF ±20% Crystal: Equivalent to bottom circuit C_0: 7 pF max. R_s: 100 Ω max. f: 1.0 MHz to 2.25 MHz	—

Notes: 1. The circuit parameters above are recommended by the crystal or ceramic oscillator manufacture. The circuit parameters are affected by the crystal, ceramic resonator, and the floating capacitance when designing the board. When using the resonator, consult with the crystal or ceramic oscillator manufacture to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, and other elements should be as short as possible, and avoid crossing other wires. Refer to the recommended layout of the crystal and ceramic oscillator (figure 17).

Operating Modes

The MCU has two low-power dissipation modes, standby mode and stop mode (table 24). Figure 18 is a mode transition diagram for these modes.

Standby Mode: Executing the SBY instruction puts the MCU into standby mode. In standby mode, the oscillator circuit is active, and interrupts and the timer/counters remain working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 24 Low-Power Dissipation Modes Function

		Condition							
Low-Power Dissipation Mode	**Instruction**	**Oscillator Circuit**	**Instruction Execution**	**Registers, Flags**	**Interrupts Function**	**RAM**	**Input/ Output Pins**	**Timer/ Counters, Serial Interface**	**Cancellation Method**
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained*3	Active	RESET input, interrupt request
Stop mode	STOP instruction	Stop	Stop	Reset*1	Stop	Retained	High impedance*2	Stop	RESET input

Notes: 1. The MCU cancels the stop mode by RESET input. Refer to table 21 for the contents of the flags and registers.
2. A high-voltage pin with pull-down MOS is tied to the V_{disp} power supply through the pull-down MOS. As the pull-down MOS stays on, a pull-down current flows when a difference between the pin voltage and the V_{disp} voltage exists. This is the additional current to the current dissipation in the stop mode (I_{STOP}).
3. When an I/O circuit is active, an I/O current may flow, depending on the state of the I/O pin in standby mode. This is the additional current for current dissipation in standby mode.

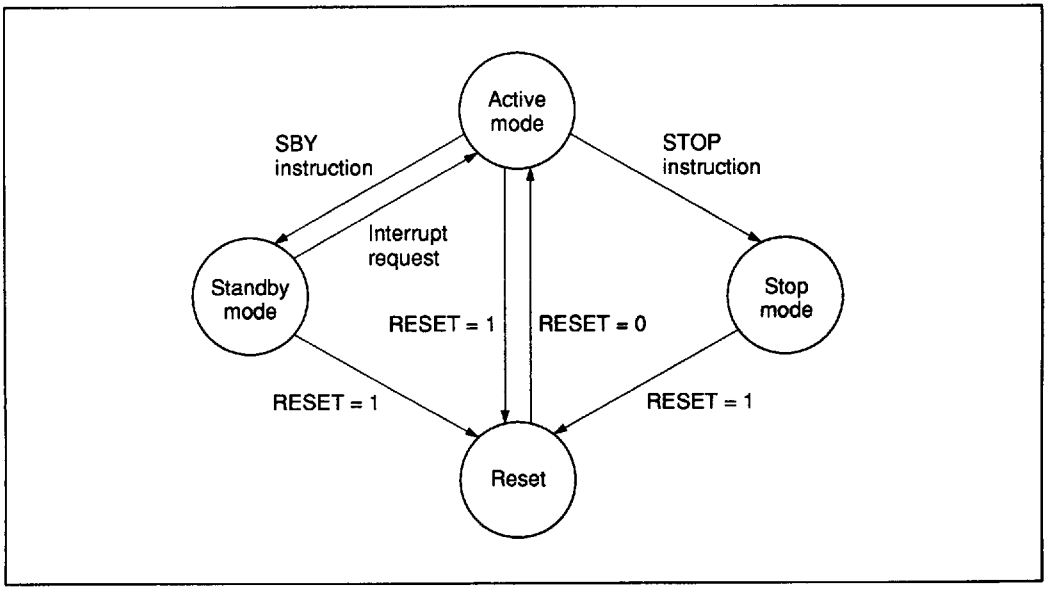


Figure 18 MCU Operation Mode Transition

The standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 at this time, the interrupt is executed; if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the latter case, the MCU becomes active and executes the next instruction following the SBY instruction.

Figure 19 shows the flowchart of the standby mode.

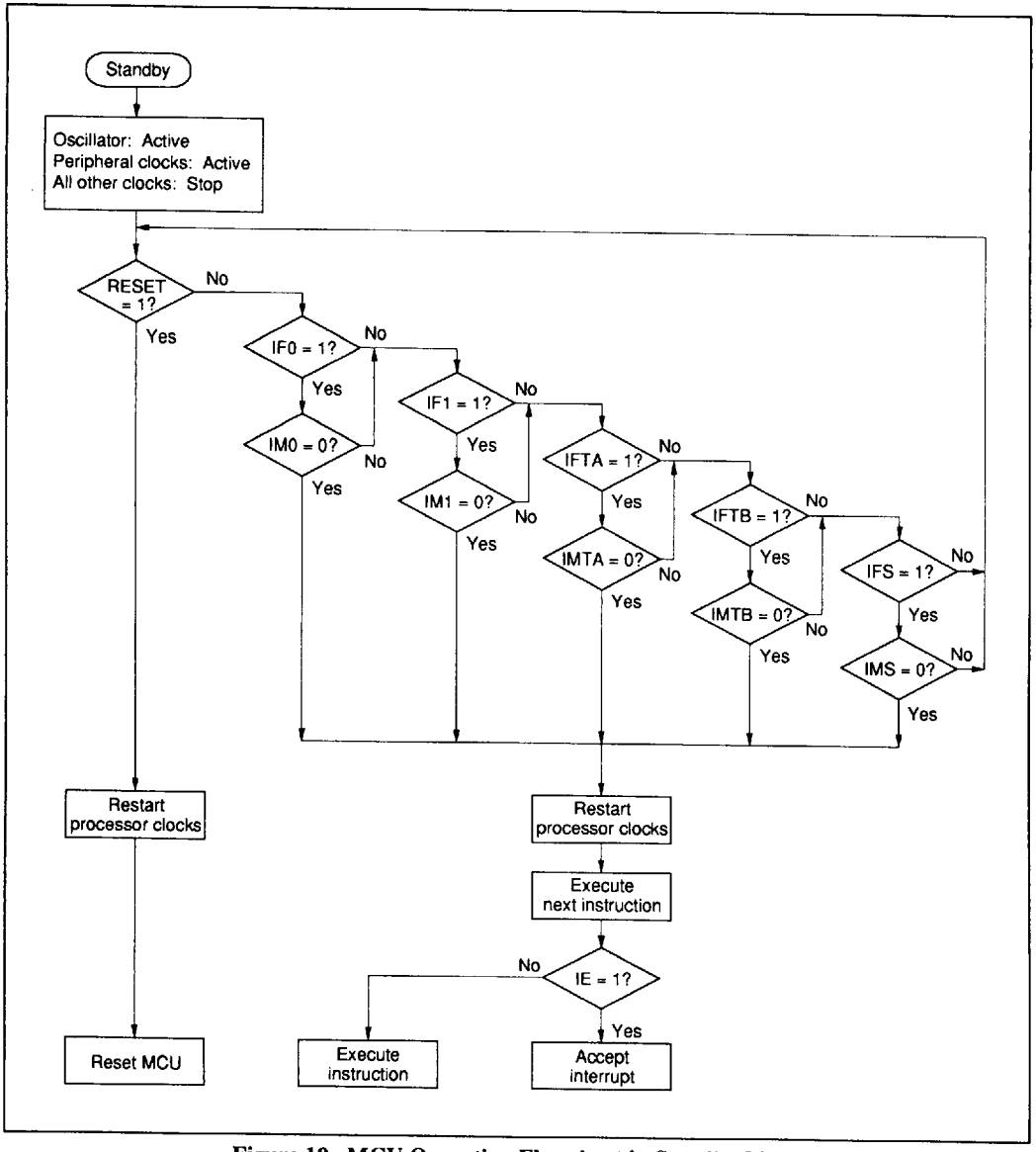


Figure 19 MCU Operating Flowchart in Standby Mode

Stop Mode: Executing the STOP instruction brings the MCU into the stop mode, in which the oscillator circuit and every function of the MCU stop.

The stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 20, the RESET input must be applied for at least t_{RC} for the oscillation to stabilize. (Refer to the AC Characteristics table.) After stop mode is cancelled, RAM retains the state it was in just before the MCU went into the stop mode, but the accumulator, B register, W register, Y/SPY registers, and carry flag will not retain their contents.

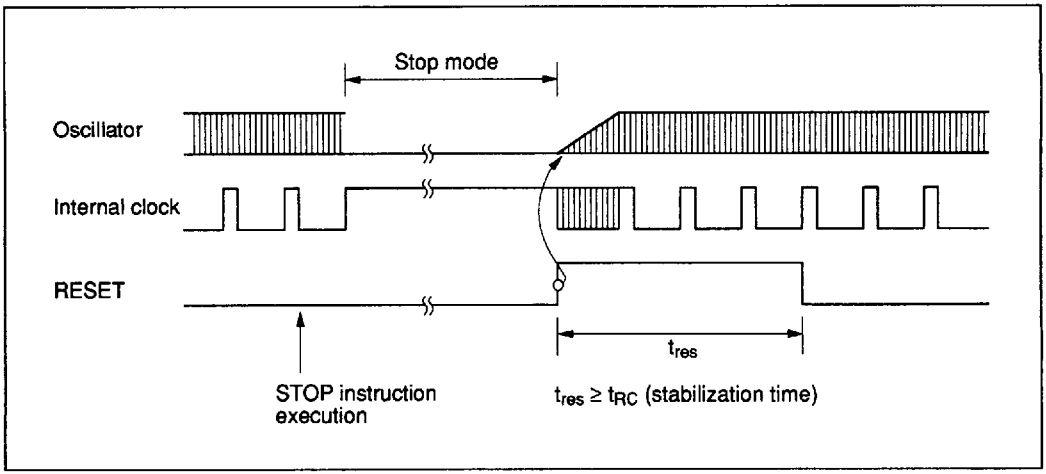


Figure 20 Timing of Stop Mode Cancellation

Addressing Modes

RAM Addressing Modes

As shown in Figure 21, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing Mode: The W register, X register, and Y register contents (10 bits total) are used as the RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing Mode: The memory registers (16 digits from $020 to $02F) are accessed by executing the LAMR and XMRA instructions.

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes as shown in figure 22.

Direct Addressing Mode: The program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has eight pages of ROM with 256 words per page. By executing the BR instruction, the program can branch to an address on the current page. This instruction replaces the low-order eight bits of the program counter (PC_7 to PC_0) with 8-bit immediate data.

When the BR instruction is on a page boundary (256n + 255) (figure 23), executing it transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR instruction is used on a page boundary. The HMCS400 series cross macroassembler has an automatic paging facility for ROM pages.

Zero-Page Addressing Mode: By executing the CAL instruction, the program can branch to the zero-page subroutine area, which is located at $0000 to $003F. When the CAL instruction is executed, 6 bits of immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing Mode: By executing the TBL instruction, the program can branch to an address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by the P instruction (figure 24). When bit 8 in the referenced ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output registers. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

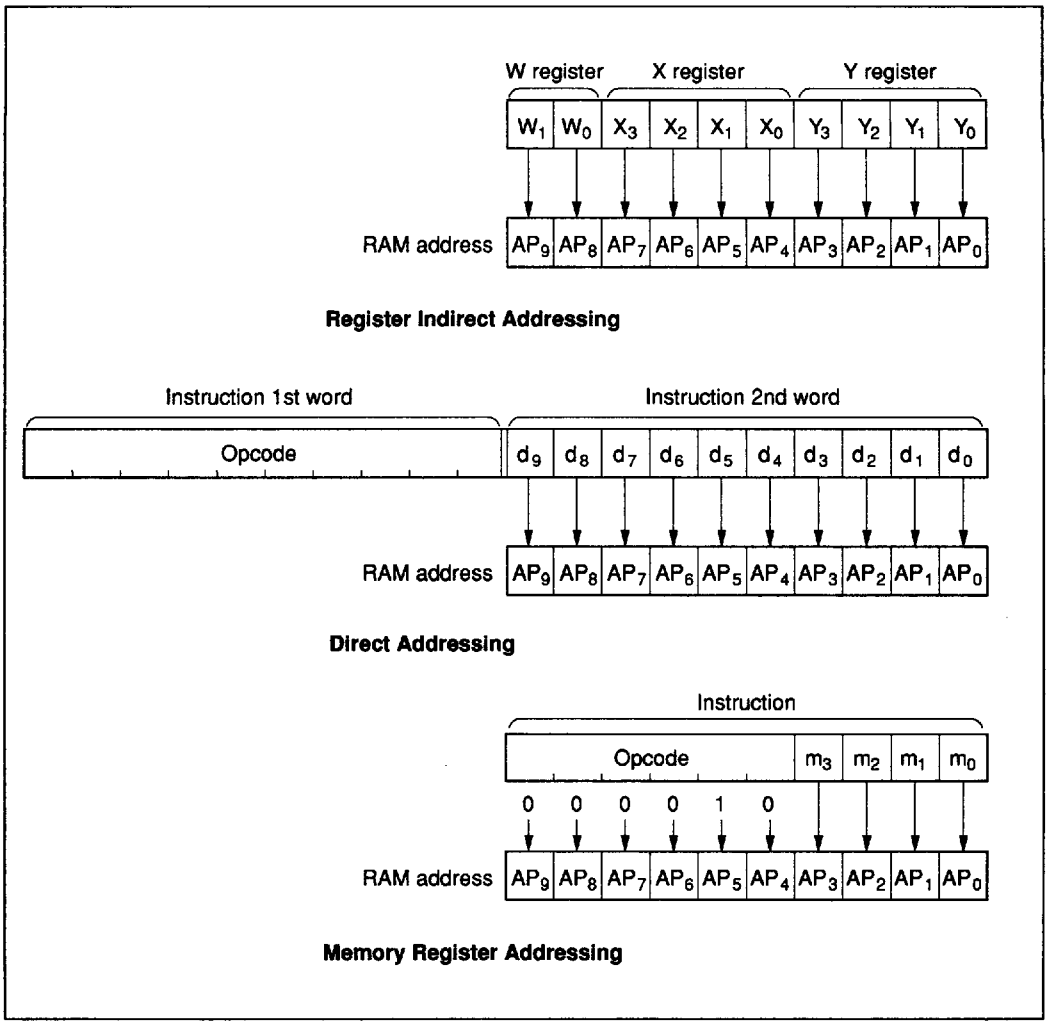


Figure 21 RAM Addressing Modes

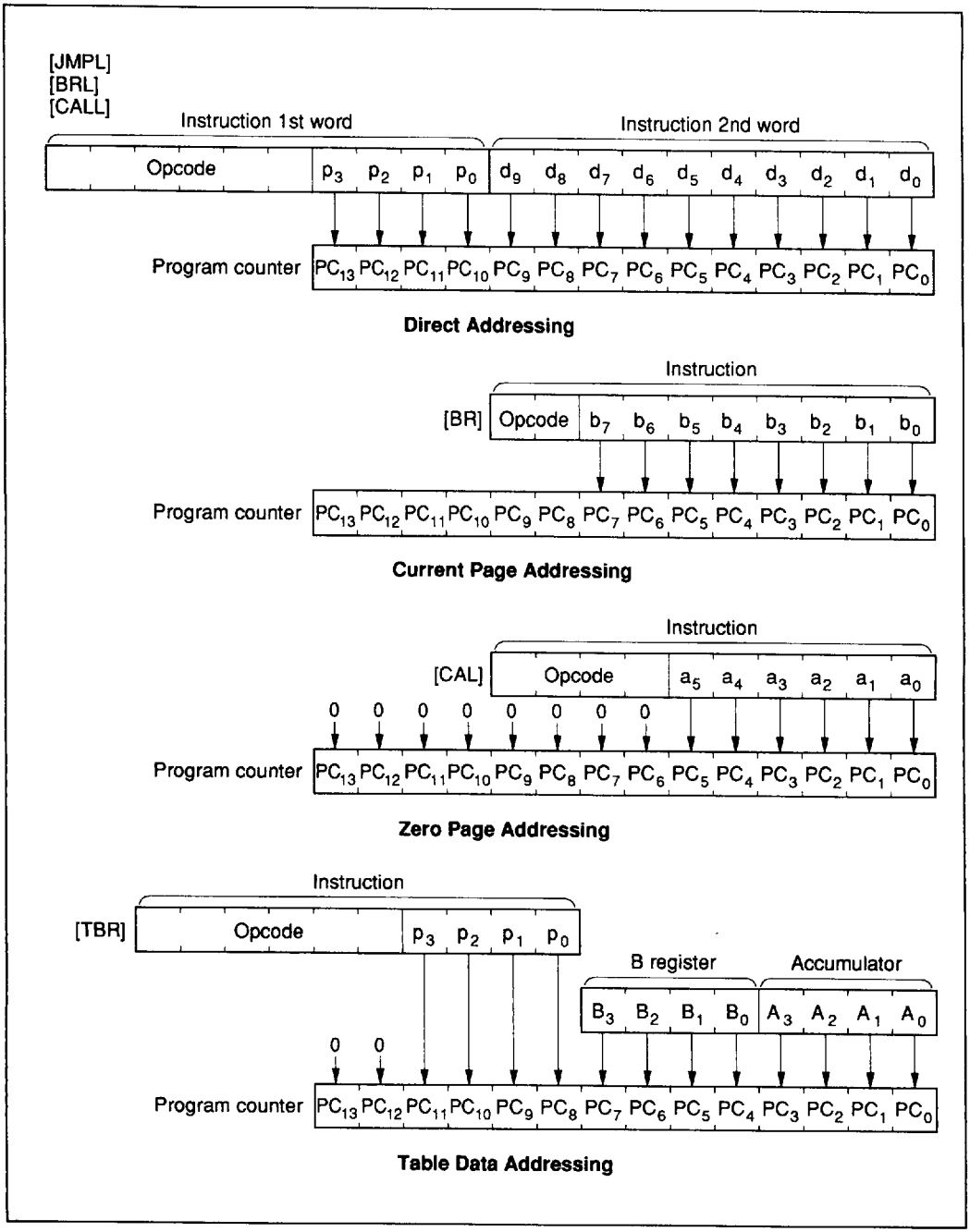


Figure 22 ROM Addressing Modes

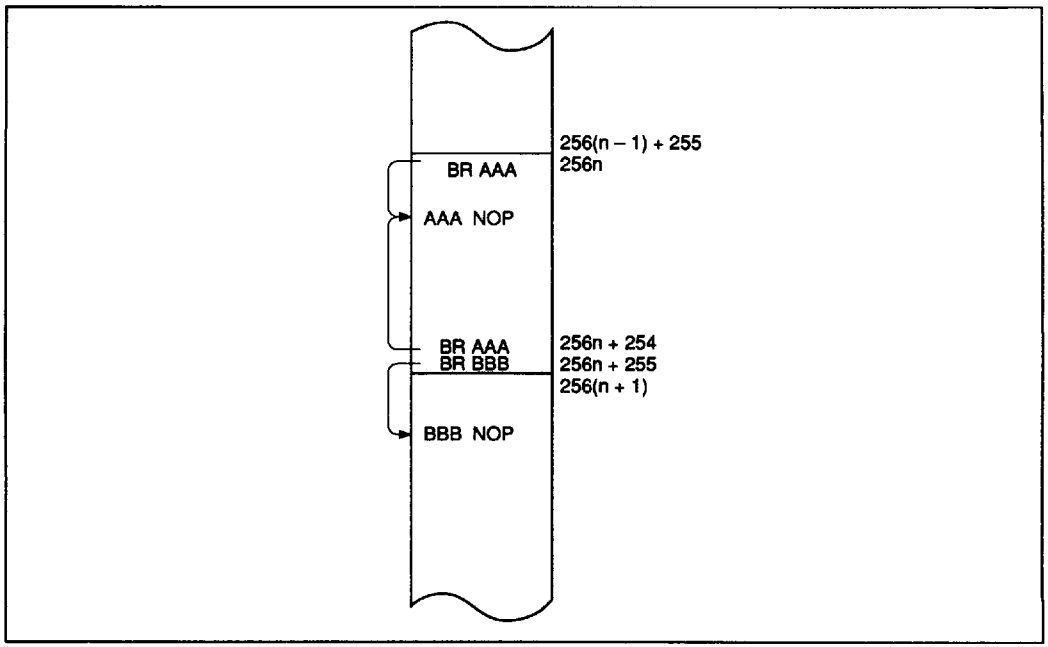


Figure 23 BR Instruction Branch Destination on a Page Boundary

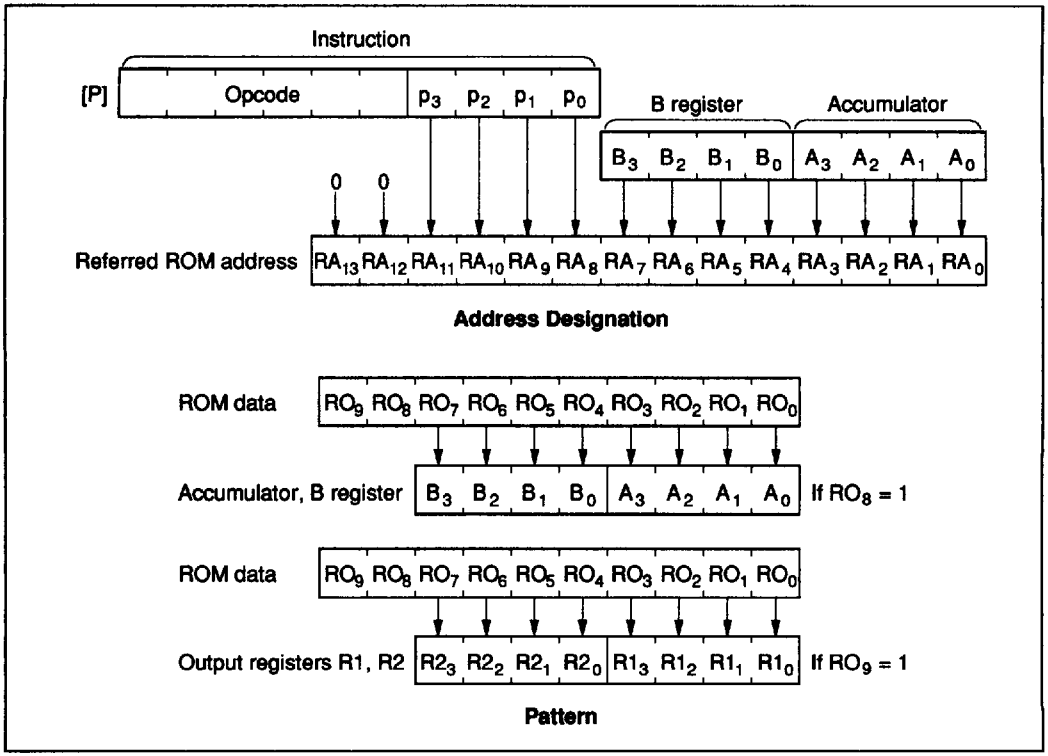


Figure 24 P Instruction

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	1
		V_{CC} – 45 to V_{CC} + 0.3	V	2
Total permissible input current	ΣI_o	50	mA	3
Total permissible output current	$-\Sigma I_o$	150	mA	4
Maximum input current	I_o	15	mA	5, 6
Maximum output current	$-I_o$	4	mA	6, 7
		6	mA	7, 8
		30	mA	7, 9
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation should be under the conditions of the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.
All voltages are with respect to GND.

1. Applied to standard pins.
2. Applied to high voltage pins.
3. Total permissible input current is the total sum of input currents which flow in from all I/O pins to GND simultaneously.
4. Total permissible output current is the total sum of the output currents which flow out from V_{CC} to all I/O pins simultaneously.
5. Maximum input current is the maximum amount of input current from each I/O pin to GND.
6. Applied to D_0 to D_3 and R3 to R8.
7. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
8. Applied to R0 to R2.
9. Applied to D_4 to D_{15}.

HMCS402C Electrical Characteristics

DC Characteristics (V_{CC} = 4 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition		Notes
Input high voltage	V_{IH}	RESET, SCK, INT_0, INT_1	0.7V_{CC}	—	V_{CC} + 0.3	V			
		SI	0.7V_{CC}	—	V_{CC} + 0.3	V			
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V			
Input low voltage	V_{IL}	RESET, SCK, INT_0, INT_1	–0.3	—	0.22V_{CC}	V			
		SI	–0.3	—	0.22V_{CC}	V			
		OSC_1	–0.3	—	0.5	V			
Output high voltage	V_{OH}	SCK, SO	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA		
			V_{CC} – 0.3	—	—	V	$-I_{OH}$ = 0.01 mA		
Output low voltage	V_{OL}	SCK, SO	—	—	0.4	V	I_{OL} = 1.6 mA		
Input/output leakage current	$\|I_{IL}\|$	RESET, SCK, INT_0, INT_1, SI, SO, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}		1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V	Crystal or ceramic oscillator f_{OSC} = 4 MHz	2, 6
			—	—	2.4	mA		Resistor oscillator f_{OSC} = 4 MHz	2, 6
Current dissipation in standby mode	I_{SBY1}	V_{CC}	—	—	1.2	mA	Maximum logic operation V_{CC} = 5 V	Crystal or ceramic oscillator f_{OSC} = 4 MHz	3, 6
			—	—	1.6	mA		Resistor oscillator f_{OSC} = 4 MHz	3, 6
	I_{SBY2}	V_{CC}	—	—	0.9	mA	Minimum logic operation V_{CC} = 5 V	Crystal or ceramic oscillator f_{OSC} = 4 MHz	4, 6
			—	—	1.3	mA		Resistor oscillator f_{OSC} = 4 MHz	4, 6
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	$V_{in(\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}, $V_{in(RESET)}$ = 0 V to 0.3 V		5
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V			

Refer to notes on the following page.

Notes: 1. Pull up MOS current and output buffer current are excluded.

2. The MCU is in the reset state. The input/output current does not flow.

   Test conditions: MCU state
   - Reset state in operation mode

   Pin state
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

3. The timer/counter operates with the fastest clock and input/output current does not flow.

   Test conditions: MCU state
   - Standby mode
   - Input/output: Reset state
   - Timer A: Divide-by-2 prescaler divide ratio
   - Timer B: Divide-by-2 prescaler divide ratio
   - Serial interface: Stop

   Pin state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

4. The timer/counter operates with the slowest clock and input/output current does not flow.

   Test conditions: MCU state
   - Standby mode
   - Input/output: Reset state
   - Timer A: Divide-by-2048 prescaler divide ratio
   - Timer B: Divide-by-2048 prescaler divide ratio
   - Serial interface: Stop

   Pin state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

5. Pull-down MOS current is excluded.

6. When $f_{OSC} = \chi$ MHz, the current dissipation in operation mode and standby mode are estimated as follows:

   Maximum value ($f_{OSC} = \chi$ MHz) = $\frac{\chi}{4}$ × max. value (f_{OSC} = 4 MHz)

Input/Output Characteristics for Standard Pins (V_{CC} = 4 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0 to D_3, R3 to R5, R9	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0 to D_3, R3 to R5, R9	–0.3	—	$0.22V_{CC}$	V		
Output high voltage	V_{OH}	D_0 to D_3, R3 to R8	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA	1
		D_0 to D_3, R3 to R8	V_{CC} – 0.3	—	—	V	$-I_{OH}$ = 0.01 mA	1
Output low voltage	V_{OL}	D_0 to D_3, R3 to R8	—	—	0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	D_0 to D_3, R3 to R9	—	—	1	µA	V_{in} = 0 V to V_{CC}	2
Pull-up MOS current	$-I_{PU}$	D_0 to D_3, R3 to R9	30	60	120	µA	V_{CC} = 5 V, V_{in} = 0 V	3

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Pull-up MOS current and output buffer current are excluded.
3. Applied to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High Voltage Pins (V_{CC} = 4 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_4 to D_{15}, R1, R2, RA_0, RA_1	0.7 V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_4 to D_{15}, R1, R2, RA_0, RA_1	V_{CC} – 40	—	0.22V_{CC}	V		
Output high voltage	V_{OH}	D_4 to D_{15}	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA, V_{CC} = 5 V ±10%	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 9 mA	
		R0 to R2	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 3 mA, V_{CC} = 5 V ±10%	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 1.8 mA	
Output low voltage	V_{OL}	D_4 to D_{15}, R0 to R2	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
		D_4 to D_{15}, R0 to R2	—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	2
Input/output leakage current	$\|I_{IL}\|$	D_4 to D_{15}, R0 to R2, RA_0, RA_1	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_4 to D_{15}, R0 to R2, RA_0, RA_1	125	250	500	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applied to I/O pins selected as with pull-down MOS by mask option.
2. Applied to I/O pins selected as without pull-down MOS (PMOS open drain) by mask option.
3. Pull-down MOS current and output buffer current are excluded.

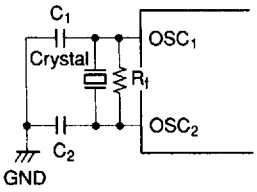
AC Characteristics (V_{CC} = 4 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item		Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Crystal or ceramic oscillator	Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz		
	Instruction cycle time	t_{cyc}		1.78	2	20	µs		
	Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms		1
Resistor oscillator	Oscillation frequency	f_{OSC}	OSC_1, OSC_2	1.8	3.0	4.2	MHz	R_f = 20 kΩ ±2%	
	Instruction cycle time	t_{cyc}		1.9	2.66	4.44	µs	R_f = 20 kΩ ±2%	
	Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	0.5	ms	R_f = 20 kΩ ±2%	1
External clock	External clock frequency	f_{CP}	OSC_1	0.4	—	4.5	MHz		2
	External clock high width	t_{CPH}	OSC_1	100	—	—	ns		2
	External clock low width	t_{CPL}	OSC_1	100	—	—	ns		2
	External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
	External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
	Instruction cycle time	t_{cyc}		1.78	—	20	µs		2
$\overline{INT_0}$ high width		t_{IH}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_0}$ low width		t_{IL}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ high width		t_{IH}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ low width		t_{IL}	$\overline{INT_1}$	2	—	—	t_{cyc}		4
RESET high width		t_{RSTH}	RESET	2	—	—	t_{cyc}		4
Input capacitance		C_{in}	All pins	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
RESET fall time		t_{RSTf}		—	—	20	ms		4

Refer to notes on the following page.

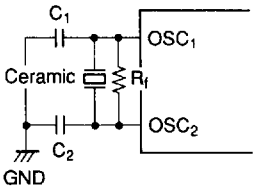
Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches 4.0 V at power-on until when the oscillator stabilizes, or after RESET goes high by MCU reset to quit the stop mode. At power-on or recovering from stop mode, apply the RESET input for more than t_{RC} to meet the necessary time for oscillator stabilization. When using a crystal or ceramic oscillator, consult with the crystal and ceramic oscillator manufacture since the oscillator stabilization time depends on the circuit constant and stray capacity.

Crystal oscillator



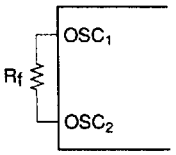
Crystal: 4.194304MHz NC-18C
(Nihon Denpa Kogyo)
R_f: 1 MΩ ±2%
C_1: 22 pF ±20%
C_2: 22 pF ±20%

Ceramic oscillator



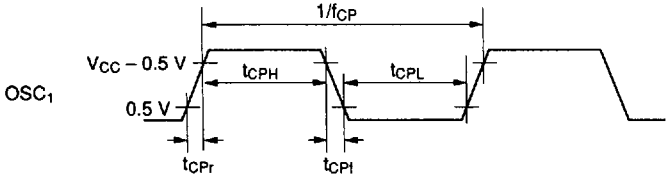
Ceramic: CSA4.00MG
(Murata)
R_f: 1 MΩ ±2%
C_1: 30 pF ±20%
C_2: 30 pF ±20%

Resistor oscillator

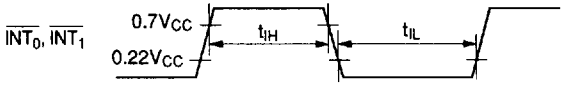


R_f: 20 MΩ ±2%

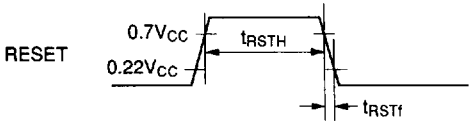
2.



3.



4.



Serial Interface Timing Characteristics (V_{CC} = 4 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	See note 2	1, 2
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—	t_{Scyc}	See note 2	1, 2
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}	See note 2	1, 2
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	100	ns	See note 2	1, 2
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	100	ns	See note 2	1, 2
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	See note 2	1, 2
Serial input data setup time	t_{SSI}	SI	500	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns		1

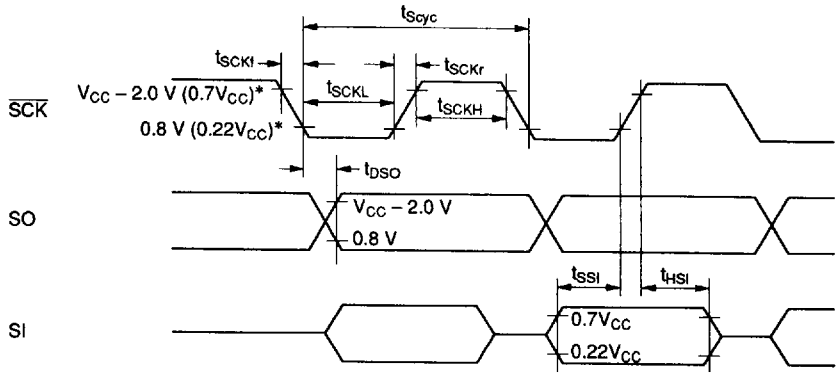
Refer to notes on the following page.

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	100	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	100	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	See note 2	1, 2
Serial input data setup time	t_{SSI}	SI	500	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns		1

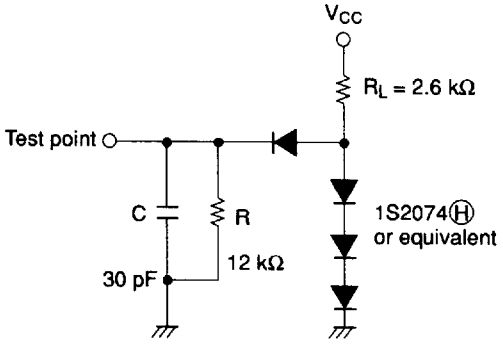
Refer to notes on the following page.

Notes: 1. Timing of serial interface

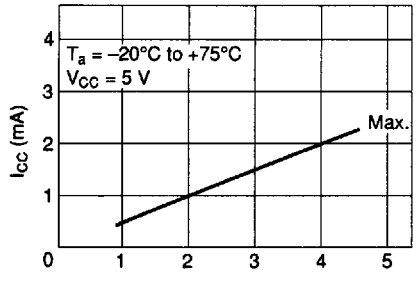


Note: * V_{CC} – 2.0 V and 0.8 V are the threshold voltages for transmit clock output.
$0.7V_{CC}$ and $0.22V_{CC}$ are the threshold voltages for transmit clock input.

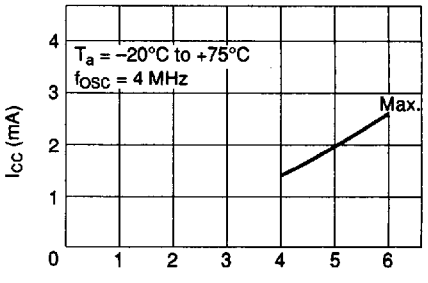
2. Timing load circuit



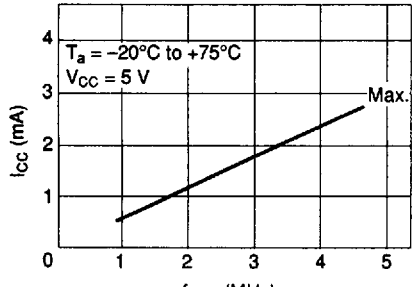
Characteristics Curves (Reference Data)



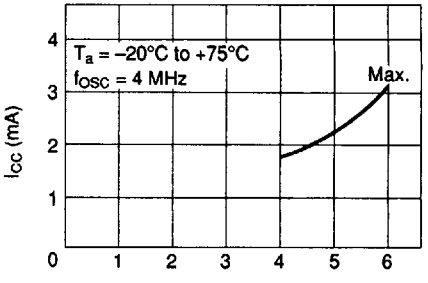
I_{CC} vs. f_{OSC} characteristics
(crystal and ceramic oscillator option)



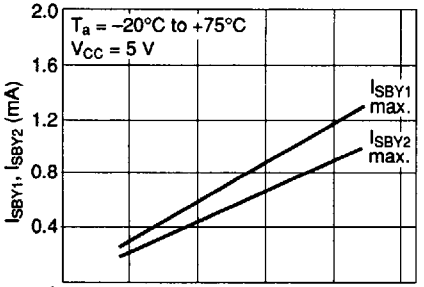
I_{CC} vs. V_{CC} characteristics
(crystal and ceramic oscillator option)



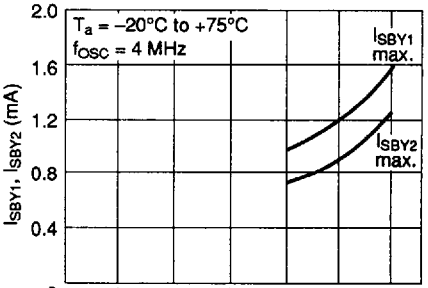
I_{CC} vs. f_{OSC} characteristics
(resistor oscillator option)



I_{CC} vs. V_{CC} characteristics
(resistor oscillator option)

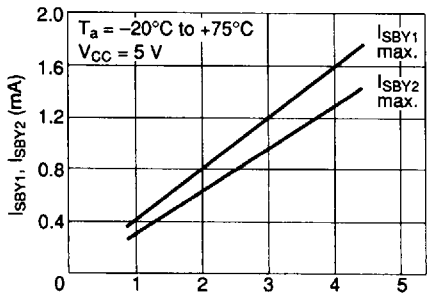


I_{SBY} vs. f_{OSC} characteristics
(crystal and ceramic oscillator option)

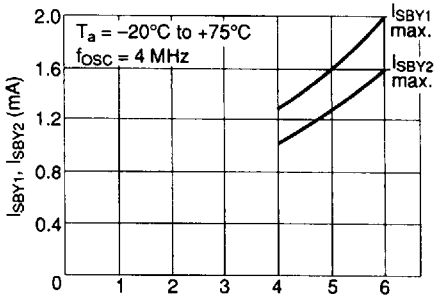


I_{SBY} vs. V_{CC} characteristics
(crystal and ceramic oscillator option)

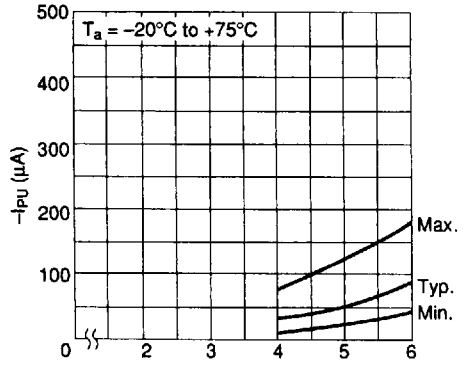
Characteristics Curves (Reference Data) (cont)



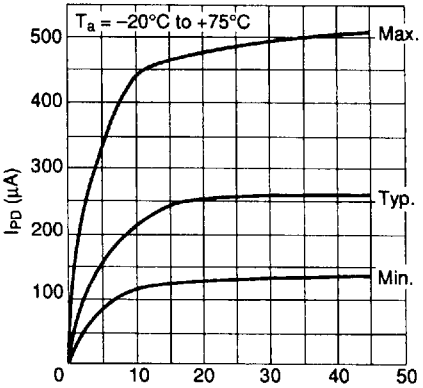
I_{SBY} vs. f_{OSC} characteristics
(resistor oscillator option)



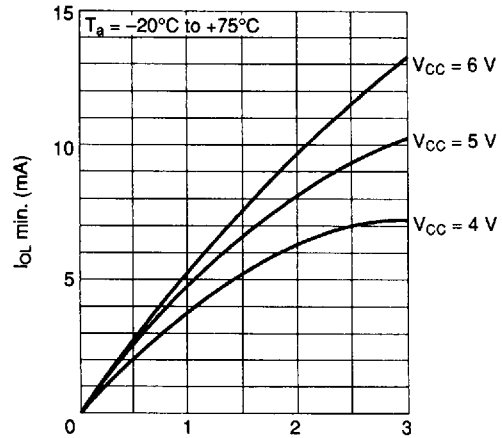
I_{SBY} vs. V_{CC} characteristics
(resistor oscillator option)



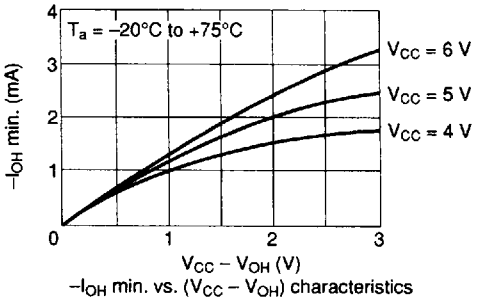
$-I_{PU}$ (pull-up MOS current) vs.
V_{CC} characteristics



I_{PD} (pull-down MOS current) vs.
($V_{CC} - V_{disp}$) characteristics

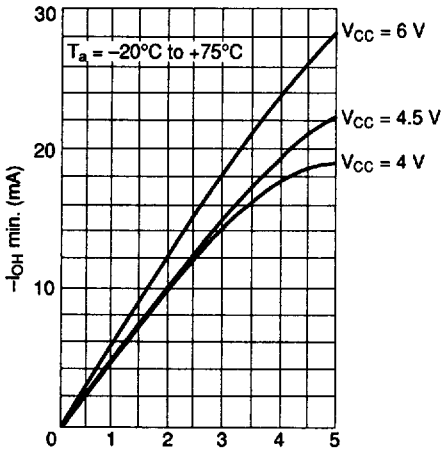


I_{OL} min. vs. V_{OL} characteristics
(standard pin)

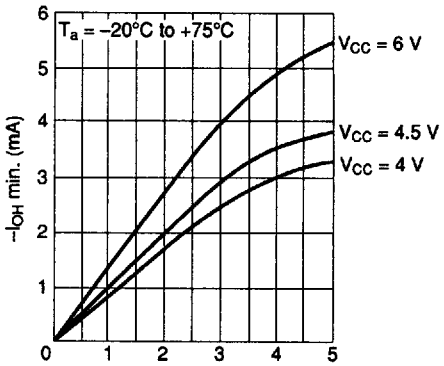


$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(standard pin CMOS)

Characteristics Curves (Reference Data) (cont)



$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(D_4 to D_{15} pins)



$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(R0 to R2 ports)

HMCS402CL Electrical Characteristics

DC Characteristics (V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$	$0.85V_{CC}$	—	V_{CC} + 0.3	V		
		SI	$0.85V_{CC}$	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.3	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$	–0.3	—	$0.15V_{CC}$	V		
		SI	–0.3	—	$0.15V_{CC}$	V		
		OSC_1	–0.3	—	0.3	V		
Output high voltage	V_{OH}	$\overline{SCK}$, SO	V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.1 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO	—	—	0.4	V	I_{OL} = 0.4 mA	
Input/output leakage current	$\|I_{IL}\|$	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	0.6	mA	V_{CC} = 3 V, f_{OSC} = 2 MHz	2, 6
Current dissipation in standby mode	I_{SBY1}	V_{CC}	—	—	0.5	mA	Maximum logic operation V_{CC} = 3 V, f_{OSC} = 2 MHz	3, 6
	I_{SBY2}	V_{CC}	—	—	0.4	mA	Minimum logic operation V_{CC} = 3 V, f_{OSC} = 2 MHz	4, 6
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	$V_{in(\overline{TEST})}$ = V_{CC} – 0.2 V to V_{CC}, $V_{in(RESET)}$ = 0 V to 0.2 V	5
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Refer to notes on the following page.

Notes: 1. Pull up MOS current and output buffer are excluded.

2. The MCU is in the reset state. The input/output current does not flow.

   Test conditions: MCU state
   - Reset state in operation mode

   Pin state
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

3. The timer/counter operates with the fastest clock and input/output current does not flow.

   Test conditions: MCU state
   - Standby mode
   - Input/output: Reset state
   - Timer A: Divide-by-2 prescaler divide ratio
   - Timer B: Divide-by-2 prescaler divide ratio
   - Serial interface: Stop

   Pin state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

4. The timer/counter operates with the slowest clock and input/output current does not flow.

   Test conditions: MCU state
   - Standby mode
   - Input/output: Reset state
   - Timer A: Divide-by-2048 prescaler divide ratio
   - Timer B: Divide-by-2048 prescaler divide ratio
   - Serial interface: Stop

   Pin state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

5. Pull-down MOS current is excluded.

6. When $f_{OSC} = \chi$ MHz, the current dissipation in operation mode and standby mode are estimated as follows:

   (For divide-by-8 (D-8) option)

   Maximum value ($f_{OSC} = \chi$ MHz) = $\frac{\chi}{2}$ × max. value (f_{OSC} = 2 MHz)

Input/Output Characteristics for Standard Pins (V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0 to D_3, R3 to R5, R9	0.85V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0 to D_3, R3 to R5, R9	–0.3	—	0.15V_{CC}	V		
Output high voltage	V_{OH}	D_0 to D_3, R3 to R8	V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.1 mA	1
Output low voltage	V_{OL}	D_0 to D_3, R3 to R8	—	—	0.4	V	I_{OH} = 0.4 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	D_0 to D_3, R3 to R9	—	—	1	µA	V_{in} = 0 V to V_{CC}	2
Pull-up MOS current	$-I_{PU}$	D_0 to D_3, R3 to R9	3	15	40	µA	V_{CC} = 3 V, V_{in} = 0 V	3
		D_0 to D_3, R3 to R9	30	60	120	µA	V_{CC} = 5 V, V_{in} = 0 V	3

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Pull-up MOS current and output buffer current are excluded.
3. Applied to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High Voltage Pins (V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_4 to D_{15}, R1, R2, RA_0, RA_1	0.85 V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_4 to D_{15}, R1, R2, RA_0, RA_1	V_{CC} – 40	—	0.15V_{CC}	V		
Output high voltage	V_{OH}	D_4 to D_{15}	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA, V_{CC} = 5 V ±10%	
			V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 2.5 mA	
		R0 to R2	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 3 mA, V_{CC} = 5 V ±10%	
			V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	D_4 to D_{15}, R0 to R2	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
		D_4 to D_{15}, R0 to R2	—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	2
Input/output leakage current	$\|I_{IL}\|$	D_4 to D_{15}, R0 to R2 RA_0, RA_1	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_4 to D_{15}, R0 to R2, RA_0, RA_1	125	250	500	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

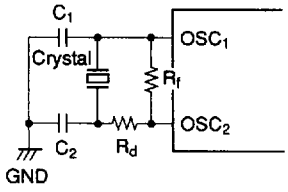
Notes: 1. Applied to I/O pins selected as with pull-down MOS by mask option.
2. Applied to I/O pins selected as without pull-down MOS (PMOS open drain) by mask option.
3. Pull-down MOS current and output buffer current are excluded.

AC Characteristics (V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	2	2.25	MHz		
Instruction cycle time	t_{cyc}		3.55	4	20	µs		
Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	60	ms		1
External clock high width	t_{CPH}	OSC_1	205	—	—	ns		2
External clock low width	t_{CPL}	OSC_1	205	—	—	ns		2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT_0}$ high width	t_{IH}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_0}$ low width	t_{IL}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ high width	t_{IH}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ low width	t_{IL}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		4
Input capacitance	C_{in}	All pins	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
RESET fall time	t_{RSTf}		—	—	15	ms		4

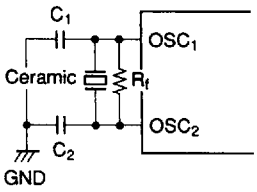
Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches 2.7 V at power-on until the oscillator stabilizes, or after RESET goes high by MCU reset to quit the stop mode. At power-on or recovering from stop mode, apply the RESET input for more than t_{RC} to meet the necessary time for oscillator stabilization. The circuits used to measure the value are shown below. When using a crystal or ceramic oscillator, consult with the crystal and ceramic oscillator manufacture since the oscillator stabilization time depends on the circuit constant and stray capacity.

Crystal oscillator



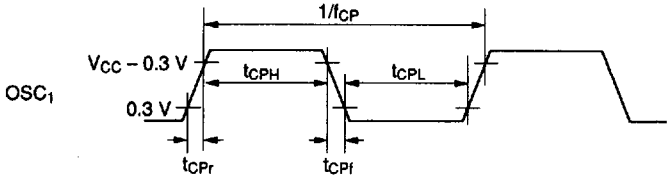
Crystal: 2.097152MHz DS-MGQ308
(Seiko Denshi)
R_f: 2 MΩ ±2%, R_d: 2.2 MΩ ±2%
C_1: 10 pF ±20%
C_2: 10 pF ±20%

Ceramic oscillator

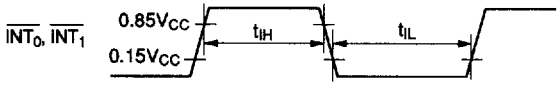


Ceramic: CSA2.000MK
(Murata)
R_f: 1 MΩ ±2%
C_1: 30 pF ±20%
C_2: 30 pF ±20%

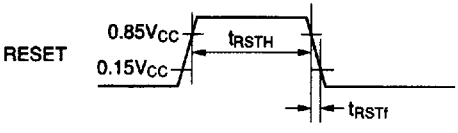
2.


1/fCP
VCC – 0.3 V
tCPH
tCPL
OSC1
0.3 V
tCPr
tCPf

3.


INT0, INT1
0.85VCC
0.15VCC
tIH
tIL

4.


RESET
0.85VCC
0.15VCC
tRSTH
tRSTf

Serial Interface Timing Characteristics (V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	See note 2	1, 2
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—	t_{Scyc}	See note 2	1, 2
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}	See note 2	1, 2
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	300	ns	See note 2	1, 2
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	300	ns	See note 2	1, 2
Serial output data delay time	t_{DSO}	SO	—	—	600	ns	See note 2	1, 2
Serial input data setup time	t_{SSI}	SI	1000	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	500	—	—	ns		1

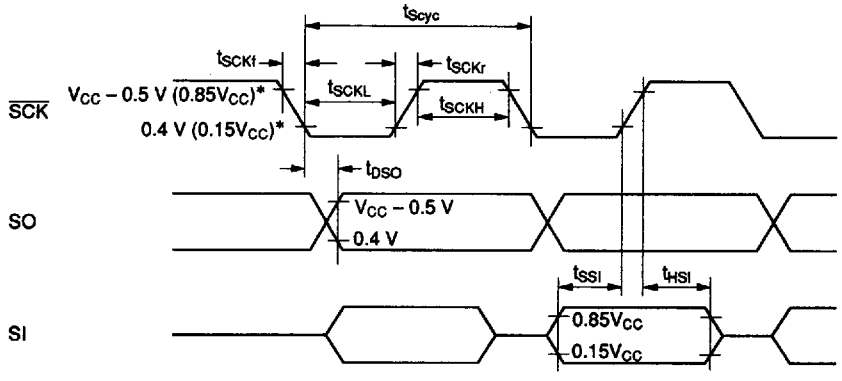
Refer to notes on the following page.

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	300	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	300	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	600	ns	See note 2	1, 2
Serial input data setup time	t_{SSI}	SI	1000	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	500	—	—	ns		1

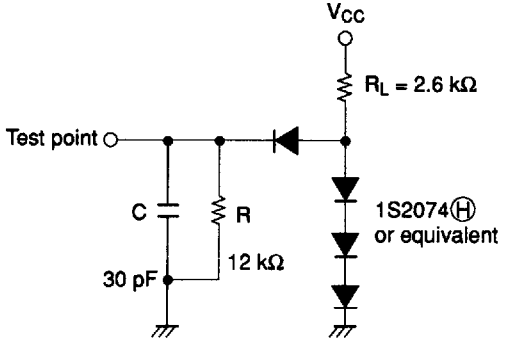
Refer to notes on the following page.

Notes: 1. Timing of serial interface

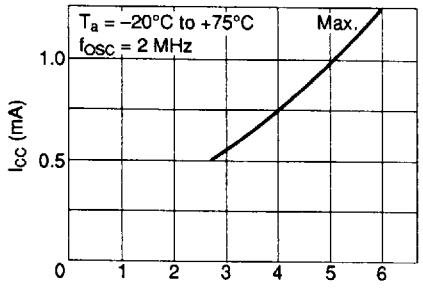


Note: * V_{CC} – 0.5 V and 0.4 V are the threshold voltages for transmit clock output.
$0.85V_{CC}$ and $0.15V_{CC}$ are the threshold voltages for transmit clock input.

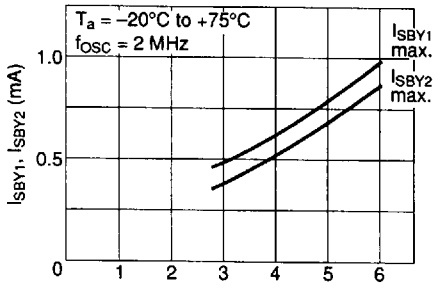
2. Timing load circuit



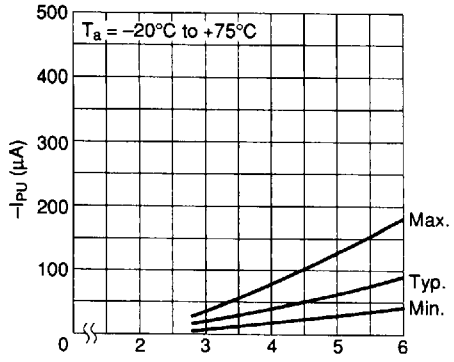
Characteristics Curves (Reference Data)



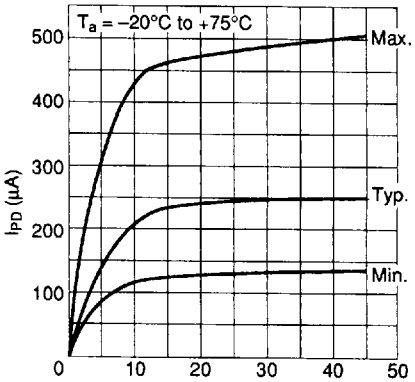
I_{SBY} vs. f_{OSC} characteristics
(crystal and ceramic oscillator)



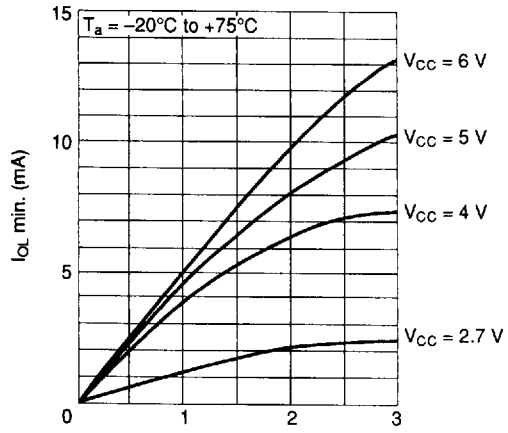
I_{SBY} vs. f_{OSC} characteristics
(crystal and ceramic oscillator)



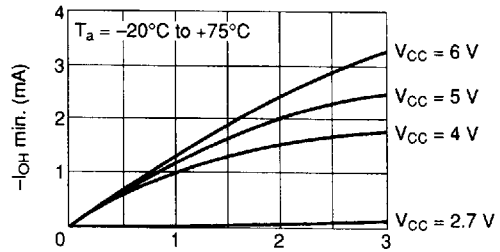
$-I_{PU}$ (pull-up MOS current) vs.
V_{CC} characteristics



I_{PD} (pull-down MOS current) vs.
($V_{CC} - V_{disp}$) characteristics

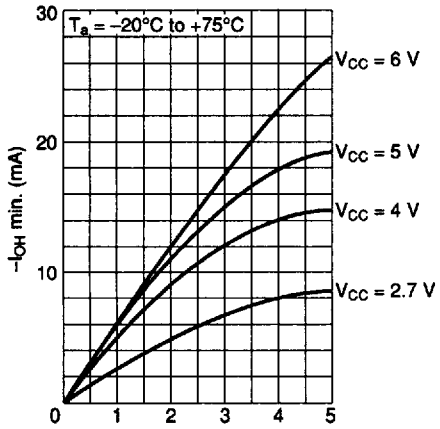


I_{OL} min. vs. V_{OL} characteristics
(standard pin)

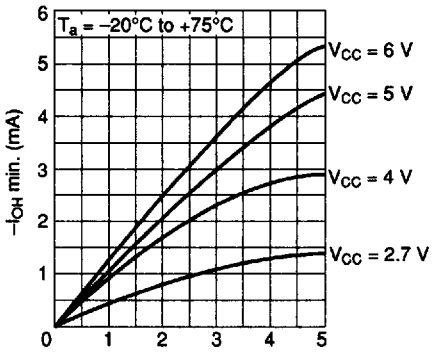


$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(standard pin CMOS)

Characteristics Curves (Reference Data) (cont)



$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(D_4 to D_{15} pins)



$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(R0 to R2 ports)

HMCS402AC Electrical Characteristics

DC Characteristics (V_{CC} = 4.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$	0.7V_{CC}	—	V_{CC} + 0.3	V		
		SI	0.7V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$	–0.3	—	0.22V_{CC}	V		
		SI	–0.3	—	0.22V_{CC}	V		
		OSC_1	–0.3	—	0.5	V		
Output high voltage	V_{OH}	$\overline{SCK}$, SO	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA	
			V_{CC} – 0.3	—	—	V	$-I_{OH}$ = 0.01 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO	—	—	0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	$\|I_{IL}\|$	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	3.0	mA	V_{CC} = 5 V, f_{OSC} = 6 MHz	2, 6
Current dissipation in standby mode	I_{SBY1}	V_{CC}	—	—	1.8	mA	Maximum logic operation V_{CC} = 5 V, f_{OSC} = 6 MHz	3, 6
	I_{SBY2}	V_{CC}	—	—	1.35	mA	Minimum logic operation V_{CC} = 5 V, f_{OSC} = 6 MHz	4, 6
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	$V_{in(\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}, $V_{in(RESET)}$ = 0 V to 0.3 V	5
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Refer to notes on the following page.

Notes: 1. Pull up MOS current and output buffer current are excluded.

2. The MCU is in the reset state. The input/output current does not flow.

   Test conditions: MCU state
   - Reset state in operation mode

   Pin state
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

3. The timer/counter operates with the fastest clock and input/output current does not flow.

   Test conditions: MCU state
   - Standby mode
   - Input/output: Reset state
   - Timer A: Divide-by-2 prescaler divide ratio
   - Timer B: Divide-by-2 prescaler divide ratio
   - Serial interface: Stop

   Pin state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

4. The timer/counter operates with the slowest clock and input/output current does not flow.

   Test conditions: MCU state
   - Standby mode
   - Input/output: Reset state
   - Timer A: Divide-by-2048 prescaler divide ratio
   - Timer B: Divide-by-2048 prescaler divide ratio
   - Serial interface: Stop

   Pin state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

5. Pull-down MOS current is excluded.

6. When $f_{OSC} = \chi$ MHz, the current dissipation in operation mode and standby mode are estimated as follows:

   Maximum value ($f_{OSC} = \chi$ MHz) = $\frac{\chi}{6} \times$ max. value (f_{OSC} = 6 MHz)

Input/Output Characteristics for Standard Pins (V_{CC} = 4.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0 to D_3, R3 to R5, R9	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0 to D_3, R3 to R5, R9	–0.3	—	$0.22V_{CC}$	V		
Output high voltage	V_{OH}	D_0 to D_3, R3 to R8	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA	1
		D_0 to D_3, R3 to R8	V_{CC} – 0.3	—	—	V	$-I_{OH}$ = 0.01 mA	1
Output low voltage	V_{OL}	D_0 to D_3, R3 to R8	—	—	0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	D_0 to D_3, R3 to R9	—	—	1	µA	V_{in} = 0 V to V_{CC}	2
Pull-up MOS current	$-I_{PU}$	D_0 to D_3, R3 to R9	30	60	120	µA	V_{CC} = 5 V, V_{in} = 0 V	3

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Pull-up MOS current and output buffer current are excluded.
3. Applied to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High Voltage Pins (V_{CC} = 4.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_4 to D_{15}, R1, R2, RA_0, RA_1	0.7 V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_4 to D_{15}, R1, R2, RA_0, RA_1	V_{CC} – 40	—	0.22V_{CC}	V		
Output high voltage	V_{OH}	D_4 to D_{15}	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA, V_{CC} = 5 V ±10%	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 9 mA	
		R0 to R2	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 3 mA, V_{CC} = 5 V ±10%	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 1.8 mA	
Output low voltage	V_{OL}	D_4 to D_{15}, R0 to R2	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
		D_4 to D_{15}, R0 to R2	—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	2
Input/output leakage current	$\|I_{IL}\|$	D_4 to D_{15}, R0 to R2 RA_0, RA_1	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_4 to D_{15} R0 to R2, RA_0, RA_1	125	250	500	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

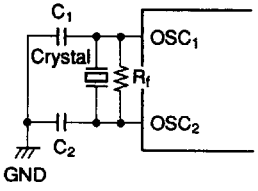
Notes: 1. Applied to I/O pins selected as with pull-down MOS by mask option.
2. Applied to I/O pins selected as without pull-down MOS (PMOS open drain) by mask option.
3. Pull-down MOS current and output buffer current are excluded.

AC Characteristics (V_{CC} = 4.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	6	6.2	MHz		
Instruction cycle time	t_{cyc}		1.29	1.33	20	µs		
Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms		1
External clock high width	t_{CPH}	OSC_1	70	—	—	ns		2
External clock low width	t_{CPL}	OSC_1	70	—	—	ns		2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT_0}$ high width	t_{IH}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_0}$ low width	t_{IL}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ high width	t_{IH}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ low width	t_{IL}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		4
Input capacitance	C_{in}	All pins	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
RESET fall time	t_{RSTf}		—	—	20	ms		4

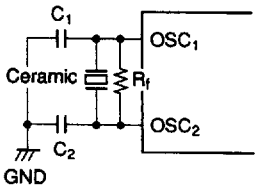
Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches 4.5 V at power-on until when the oscillator stabilizes, or after RESET goes high by MCU reset to quit the stop mode. At power-on or recovering from stop mode, apply the RESET input for more than t_{RC} to meet the necessary time for oscillator stabilization. The circuits used to measure the value are shown below. When using a crystal or ceramic oscillator, consult with the crystal and ceramic oscillator manufacture since the oscillator stabilization time depends on the circuit constant and stray capacity.

Crystal oscillator



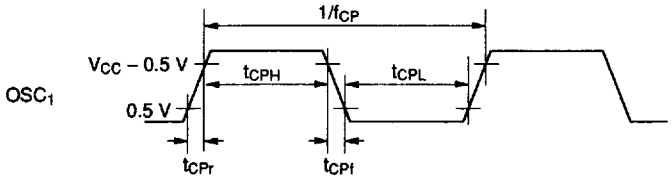
Crystal: 6.0MHz NC-18C
(Nihon Denpa Kogyo)
R_f: 1 MΩ ±2%
C_1: 20 pF ±20%
C_2: 20 pF ±20%

Ceramic oscillator

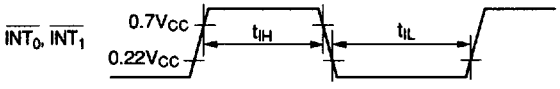


Ceramic: CSA6.00MG
(Murata)
R_f: 1 MΩ ±2%
C_1: 30 pF ±20%
C_2: 30 pF ±20%

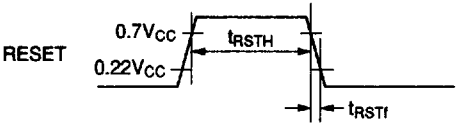
2.


1/fCP
Vcc – 0.5 V
tCPH
tCPL
OSC1
0.5 V
tCPr
tCPf

3.


INT0, INT1
0.7Vcc
tIH
tIL
0.22Vcc

4.


RESET
0.7Vcc
tRSTH
0.22Vcc
tRSTf

Serial Interface Timing Characteristics (V_{CC} = 4.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	See note 2	1, 2
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—	t_{Scyc}	See note 2	1, 2
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}	See note 2	1, 2
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	100	ns	See note 2	1, 2
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	100	ns	See note 2	1, 2
Serial output data delay time	t_{DSO}	SO	—	—	250	ns	See note 2	1, 2
Serial input data setup time	t_{SSI}	SI	300	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns		1

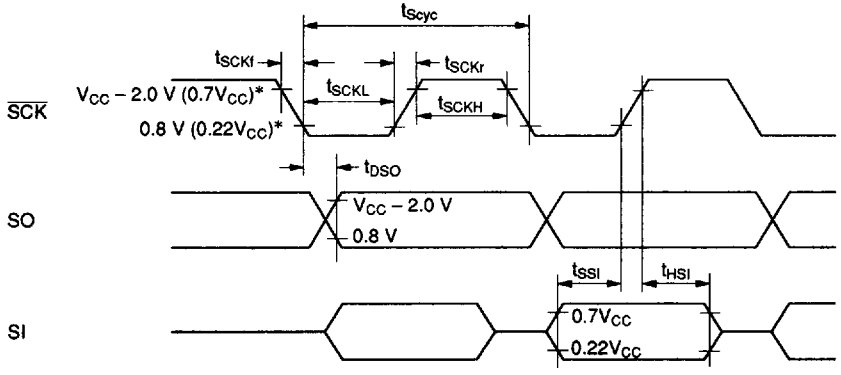
Refer to notes on the following page.

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	100	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	100	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	250	ns	See note 2	1, 2
Serial input data setup time	t_{SSI}	SI	300	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns		1

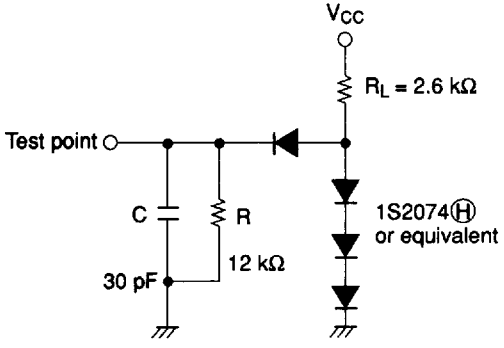
Refer to notes on the following page.

Notes: 1. Timing of serial interface

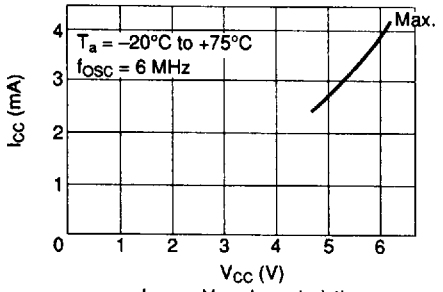


Note: * V_{CC} – 2.0 V and 0.8 V are the threshold voltages for transmit clock output.
$0.7V_{CC}$ and $0.22V_{CC}$ are the threshold voltages for transmit clock input.

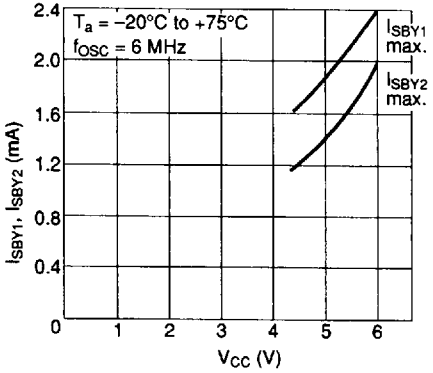
2. Timing load circuit



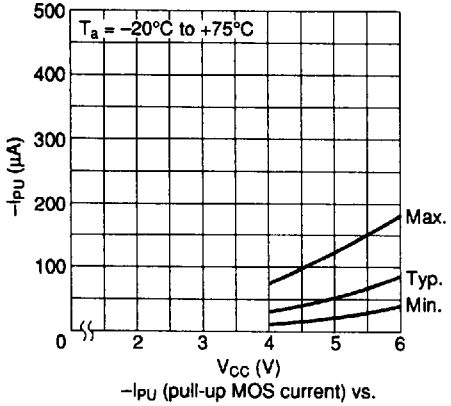
Characteristics Curves (Reference Data)



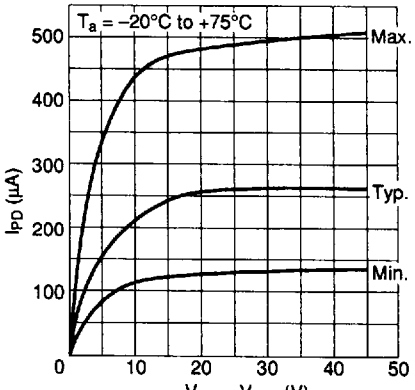
I_{CC} vs. V_{CC} characteristics
(crystal and ceramic oscillator)



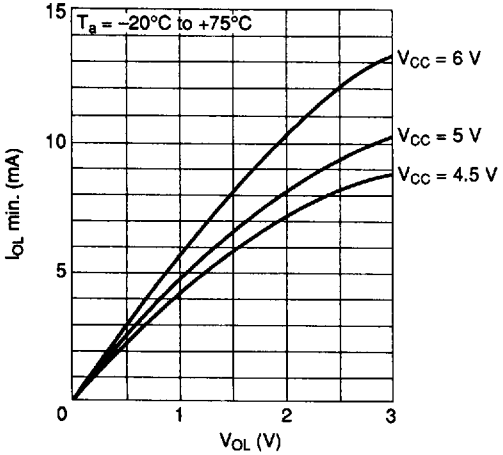
I_{SBY} vs. V_{CC} characteristics
(crystal and ceramic oscillator)



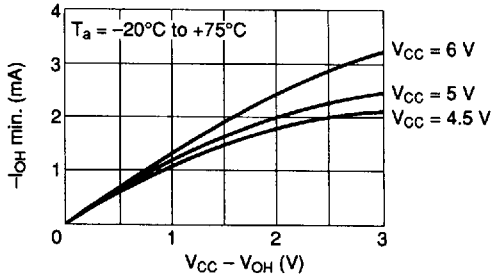
$-I_{PU}$ (pull-up MOS current) vs.
V_{CC} characteristics



I_{PD} (pull-down MOS current) vs.
($V_{CC} - V_{disp}$) characteristics

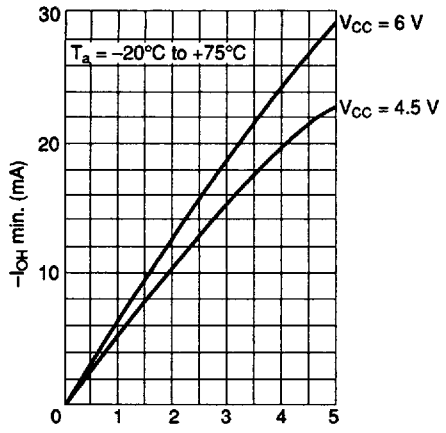


I_{OL} min. vs. V_{OL} characteristics
(standard pin)

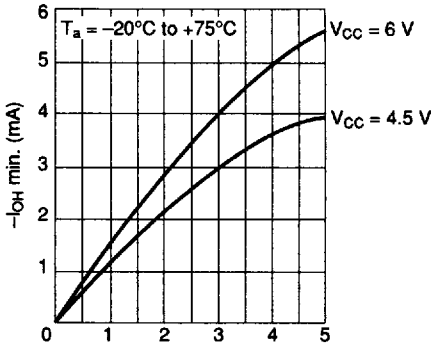


$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(standard pin CMOS)

Characteristics Curves (Reference Data) (cont)



$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(D_4 to D_{15} pins)



$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(R0 to R2 ports)

HMCS402C/CL/AC
Option List

Please check off the appropriate applications and enter the necessary information.

5-V operation:	☐ HMCS402C (HD614023)
3-V operation:	☐ HMCS402CL (HD614026)
High speed operation:	☐ HMCS402AC (HD614029)

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI type number (Hitachi's entry)	

1. I/O option

Note: I/O options masked by ▨ are not available.

Pin		I/O		I/O option					Pin		I/O		I/O option				
				A	B	C	D	E					A	B	C	D	E
D0		Standard pins	I/O				▨	▨	R3	R30	Standard pins	I/O				▨	▨
D1			I/O				▨	▨		R31		I/O				▨	▨
D2			I/O				▨	▨		R32		I/O				▨	▨
D3			I/O				▨	▨		R33		I/O				▨	▨
D4		High voltage pins	I/O	▨	▨	▨			R4	R40		I/O				▨	▨
D5			I/O	▨	▨	▨				R41		I/O				▨	▨
D6			I/O	▨	▨	▨				R42		I/O				▨	▨
D7			I/O	▨	▨	▨				R43		I/O				▨	▨
D8			I/O	▨	▨	▨			R5	R50		I/O				▨	▨
D9			I/O	▨	▨	▨				R51		I/O				▨	▨
D10			I/O	▨	▨	▨				R52		I/O				▨	▨
D11			I/O	▨	▨	▨				R53		I/O				▨	▨
D12			I/O	▨	▨	▨			R6	R60		O				▨	▨
D13			I/O	▨	▨	▨				R61		O				▨	▨
D14			I/O	▨	▨	▨				R62		O				▨	▨
D15			I/O	▨	▨	▨				R63		O				▨	▨
									R7	R70		O				▨	▨
R0	R00	High voltage pins	O	▨	▨	▨				R71		O				▨	▨
	R01		O	▨	▨	▨				R72		O				▨	▨
	R02		O	▨	▨	▨				R73		O				▨	▨
	R03		O	▨	▨	▨			R8	R80		O				▨	▨
R1	R10		I/O	▨	▨	▨				R81		O				▨	▨
	R11		I/O	▨	▨	▨				R82		O				▨	▨
	R12		I/O	▨	▨	▨				R83		O				▨	▨
	R13		I/O	▨	▨	▨			R9	R90		I			▨	▨	▨
R2	R20		I/O	▨	▨	▨				R91		I			▨	▨	▨
	R21		I/O	▨	▨	▨				R92		I			▨	▨	▨
	R22		I/O	▨	▨	▨				R93		I			▨	▨	▨
	R23		I/O	▨	▨	▨			RA	RA0		I	▨	▨	▨		
										RA1	High voltage pins	I	Use checklist RA1/Vdisp				

A: Without pull-up MOS (NMOS open drain)
B: With pull-up MOS
C: CMOS (not to be used as input)
D: Without pull-down MOS (PMOS open drain)
E: With pull-down MOS

2. RA1/Vdisp

☐ RA1: Without pull-down MOS (D)
☐ Vdisp

Note: If even one high-voltage pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

3. Divider (DIV)

■ Divide-by-8

4. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

5. System oscillator (OSC1 and OSC2)

☐ HMCS402C (5-V operation)	☐ HMCS402CL (3-V operation)	☐ HMCS402AC (high speed operation)
☐ Resistor (R_f = 20 kΩ ±2%)		
☐ Ceramic oscillator	☐ Ceramic oscillator	☐ Ceramic oscillator
☐ Crystal oscillator	☐ Crystal oscillator	☐ Crystal oscillator
☐ External clock	☐ External clock	☐ External clock

6. Stop mode

☐ Used
☐ Not used

7. Package

☐ DP-64S
☐ FP-64

HMCS404C Electrical Characteristics

DC Characteristics (V_{CC} = 4 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition		Notes
Input high voltage	V_{IH}	RESET, SCK, $\overline{INT_0}$, $\overline{INT_1}$	0.7V_{CC}	—	V_{CC} + 0.3	V			
		SI	0.7V_{CC}	—	V_{CC} + 0.3	V			
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V			
Input low voltage	V_{IL}	RESET, SCK, $\overline{INT_0}$, $\overline{INT_1}$	–0.3	—	0.22V_{CC}	V			
		SI	–0.3	—	0.22V_{CC}	V			
		OSC_1	–0.3	—	0.5	V			
Output high voltage	V_{OH}	SCK, SO	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA		
			V_{CC} – 0.3	—	—	V	$-I_{OH}$ = 0.01 mA		
Output low voltage	V_{OL}	SCK, SO	—	—	0.4	V	I_{OL} = 1.6 mA		
Input/output leakage current	$\|I_{IL}\|$	RESET, SCK, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}		1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V	Crystal or ceramic oscillator f_{OSC} = 4 MHz	2, 6
			—	—	2.4	mA		Resistor oscillator f_{OSC} = 4 MHz	2, 6
Current dissipation in standby mode	I_{SBY1}	V_{CC}	—	—	1.2	mA	Maximum logic operation V_{CC} = 5 V	Crystal or ceramic oscillator f_{OSC} = 4 MHz	3, 6
			—	—	1.6	mA		Resistor oscillator f_{OSC} = 4 MHz	3, 6
	I_{SBY2}	V_{CC}	—	—	0.9	mA	Minimum logic operation V_{CC} = 5 V	Crystal or ceramic oscillator f_{OSC} = 4 MHz	4, 6
			—	—	1.3	mA		Resistor oscillator f_{OSC} = 4 MHz	4, 6
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	$V_{in(\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}, $V_{in(RESET)}$ = 0 V to 0.3 V		5
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V			

Refer to notes on the following page.

Notes: 1. Pull up MOS current and output buffer current are excluded.

2. The MCU is in the reset state. The input/output current does not flow.

   Test conditions: MCU state
   - Reset state in operation mode

   Pin state
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

3. The timer/counter operates with the fastest clock and input/output current does not flow.

   Test conditions: MCU state
   - Standby mode
   - Input/output: Reset state
   - Timer A: Divide-by-2 prescaler divide ratio
   - Timer B: Divide-by-2 prescaler divide ratio
   - Serial interface: Stop

   Pin state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

4. The timer/counter operates with the slowest clock and input/output current does not flow.

   Test conditions: MCU state
   - Standby mode
   - Input/output: Reset state
   - Timer A: Divide-by-2048 prescaler divide ratio
   - Timer B: Divide-by-2048 prescaler divide ratio
   - Serial interface: Stop

   Pin state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

5. Pull-down MOS current is excluded.

6. When $f_{OSC} = \chi$ MHz, the current dissipation in operation mode and standby mode are estimated as follows:

   Maximum value ($f_{OSC} = \chi$ MHz) = $\frac{\chi}{4}$ × max. value (f_{OSC} = 4 MHz)

Input/Output Characteristics for Standard Pins (V_{CC} = 4 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0 to D_3, R3 to R5, R9	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0 to D_3, R3 to R5, R9	–0.3	—	0.22V_{CC}	V		
Output high voltage	V_{OH}	D_0 to D_3, R3 to R8	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA	1
		D_0 to D_3, R3 to R8	V_{CC} – 0.3	—	—	V	$-I_{OH}$ = 0.01 mA	1
Output low voltage	V_{OL}	D_0 to D_3, R3 to R8	—	—	0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	D_0 to D_3, R3 to R9	—	—	1	µA	V_{in} = 0 V to V_{CC}	2
Pull-up MOS current	$-I_{PU}$	D_0 to D_3, R3 to R9	30	60	120	µA	V_{CC} = 5 V, V_{in} = 0 V	3

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Pull-up MOS current and output buffer current are excluded.
3. Applied to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High Voltage Pins (V_{CC} = 4 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_4 to D_{15}, R1, R2, RA_0, RA_1	0.7 V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_4 to D_{15}, R1, R2, RA_0, RA_1	V_{CC} – 40	—	0.22V_{CC}	V		
Output high voltage	V_{OH}	D_4 to D_{15}	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA, V_{CC} = 5 V ±10%	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 9 mA	
		R0 to R2	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 3 mA, V_{CC} = 5 V ±10%	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 1.8 mA	
Output low voltage	V_{OL}	D_4 to D_{15}, R0 to R2	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
		D_4 to D_{15}, R0 to R2	—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	2
Input/output leakage current	$\|I_{IL}\|$	D_4 to D_{15}, R0 to R2 RA_0, RA_1	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_4 to D_{15} R0 to R2, RA_0, RA_1	125	250	500	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applied to I/O pins selected as with pull-down MOS by mask option.
2. Applied to I/O pins selected as without pull-down MOS (PMOS open drain) by mask option.
3. Pull-down MOS current and output buffer current are excluded.

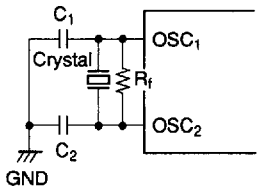
AC Characteristics (V_{CC} = 4 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item		Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Crystal or ceramic oscillator	Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz		
	Instruction cycle time	t_{cyc}		1.78	2	20	µs		
	Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms		1
Resistor oscillator	Oscillation frequency	f_{OSC}	OSC_1, OSC_2	1.8	3.0	4.2	MHz	R_f = 20 kΩ ±2%	
	Instruction cycle time	t_{cyc}		1.9	2.66	4.44	µs	R_f = 20 kΩ ±2%	
	Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	0.5	ms	R_f = 20 kΩ ±2%	1
External clock	External clock frequency	f_{CP}	OSC_1	0.4	—	4.5	MHz		2
	External clock high width	t_{CPH}	OSC_1	100	—	—	ns		2
	External clock low width	t_{CPL}	OSC_1	100	—	—	ns		2
	External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
	External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
	Instruction cycle time	t_{cyc}		1.78	—	20	µs		2
$\overline{INT_0}$ high width		t_{IH}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_0}$ low width		t_{IL}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ high width		t_{IH}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ low width		t_{IL}	$\overline{INT_1}$	2	—	—	t_{cyc}		4
RESET high width		t_{RSTH}	RESET	2	—	—	t_{cyc}		4
Input capacitance		C_{in}	All pins	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
RESET fall time		t_{RSTf}		—	—	20	ms		4

Refer to notes on the following page.

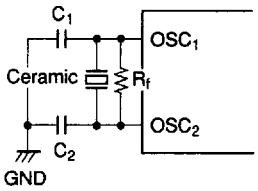
Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches 4.0 V at power-on until when the oscillator stabilizes, or after RESET goes high by MCU reset to quit the stop mode. At power-on or recovering from stop mode, apply the RESET input for more than t_{RC} to meet the necessary time for oscillator stabilization. When using a crystal or ceramic oscillator, consult with the crystal and ceramic oscillator manufacture since the oscillator stabilization time depends on the circuit constant and stray capacity.

Crystal oscillator



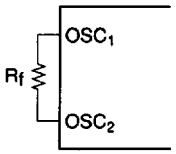
Crystal: 4.194304MHz NC-18C
(Nihon Denpa Kogyo)
R_f: 1 MΩ ±2%
C_1: 22 pF ±20%
C_2: 22 pF ±20%

Ceramic oscillator



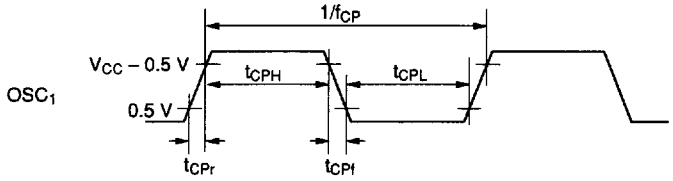
Ceramic: CSA4.00MG
(Murata)
R_f: 1 MΩ ±2%
C_1: 30 pF ±20%
C_2: 30 pF ±20%

Resistor oscillator

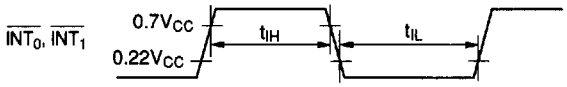


R_f: 20 MΩ ±2%

2.



3.



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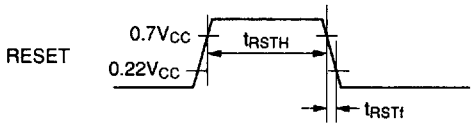


Serial Interface Timing Characteristics (V_{CC} = 4 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	See note 2	1, 2
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—	t_{Scyc}	See note 2	1, 2
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}	See note 2	1, 2
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	100	ns	See note 2	1, 2
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	100	ns	See note 2	1, 2
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	See note 2	1, 2
Serial input data setup time	t_{SSI}	SI	500	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns		1

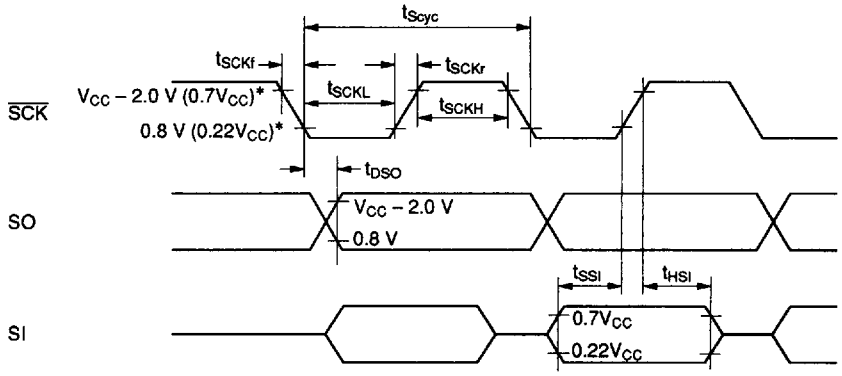
Refer to notes on the following page.

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	100	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	100	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	See note 2	1, 2
Serial input data setup time	t_{SSI}	SI	500	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns		1

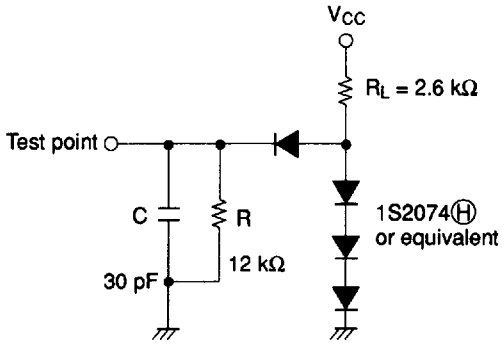
Refer to notes on the following page.

Notes: 1. Timing of serial interface

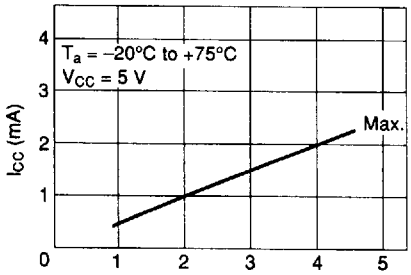


Note: * V_{CC} – 2.0 V and 0.8 V are the threshold voltages for transmit clock output.
0.7V_{CC} and 0.22V_{CC} are the threshold voltages for transmit clock input.

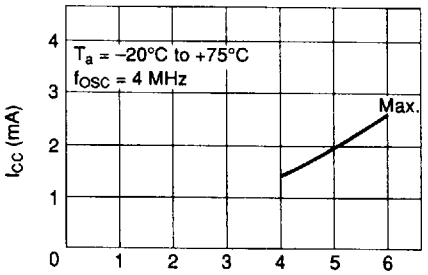
2. Timing load circuit



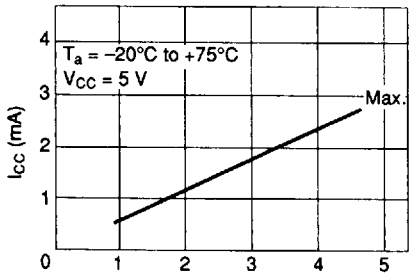
Characteristics Curves (Reference Data)



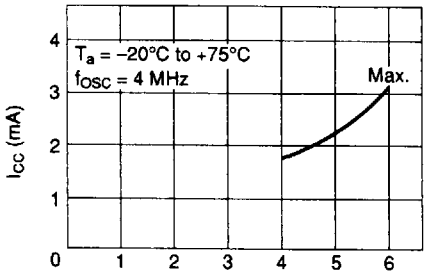
I_{CC} vs. f_{OSC} characteristics
(crystal and ceramic oscillator option)



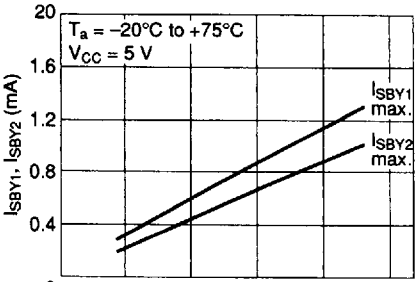
I_{CC} vs. V_{CC} characteristics
(crystal and ceramic oscillator option)



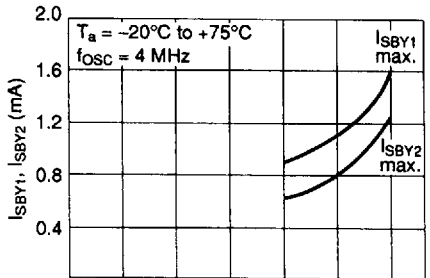
I_{CC} vs. f_{OSC} characteristics
(resistor oscillator option)



I_{CC} vs. V_{CC} characteristics
(resistor oscillator option)

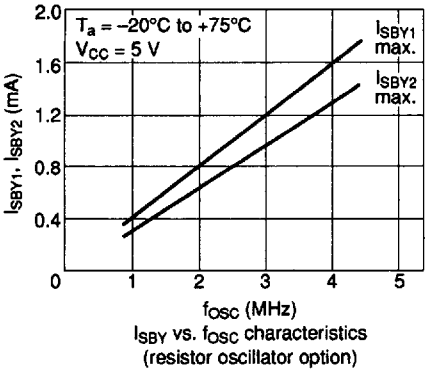


I_{SBY} vs. f_{OSC} characteristics
(crystal and ceramic oscillator option)

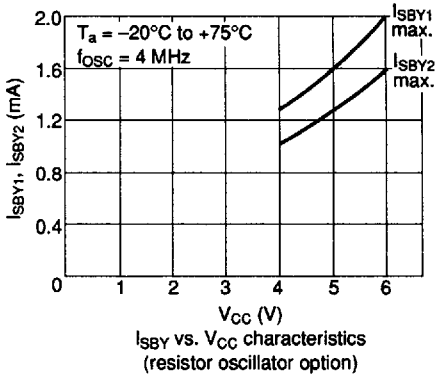


I_{SBY} vs. V_{CC} characteristics
(crystal and ceramic oscillator option)

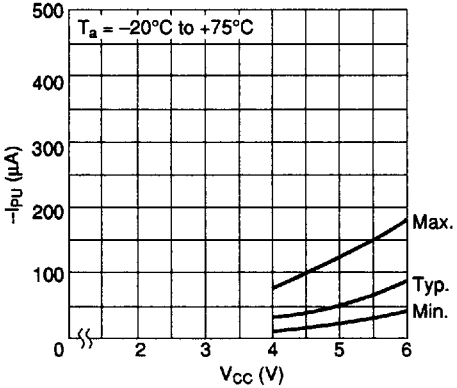
Characteristics Curves (Reference Data) (cont)



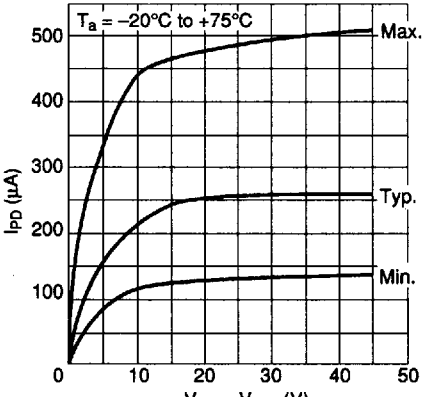
I_{SBY} vs. f_{OSC} characteristics
(resistor oscillator option)



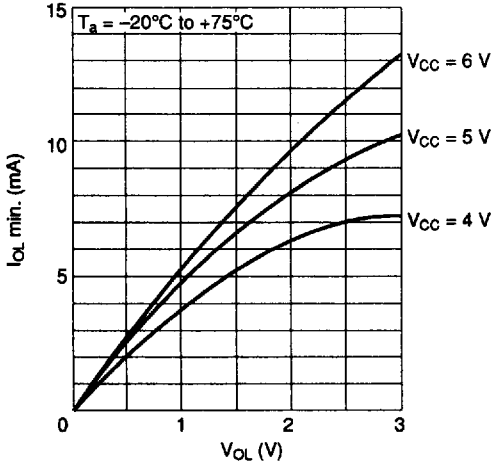
I_{SBY} vs. V_{CC} characteristics
(resistor oscillator option)



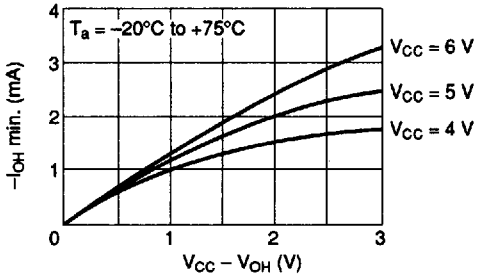
$-I_{PU}$ (pull-up MOS current) vs.
V_{CC} characteristics



I_{PD} (pull-down MOS current) vs.
($V_{CC} - V_{disp}$) characteristics

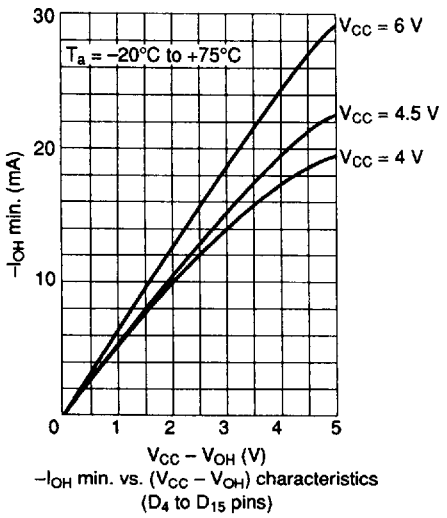


I_{OL} min. vs. V_{OL} characteristics
(standard pin)

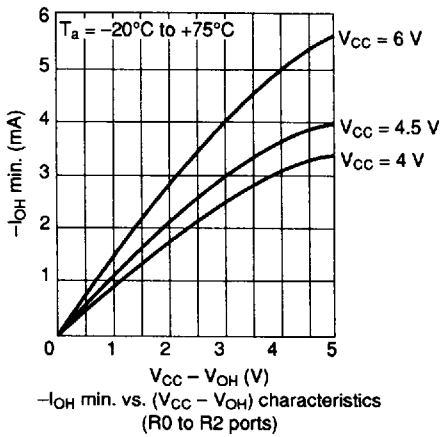


$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(standard pin CMOS)

Characteristics Curves (Reference Data) (cont)



$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(D_4 to D_{15} pins)



$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(R0 to R2 ports)

HMCS404CL Electrical Characteristics

DC Characteristics (V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $\overline{SCK}$ $\overline{INT_0}$, $\overline{INT_1}$	0.85V_{CC}	—	V_{CC} + 0.3	V		
		SI	0.85V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.3	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$	–0.3	—	0.15V_{CC}	V		
		SI	–0.3	—	0.15V_{CC}	V		
		OSC_1	–0.3	—	0.3	V		
Output high voltage	V_{OH}	$\overline{SCK}$, SO	V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.1 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO	—	—	0.4	V	I_{OL} = 0.4 mA	
Input/output leakage current	$\|I_{IL}\|$	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	0.6	mA	V_{CC} = 3 V, f_{OSC} = 2 MHz	2, 6
Current dissipation in standby mode	I_{SBY1}	V_{CC}	—	—	0.5	mA	Maximum logic operation V_{CC} = 3 V, f_{OSC} = 2 MHz	3, 6
	I_{SBY2}	V_{CC}	—	—	0.4	mA	Minimum logic operation V_{CC} = 3 V, f_{OSC} = 2 MHz	4, 6
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	$V_{in(\overline{TEST})}$ = V_{CC} – 0.2 V to V_{CC}, $V_{in(RESET)}$ = 0 V to 0.2 V	5
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Refer to notes on the following page.

Notes: 1. Pull up MOS current and output buffer are excluded.

2. The MCU is in the reset state. The input/output current does not flow.

   Test conditions: MCU state
   - Reset state in operation mode

   Pin state
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

3. The timer/counter operates with the fastest clock and input/output current does not flow.

   Test conditions: MCU state
   - Standby mode
   - Input/output: Reset state
   - Timer A: Divide-by-2 prescaler divide ratio
   - Timer B: Divide-by-2 prescaler divide ratio
   - Serial interface: Stop

   Pin state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

4. The timer/counter operates with the slowest clock and input/output current does not flow.

   Test conditions: MCU state
   - Standby mode
   - Input/output: Reset state
   - Timer A: Divide-by-2048 prescaler divide ratio
   - Timer B: Divide-by-2048 prescaler divide ratio
   - Serial interface: Stop

   Pin state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

5. Pull-down MOS current is excluded.

6. When $f_{OSC} = \chi$ MHz, the current dissipation in operation mode and standby mode are estimated as follows:

   (For divide-by-8 (D-8) option)

   Maximum value ($f_{OSC} = \chi$ MHz) = $\frac{\chi}{2}$ × max. value (f_{OSC} = 2 MHz)

Input/Output Characteristics for Standard Pins (V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0 to D_3, R3 to R5, R9	0.85V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0 to D_3, R3 to R5, R9	–0.3	—	0.15V_{CC}	V		
Output high voltage	V_{OH}	D_0 to D_3, R3 to R8	V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.1 mA	1
Output low voltage	V_{OL}	D_0 to D_3, R3 to R8	—	—	0.4	V	I_{OH} = 0.4 mA	
Input/output leakage current	$\|I_{IL}\|$	D_0 to D_3, R3 to R9	—	—	1	µA	V_{in} = 0 V to V_{CC}	2
Pull-up MOS current	$-I_{PU}$	D_0 to D_3, R3 to R9	3	15	40	µA	V_{CC} = 3 V, V_{in} = 0 V	3
		D_0 to D_3, R3 to R9	30	60	120	µA	V_{CC} = 5 V, V_{in} = 0 V	3

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Pull-up MOS current and output buffer current are excluded.
3. Applied to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High Voltage Pins (V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_4 to D_{15}, R1, R2, RA_0, RA_1	0.85 V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_4 to D_{15}, R1, R2, RA_0, RA1	V_{CC} – 40	—	0.15V_{CC}	V		
Output high voltage	V_{OH}	D_4 to D_{15}	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA, V_{CC} = 5 V ±10%	
			V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 2.5 mA	
		R0 to R2	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 3 mA, V_{CC} = 5 V ±10%	
			V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	D_4 to D_{15}, R0 to R2	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
		D_4 to D_{15}, R0 to R2	—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	2
Input/output leakage current	$\|I_{IL}\|$	D_4 to D_{15}, R0 to R2 RA_0, RA_1	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_4 to D_{15}, R0 to R2, RA_0, RA_1	125	250	500	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

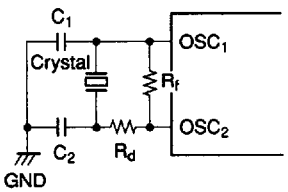
Notes: 1. Applied to I/O pins selected as with pull-down MOS by mask option.
2. Applied to I/O pins selected as without pull-down MOS (PMOS open drain) by mask option.
3. Pull-down MOS current and output buffer current are excluded.

AC Characteristics (V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	2	2.25	MHz		
Instruction cycle time	t_{cyc}		3.55	4	20	µs		
Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	60	ms		1
External clock high width	t_{CPH}	OSC_1	205	—	—	ns		2
External clock low width	t_{CPL}	OSC_1	205	—	—	ns		2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT_0}$ high width	t_{IH}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_0}$ low width	t_{IL}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ high width	t_{IH}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ low width	t_{IL}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		4
Input capacitance	C_{in}	All pins	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
RESET fall time	t_{RSTf}		—	—	15	ms		4

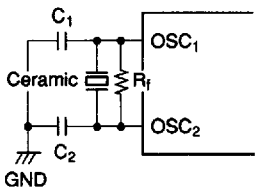
Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches 2.7 V at power-on until the oscillator stabilizes, or after RESET goes high by MCU reset to quit the stop mode. At power-on or recovering from stop mode, apply the RESET input for more than t_{RC} to meet the necessary time for oscillator stabilization. The circuits used to measure the value are shown below. When using a crystal or ceramic oscillator, consult with the crystal and ceramic oscillator manufacture since the oscillator stabilization time depends on the circuit constant and stray capacity.

Crystal oscillator



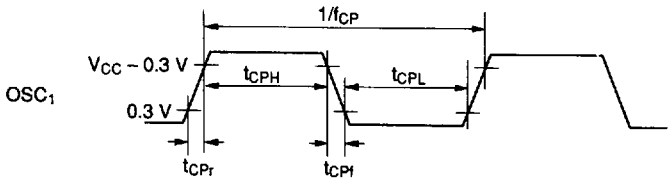
Crystal: 2.097152MHz DS-MGQ308
(Seiko Denshi)
R_f: 2 MΩ ±2%, R_d: 2.2 kΩ ±2%
C_1: 10 pF ±20%
C_2: 10 pF ±20%

Ceramic oscillator

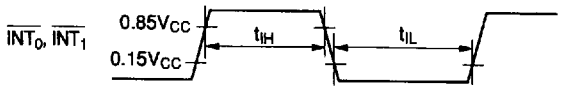


Ceramic: CSA2.000MK
(Murata)
R_f: 1 MΩ ±2%
C_1: 30 pF ±20%
C_2: 30 pF ±20%

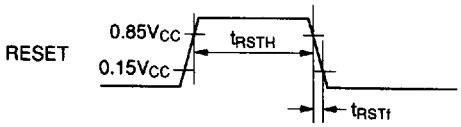
Notes (cont): 2.



3.



4.



Serial Interface Timing Characteristics (V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	See note 2	1, 2
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—	t_{Scyc}	See note 2	1, 2
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}	See note 2	1, 2
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	300	ns	See note 2	1, 2
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	300	ns	See note 2	1, 2
Serial output data delay time	t_{DSO}	SO	—	—	600	ns	See note 2	1, 2
Serial input data setup time	t_{SSI}	SI	1000	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	500	—	—	ns		1

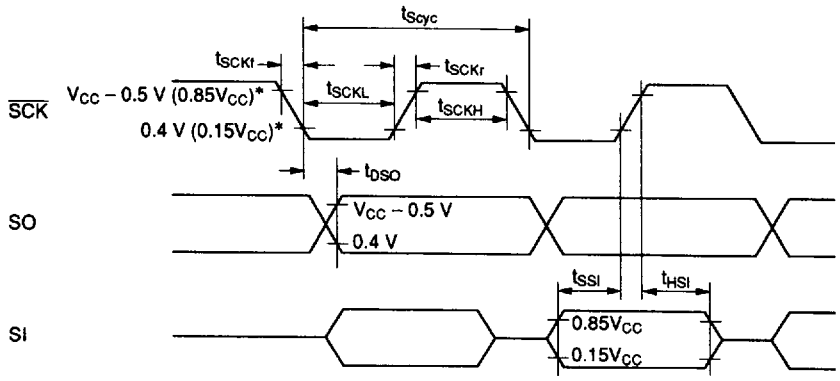
Refer to notes on the following page.

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	300	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	300	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	600	ns	See note 2	1, 2
Serial input data setup time	t_{SSI}	SI	1000	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	500	—	—	ns		1

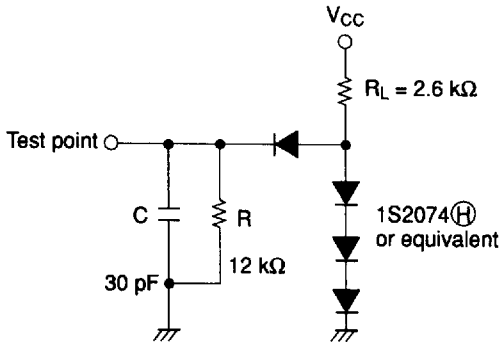
Refer to notes on the following page.

Notes: 1. Timing of serial interface

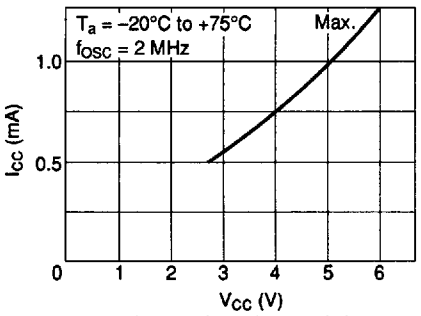


Note: * V_{CC} – 0.5 V and 0.4 V are the threshold voltages for transmit clock output.
0.85V_{CC} and 0.15V_{CC} are the threshold voltages for transmit clock input.

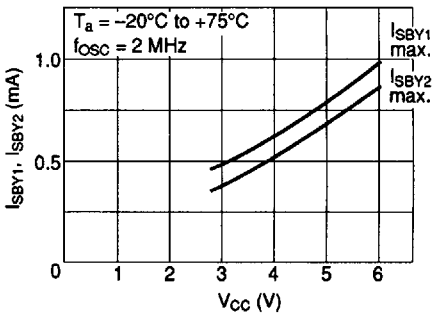
2. Timing load circuit



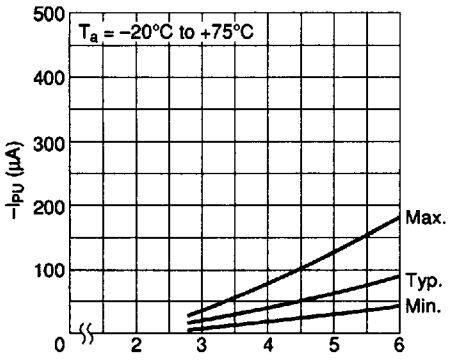
Characteristics Curves (Reference Data)



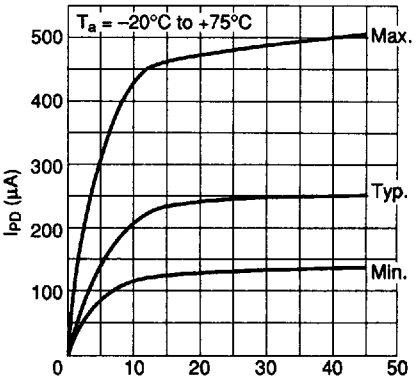
I_{SBY} vs. f_{OSC} characteristics
(crystal and ceramic oscillator)



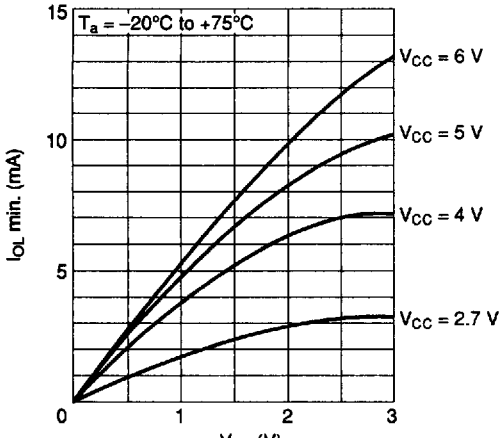
I_{SBY} vs. f_{OSC} characteristics
(crystal and ceramic oscillator)



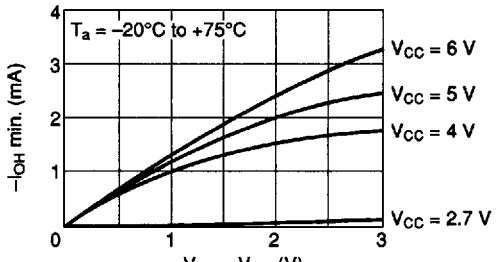
$-I_{PU}$ (pull-up MOS current) vs.
V_{CC} characteristics



I_{PD} (pull-down MOS current) vs.
($V_{CC} - V_{disp}$) characteristics

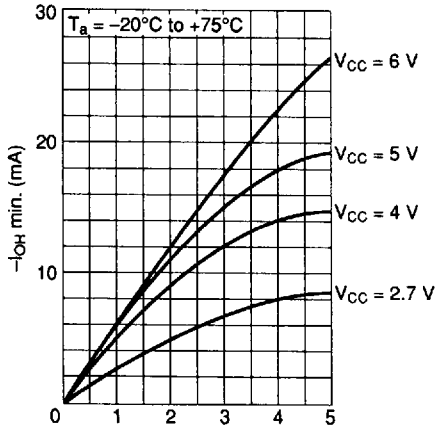


I_{OL} min. vs. V_{OL} characteristics
(standard pin)

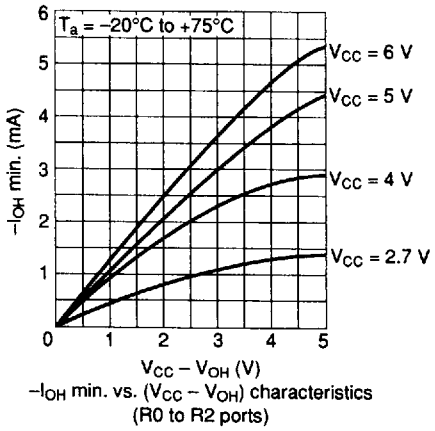


$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(standard pin CMOS)

Characteristics Curves (Reference Data) (cont)



$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(D_4 to D_{15} pins)



$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(R0 to R2 ports)

HMCS404AC Electrical Characteristics

DC Characteristics (V_{CC} = 4.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, SCK, $\overline{INT_0}$, $\overline{INT_1}$	0.7V_{CC}	—	V_{CC} + 0.3	V		
		SI	0.7V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, SCK, $\overline{INT_0}$, $\overline{INT_1}$	–0.3	—	0.22V_{CC}	V		
		SI	–0.3	—	0.22V_{CC}	V		
		OSC_1	–0.3	—	0.5	V		
Output high voltage	V_{OH}	SCK, SO	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA	
			V_{CC} – 0.3	—	—	V	$-I_{OH}$ = 0.01 mA	
Output low voltage	V_{OL}	SCK, SO	—	—	0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	$\|I_{IL}\|$	RESET, SCK, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	3.0	mA	V_{CC} = 5 V, f_{OSC} = 6 MHz	2, 6
Current dissipation in standby mode	I_{SBY1}	V_{CC}	—	—	1.8	mA	Maximum logic operation V_{CC} = 5 V, f_{OSC} = 6 MHz	3, 6
	I_{SBY2}	V_{CC}	—	—	1.35	mA	Minimum logic operation V_{CC} = 5 V, f_{OSC} = 6 MHz	4, 6
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	$V_{in(\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}, $V_{in(RESET)}$ = 0 V to 0.3 V	5
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Refer to notes on the following page.

Notes: 1. Pull up MOS current and output buffer current are excluded.

2. The MCU is in the reset state. The input/output current does not flow.

   Test conditions: MCU state
   - Reset state in operation mode

   Pin state
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

3. The timer/counter operates with the fastest clock and input/output current does not flow.

   Test conditions: MCU state
   - Standby mode
   - Input/output: Reset state
   - Timer A: Divide-by-2 prescaler divide ratio
   - Timer B: Divide-by-2 prescaler divide ratio
   - Serial interface: Stop

   Pin state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

4. The timer/counter operates with the slowest clock and input/output current does not flow.

   Test conditions: MCU state
   - Standby mode
   - Input/output: Reset state
   - Timer A: Divide-by-2048 prescaler divide ratio
   - Timer B: Divide-by-2048 prescaler divide ratio
   - Serial interface: Stop

   Pin state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

5. Pull-down MOS current is excluded.

6. When $f_{OSC} = \chi$ MHz, the current dissipation in operation mode and standby mode are estimated as follows:

   Maximum value ($f_{OSC} = \chi$ MHz) = $\frac{\chi}{6}$ × max. value (f_{OSC} = 6 MHz)

Input/Output Characteristics for Standard Pins (V_{CC} = 4.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0 to D_3, R3 to R5, R9	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0 to D_3, R3 to R5, R9	–0.3	—	0.22V_{CC}	V		
Output high voltage	V_{OH}	D_0 to D_3, R3 to R8	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA	1
		D_0 to D_3, R3 to R8	V_{CC} – 0.3	—	—	V	$-I_{OH}$ = 0.01 mA	1
Output low voltage	V_{OL}	D_0 to D_3, R3 to R8	—	—	0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	$\|I_{IL}\|$	D_0 to D_3, R3 to R9	—	—	1	µA	V_{in} = 0 V to V_{CC}	2
Pull-up MOS current	$-I_{PU}$	D_0 to D_3, R3 to R9	30	60	120	µA	V_{CC} = 5 V, V_{in} = 0 V	3

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Pull-up MOS current and output buffer current are excluded.
3. Applied to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High Voltage Pins (V_{CC} = 4.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_4 to D_{15}, R1, R2, RA_0, RA_1	0.7 V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_4 to D_{15}, R1, R2, RA_0, RA_1	V_{CC} – 40	—	0.22V_{CC}	V		
Output high voltage	V_{OH}	D_4 to D_{15}	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA, V_{CC} = 5 V ±10%	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 9 mA	
		R0 to R2	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 3 mA, V_{CC} = 5 V ±10%	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 1.8 mA	
Output low voltage	V_{OL}	D_4 to D_{15}, R0 to R2	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
		D_4 to D_{15}, R0 to R2	—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	2
Input/output leakage current	$\|I_{IL}\|$	D_4 to D_{15}, R0 to R2 RA_0, RA_1	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_4 to D_{15} R0 to R2, RA_0, RA_1	125	250	500	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

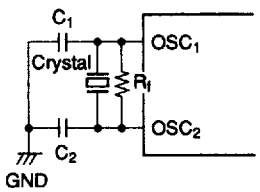
Notes: 1. Applied to I/O pins selected as with pull-down MOS by mask option.
2. Applied to I/O pins selected as without pull-down MOS (PMOS open drain) by mask option.
3. Pull-down MOS current and output buffer current are excluded.

AC Characteristics (V_{CC} = 4.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	6	6.2	MHz		
Instruction cycle time	t_{cyc}		1.29	1.33	20	µs		
Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms		1
External clock high width	t_{CPH}	OSC_1	70	—	—	ns		2
External clock low width	t_{CPL}	OSC_1	70	—	—	ns		2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT_0}$ high width	t_{IH}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_0}$ low width	t_{IL}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ high width	t_{IH}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ low width	t_{IL}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		4
Input capacitance	C_{in}	All pins	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
RESET fall time	t_{RSTf}		—	—	20	ms		4

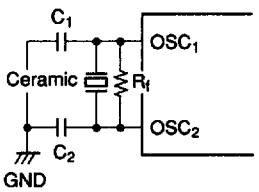
Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches 4.5 V at power-on until when the oscillator stabilizes, or after RESET goes high by MCU reset to quit the stop mode. At power-on or recovering from stop mode, apply the RESET input for more than t_{RC} to meet the necessary time for oscillator stabilization. The circuits used to measure the value are shown below. When using a crystal or ceramic oscillator, consult with the crystal and ceramic oscillator manufacture since the oscillator stabilization time depends on the circuit constant and stray capacity.

Crystal oscillator



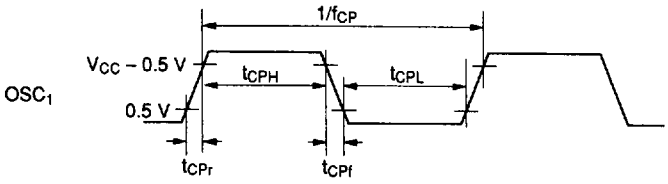
Crystal: 6.0MHz NC-18C
(Nihon Denpa Kogyo)
R_f: 1 MΩ ±2%
C_1: 20 pF ±20%
C_2: 20 pF ±20%

Ceramic oscillator

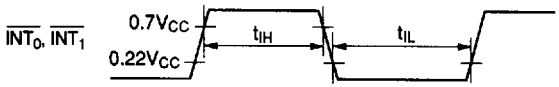


Ceramic: CSA6.00MG
(Murata)
R_f: 1 MΩ ±2%
C_1: 30 pF ±20%
C_2: 30 pF ±20%

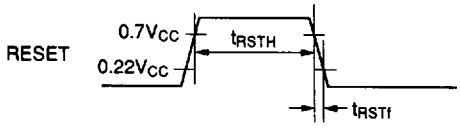
Notes (cont): 2.



3.



4.



Serial Interface Timing Characteristics (V_{CC} = 4.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	See note 2	1, 2
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—	t_{Scyc}	See note 2	1, 2
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}	See note 2	1, 2
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	100	ns	See note 2	1, 2
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	100	ns	See note 2	1, 2
Serial output data delay time	t_{DSO}	SO	—	—	250	ns	See note 2	1, 2
Serial input data setup time	t_{SSI}	SI	300	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns		1

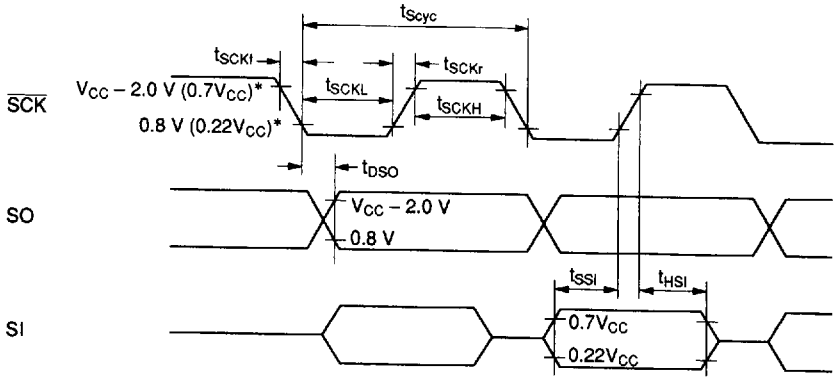
Refer to notes on the following page.

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	100	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	100	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	250	ns	See note 2	1, 2
Serial input data setup time	t_{SSI}	SI	500	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns		1

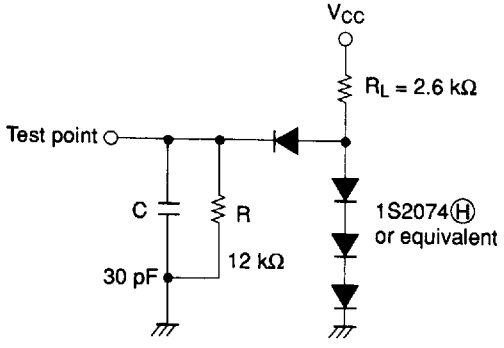
Refer to notes on the following page.

Notes: 1. Timing of serial interface

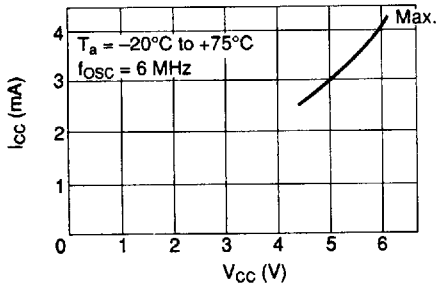


Note: * V_{CC} – 2.0 V and 0.8 V are the threshold voltages for transmit clock output.
$0.7V_{CC}$ and $0.22V_{CC}$ are the threshold voltages for transmit clock input.

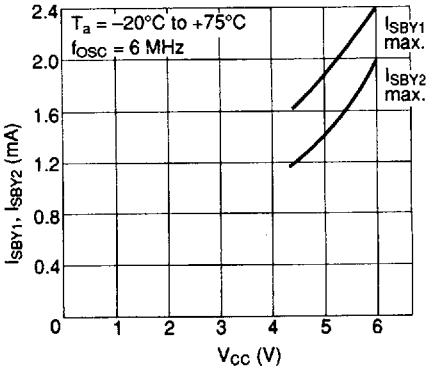
2. Timing load circuit



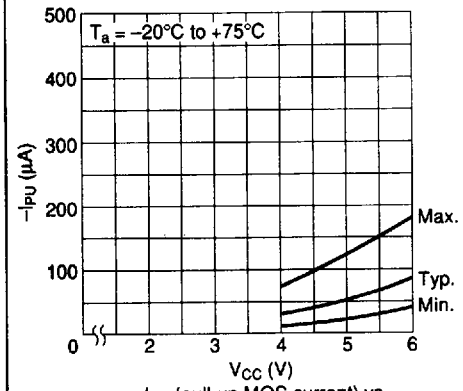
Characteristics Curves (Reference Data)



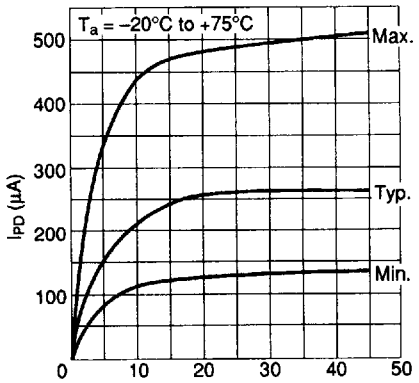
I_{CC} vs. V_{CC} characteristics
(crystal and ceramic oscillator)



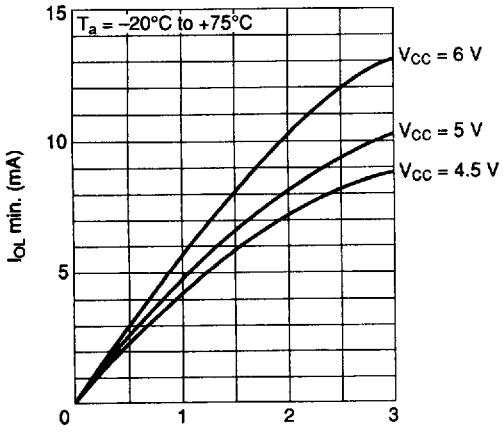
I_{SBY} vs. V_{CC} characteristics
(crystal and ceramic oscillator)



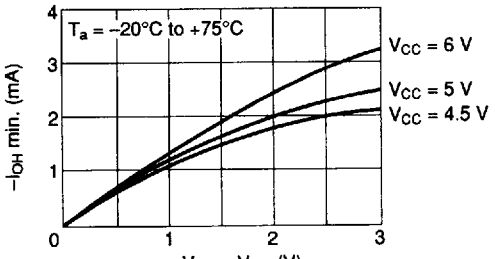
$-I_{PU}$ (pull-up MOS current) vs.
V_{CC} characteristics



I_{PD} (pull-down MOS current) vs.
($V_{CC} - V_{disp}$) characteristics

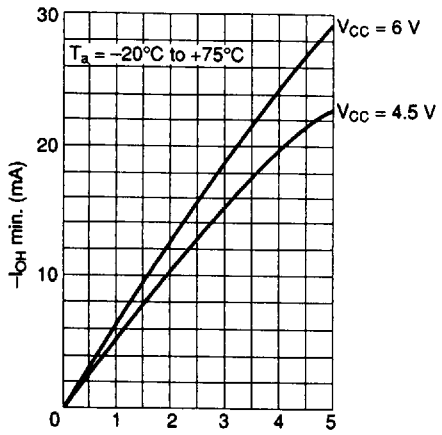


I_{OL} min. vs. V_{OL} characteristics
(standard pin)

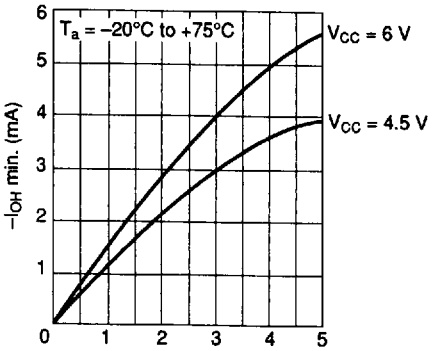


$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(standard pin CMOS)

Characteristics Curves (Reference Data) (cont)



$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(D_4 to D_{15} pins)



$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) characteristics
(R0 to R2 ports)

HMCS404C/CL/AC
Option List

Please check off the appropriate applications and enter the necessary information.

5-V operation:	☐ HMCS404C (HD614043)
3-V operation:	☐ HMCS404CL (HD614046)
High speed operation:	☐ HMCS404AC (HD614049)

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI type number (Hitachi's entry)	

1. I/O option

Note: I/O options masked by ▒ are not available.

Pin		I/O		I/O option				
				A	B	C	D	E
D0		Standard pins	I/O				▒	▒
D1			I/O				▒	▒
D2			I/O				▒	▒
D3			I/O				▒	▒
D4		High voltage pins	I/O	▒	▒	▒		
D5			I/O	▒	▒	▒		
D6			I/O	▒	▒	▒		
D7			I/O	▒	▒	▒		
D8			I/O	▒	▒	▒		
D9			I/O	▒	▒	▒		
D10			I/O	▒	▒	▒		
D11			I/O	▒	▒	▒		
D12			I/O	▒	▒	▒		
D13			I/O	▒	▒	▒		
D14			I/O	▒	▒	▒		
D15			I/O	▒	▒	▒		
R0	R00	High voltage pins	O	▒	▒	▒		
	R01		O	▒	▒	▒		
	R02		O	▒	▒	▒		
	R03		O	▒	▒	▒		
R1	R10		I/O	▒	▒	▒		
	R11		I/O	▒	▒	▒		
	R12		I/O	▒	▒	▒		
	R13		I/O	▒	▒	▒		
R2	R20		I/O	▒	▒	▒		
	R21		I/O	▒	▒	▒		
	R22		I/O	▒	▒	▒		
	R23		I/O	▒	▒	▒		

Pin		I/O		I/O option				
				A	B	C	D	E
R3	R30	Standard pins	I/O					
	R31		I/O					
	R32		I/O					
	R33		I/O					
R4	R40		I/O					
	R41		I/O					
	R42		I/O					
	R43		I/O					
R5	R50		I/O					
	R51		I/O					
	R52		I/O					
	R53		I/O					
R6	R60		O					
	R61		O					
	R62		O					
	R63		O					
R7	R70		O					
	R71		O					
	R72		O					
	R73		O					
R8	R80		O					
	R81		O					
	R82		O					
	R83		O					
R9	R90		I				▒	▒
	R91		I				▒	▒
	R92		I				▒	▒
	R93		I				▒	▒
RA	RA0	High voltage pins	I	▒	▒	▒		
	RA1		I	Use checklist RA1/Vdisp				

A: Without pull-up MOS (NMOS open drain)
B: With pull-up MOS
C: CMOS (not to be used as input)
D: Without pull-down MOS (PMOS open drain)
E: With pull-down MOS

2. RA1/Vdisp

☐ RA1: Without pull-down MOS (D)
☐ Vdisp

Note: If even one high-voltage pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

3. Divider (DIV)

■ Divide-by-8

4. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

5. Oscillator (OSC1 and OSC2)

☐ HMCS404C (5-V operation)	☐ HMCS404CL (3-V operation)	☐ HMCS404AC (high speed operation)
☐ Resistor (R_f = 20 kΩ ±2%)		
☐ Ceramic oscillator	☐ Ceramic oscillator	☐ Ceramic oscillator
☐ Crystal oscillator	☐ Crystal oscillator	☐ Crystal oscillator
☐ External clock	☐ External clock	☐ External clock

6. Stop mode

☐ Used
☐ Not used

7. Package

☐ DP-64S
☐ FP-64

HMCS408C/CL/AC Electrical Characteristics

DC Characteristics (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, HMCS408C: V_{CC} = 3.5 V to 6 V, HMCS408CL: V_{CC} = 2.5 V to 6 V, HMCS408AC: V_{CC} = 4.5 V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $\overline{SCK}$, $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$	$0.8V_{CC}$		V_{CC} + 0.3	V		
		SI	$0.7V_{CC}$		V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5		V_{CC} + 0.3	V	HMCS408C/AC	
			V_{CC} – 0.3		V_{CC} + 0.3	V	HMCS408CL	
Input low voltage	V_{IL}	RESET, $\overline{SCK}$, $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$	–0.3		$0.2V_{CC}$	V		
		SI	–0.3		$0.3V_{CC}$	V		
		OSC_1	–0.3		0.5	V	HMCS408C/AC	
			–0.3		0.3	V	HMCS408CL	
Output high voltage	V_{OH}	$\overline{SCK}$, SO	V_{CC} – 1.0			V	HMCS408C/AC: $-I_{OH}$ = 1.0 mA	
			V_{CC} – 0.5			V	HMCS408C/AC: $-I_{OH}$ = 0.5 mA; HMCS408CL: $-I_{OH}$ = 0.3 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO	—		0.4	V	HMCS408C/AC: I_{OL} = 1.6 mA; HMCS408CL: I_{OL} = 0.4 mA	
Input/output leakage current	$\|I_{IL}\|$	RESET, $\overline{SCK}$, $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$, SI, SO, OSC_1	—		1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—		2.3	mA	HMCS408C: V_{CC} = 5 V; f_{OSC} = 4 MHz, ÷ 8, or f_{OSC} = 2 MHz, ÷4	2, 5
			—		1.1	mA	HMCS408CL: V_{CC} = 3 V; f_{OSC} = 4 MHz, ÷ 16, or f_{OSC} = 2 MHz, ÷ 8	2, 5
			—		4.5	mA	HMCS408AC: V_{CC} = 5 V; f_{OSC} = 4 MHz, ÷ 4, or f_{OSC} = 8 MHz, ÷ 8	2, 5

DC Characteristics (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, HMCS408C: V_{CC} = 3.5 V to 6 V, HMCS408CL: V_{CC} = 2.5 V to 6 V, HMCS408AC: V_{CC} = 4.5 V to 6 V) (cont)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	1.2	mA	HMCS408C: V_{CC} = 5 V; f_{OSC} = 4 MHz, ÷ 8 or f_{OSC} = 2 MHz, ÷ 4	3, 5
			—	—	0.5	mA	HMCS408CL: V_{CC} = 3 V; f_{OSC} = 4 MHz, ÷ 16, or f_{OSC} = 2 MHz, ÷ 8	3, 5
			—	—	1.7	mA	HMCS408AC: V_{CC} = 5 V; f_{OSC} = 4 MHz, ÷ 4, or f_{OSC} = 8 MHz, ÷8	3, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	HMCS408C/AC: $V_{in(\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}; V_{CC}, $V_{in(RESET)}$ = 0 V to 0.3 V HMCS408CL: $V_{in(\overline{TEST})}$ = V_{CC} – 0.2 V to V_{CC}; V_{CC}, $V_{in(RESET)}$ = 0 V to 0.2 V	4
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Excluding pull up MOS current and output buffer current.
2. The MCU is in the reset state. Input/output current does not flow.
   - MCU in reset state, operation mode
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}
3. The timer/counter operates with the fastest clock. Input/output current does not flow.
   - MCU in standby mode
   - Input/output in reset state
   - Serial interface: Stop
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}
4. Excluding pull-down MOS current.
5. When f_{OSC} = x MHz, estimate the current dissipation as follows:
   HMCS408C/AC: Maximum value at x MHz = (x/4) × (max. value at 4 MHz)
   HMCS408CL: Maximum value at x MHz = (x/2) × (max. value at 2 MHz)

Input/Output Characteristics for Standard Pins (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, HMCS408C: V_{CC} = 3.5 V to 6 V, HMCS408CL: V_{CC} = 2.5 V to 6 V, HMCS408AC: V_{CC} = 4.5 V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0 to D_3, R3 to R5, R9	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0 to D_3, R3 to R5, R9	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	D_0 to D_3, R3 to R8	V_{CC} – 1.0	—	—	V	HMCS408C/AC: $-I_{OH}$ = 1.0 mA	1
		D_0 to D_3, R3 to R8	V_{CC} – 0.5	—	—	V	HMCS408C/AC: $-I_{OH}$ = 0.5 mA HMCS408CL: $-I_{OH}$ = 0.3 mA	1
Output low voltage	V_{OL}	D_0 to D_3, R3 to R8	—	—	0.4	V	HMCS408C/AC: I_{OL} = 1.6 mA HMCS408CL: I_{OH} = 0.4 mA	
Input/output leakage current	$\|I_{IL}\|$	D_0 to D_3, R3 to R9	—	—	1	µA	V_{in} = 0 V to V_{CC}	2
Pull-up MOS current	$-I_{PU}$	D_0 to D_3, R3 to R9	30	60	150	µA	V_{CC} = 5 V, V_{in} = 0 V	3
		D_0 to D_3, R3 to R9	3	15	50	µA	HMCS408CL only: V_{CC} = 3 V, V_{in} = 0 V	3

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Pull-up MOS current and output buffer current are excluded.
3. Applied to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High Voltage Pins (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, HMCS408C: V_{CC} = 3.5 V to 6 V, HMCS408CL: V_{CC} = 2.5 V to 6 V, HMCS408AC: V_{CC} = 4.5 V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_4 to D_{15}, R1, R2, RA_0, RA_1	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_4 to D_{15}, R1, R2, RA_0, RA_1	V_{CC} – 40	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	D_4 to D_{15}	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA, V_{CC} = 5 V ±20%	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 10 mA, V_{CC} = 5 V ±20%	
			V_{CC} – 1.0	—	—	V	HMCS408C/AC: $-I_{OH}$ = 4 mA HMCS408CL: $-I_{OH}$ = 2.5 mA	
		R0 to R2	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 3 mA, V_{CC} = 5 V ±20%	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 2 mA, V_{CC} = 5 V ±20%	
			V_{CC} – 1.0	—	—	V	HMCS408C/AC: $-I_{OH}$ = 0.8 mA HMCS408CL: $-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	D_4 to D_{15}, R0 to R2	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
		D_4 to D_{15}, R0 to R2	—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	2
Input/output leakage current	$\|I_{IL}\|$	D_4 to D_{15}, R0 to R2, RA_0, RA_1	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_4 to D_{15}, R0 to R2, RA_0, RA_1	125	250	600	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applied to I/O pins selected as with pull-up MOS by mask option.
2. Applied to I/O pins selected as without pull-up MOS (PMOS open drain) by mask option.
3. Pull-down MOS current and output buffer current are excluded.

AC Characteristics (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, HMCS408C: V_{CC} = 3.5 V to 6 V, HMCS408CL: V_{CC} = 2.5 V to 6 V, HMCS408AC: V_{CC} = 4.5 V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz	HMCS408C: divide-by-8	
			0.2	2	2.25	MHz	HMCS408C: divide-by-4	
			0.8	4	4.5	MHz	HMCS408CL: divide-by-16	
			0.4	2	2.25	MHz	HMCS408CL: divide-by-8	
			0.2	4	4.5	MHz	HMCS408AC: divide-by-4	
			0.4	8	9	MHz	HMCS408AC: divide-by-8	
Instruction cycle time	t_{cyc}		1.78	2	20	µs	HMCS408C	
			3.55	4	20	µs	HMCS408CL	
			0.89	1	20	µs	HMCS408AC	
Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms	HMCS408C/AC	1
			—	—	60	ms	HMCS408CL	1
External clock high and low widths	t_{CPH}, t_{CPL}	OSC_1	92	—	—	ns	HMCS408C: divide-by-8 HMCS408CL: divide-by-16 HMCS408AC: divide-by-4	2
			203	—	—	ns	HMCS408C: divide-by-4 HMCS408CL: divide-by-8	2
			41	—	—	ns	HMCS408AC: divide-by-8	

AC Characteristics (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, HMCS408C: V_{CC} = 3.5 V to 6 V, HMCS408CL: V_{CC} = 2.5 V to 6 V, HMCS408AC: V_{CC} = 4.5 V to 6 V) (cont)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT_0}$ high width	t_{IH}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_0}$ low width	t_{IL}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ high width	t_{IH}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ low width	t_{IL}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		4
Input capacitance	C_{in}	All pins	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
RESET fall time	t_{RSTf}		—	—	20	ms	HMCS408C/AC	4
			—	—	15	ms	HMCS408CL	4

Notes: 1. The oscillator stabilization time is period from when V_{CC} reaches its minimum allowable voltage at power-on until when the oscillator stabilizes, or after RESET goes high. At power-on or recovering from stop mode, apply the RESET input for more than t_{RC} to meet the necessary time for oscillator stabilization. When using a crystal or ceramic oscillator, consult with the crystal and ceramic oscillator manufacture since the oscillator stabilization time depends on the circuit constant and stray capacitance.
2. See figure 25.
3. See figure 26.
4. See figure 27.

Serial Interface Timing Characteristics (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, HMCS408C: V_{CC} = 3.5 V to 6 V, HMCS408CL: V_{CC} = 2.5 V to 6 V, HMCS408AC: V_{CC} = 4.5 V to 6 V)

During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1, 2
Transmit clock high and low width	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1, 2
Transmit clock rise and fall times	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	—	—	100	ns	HMCS408C/AC	1, 2
			—	—	300	ns	HMCS408CL	1, 2
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	HMCS408C	1, 2
			—	—	600	ns	HMCS408CL	1, 2
			—	—	250	ns	HMCS408AC	1, 2
Serial input data setup time	t_{SSI}	SI	500	—	—	ns	HMCS408C	1
			1000	—	—	ns	HMCS408CL	1
			300	—	—	ns	HMCS408AC	1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns	HMCS408C/AC	1
			500	—	—	ns	HMCS408CL	1

Refer to notes on the next page.

Serial Interface Timing Characteristics (GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, HMCS408C: V_{CC} = 3.5 V to 6 V, HMCS408CL: V_{CC} = 2.5 V to 6 V, HMCS408AC: V_{CC} = 4.5 V to 6 V)

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high and low width	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1
Transmit clock rise and fall times	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	—	—	100	ns	HMCS408C/AC	1
			—	—	300	ns	HMCS408CL	1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	HMCS408C	1, 2
			—	—	600	ns	HMCS408CL	1, 2
			—	—	250	ns	HMCS408AC	1, 2
Serial input data setup time	t_{SSI}	SI	500	—	—	ns	HMCS408C	1
			1000	—	—	ns	HMCS408CL	1
			300	—	—	ns	HMCS408AC	1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns	HMCS408C/AC	1
			500	—	—	ns	HMCS408CL	1

Notes: 1. See figure 28.
2. See figure 29.

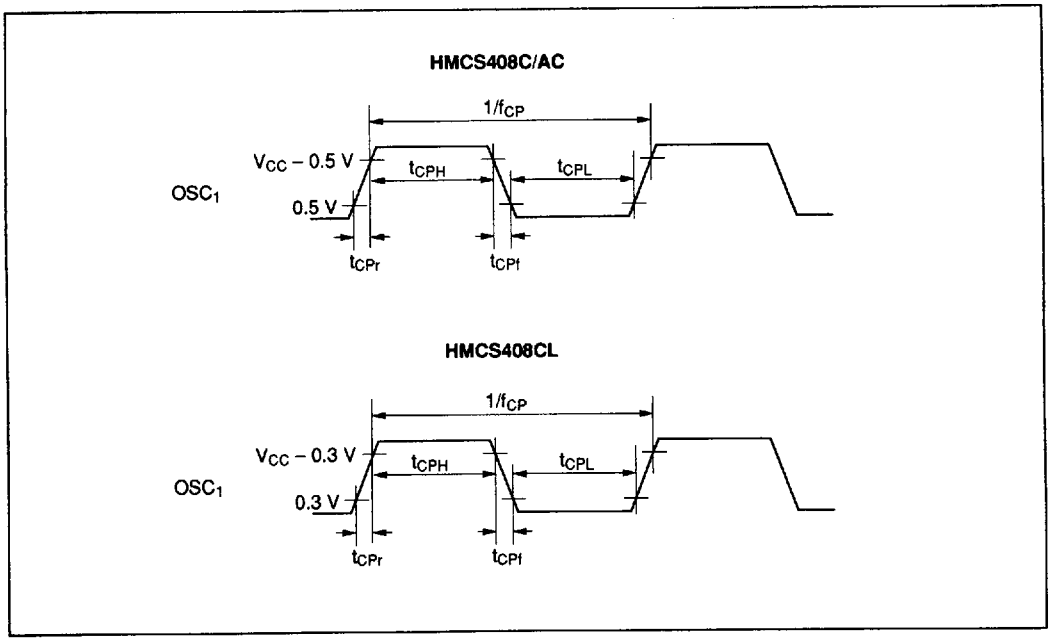


Figure 25 Oscillator Timing

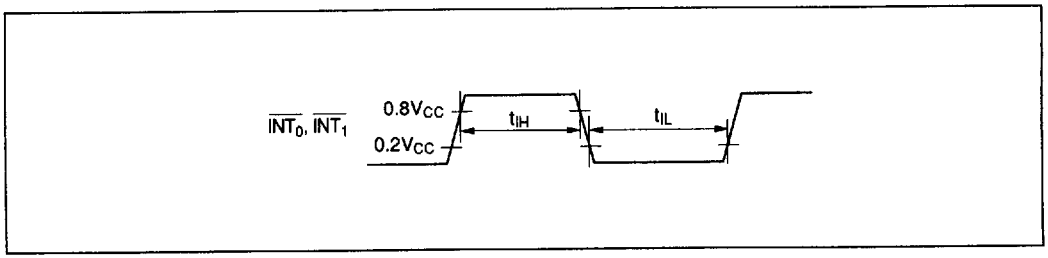


Figure 26 Interrupt Timing

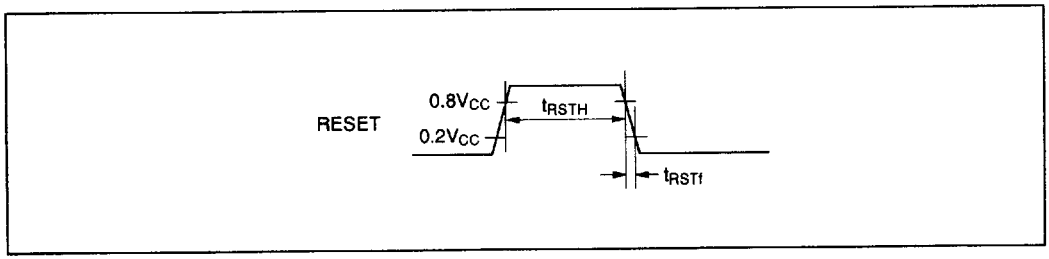
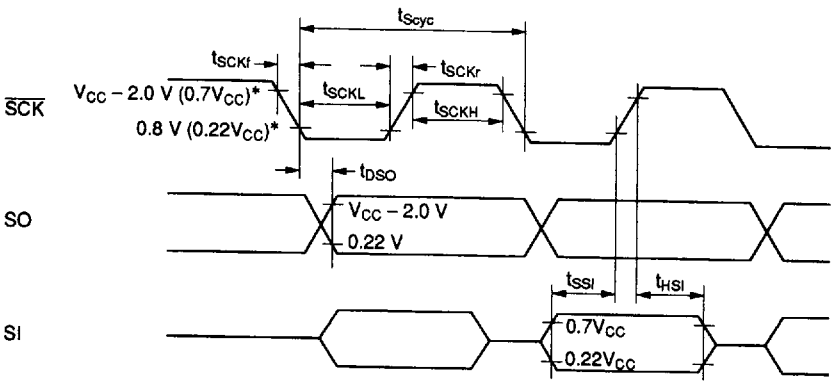


Figure 27 Reset Timing



Note: * V_{CC} – 2.0 V and 0.8 V are the threshold voltages for transmit clock output.
$0.7V_{CC}$ and $0.22V_{CC}$ are the threshold voltages for transmit clock input.

Figure 28 Serial Interface Timing

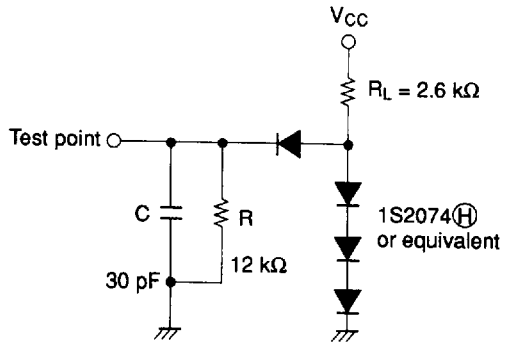


Figure 29 Timing Load Circuit

HMCS408C/CL/AC
Option List

Date of order	
Customer	
Dept.	
Name	
ROM code name	
LSI type number (Hitachi's entry)	

Please check off the appropriate applications and enter the necessary information.

5-V operation:	☐ HMCS408C (HD614081)
3-V operation:	☐ HMCS408CL (HD614086)
High speed operation:	☐ HMCS408AC (HD614089)

1. I/O option

Note: I/O options masked by ▒ are not available.

Pin		I/O	I/O option				
			A	B	C	D	E
D0	Standard pins	I/O				▒	▒
D1		I/O				▒	▒
D2		I/O				▒	▒
D3		I/O				▒	▒
D4	High voltage pins	I/O	▒	▒	▒		
D5		I/O	▒	▒	▒		
D6		I/O	▒	▒	▒		
D7		I/O	▒	▒	▒		
D8		I/O	▒	▒	▒		
D9		I/O	▒	▒	▒		
D10		I/O	▒	▒	▒		
D11		I/O	▒	▒	▒		
D12		I/O	▒	▒	▒		
D13		I/O	▒	▒	▒		
D14		I/O	▒	▒	▒		
D15		I/O	▒	▒	▒		
R0	R00	O	▒	▒	▒		
	R01	O	▒	▒	▒		
	R02	O	▒	▒	▒		
	R03	O	▒	▒	▒		
R1	R10	I/O	▒	▒	▒		
	R11	I/O	▒	▒	▒		
	R12	I/O	▒	▒	▒		
	R13	I/O	▒	▒	▒		
R2	R20	I/O	▒	▒	▒		
	R21	I/O	▒	▒	▒		
	R22	I/O	▒	▒	▒		
	R23	I/O	▒	▒	▒		

Pin		I/O	I/O option				
			A	B	C	D	E
R3	R30	I/O				▒	▒
	R31	I/O				▒	▒
	R32	I/O				▒	▒
	R33	I/O				▒	▒
R4	R40	I/O				▒	▒
	R41	I/O				▒	▒
	R42	I/O				▒	▒
	R43	I/O				▒	▒
R5	R50	I/O				▒	▒
	R51	I/O				▒	▒
	R52	I/O				▒	▒
	R53	I/O				▒	▒
R6	R60	O				▒	▒
	R61	O				▒	▒
	R62	O				▒	▒
	R63	O				▒	▒
R7	R70	O				▒	▒
	R71	O				▒	▒
	R72	O				▒	▒
	R73	O				▒	▒
R8	R80	O				▒	▒
	R81	O				▒	▒
	R82	O				▒	▒
	R83	O				▒	▒
R9	R90	I			▒	▒	▒
	R91	I			▒	▒	▒
	R92	I			▒	▒	▒
	R93	I			▒	▒	▒
RA	RA0	I	▒	▒	▒		
	RA1	I	Use checklist RA1/Vdisp				

Standard pins

High voltage pins

A: Without pull-up MOS (NMOS open drain)
B: With pull-up MOS
C: CMOS (not be used as input)
D: Without pull-down MOS (PMOS open drain)
E: With pull-down MOS

2. RA1/Vdisp

☐ RA1: Without pull-down MOS (D)
☐ Vdisp

Note: If even one high-voltage pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

3. Divider (DIV)

Divider	4	8	16
HMCS408C	☐	☐	
HMCS408CL		☐	☐
HMCS408AC	☐	☐	

4. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

5. System oscillator (OSC1 and OSC2)

☐ HMCS408C (5-V operation)	☐ HMCS408CL (3-V operation)	☐ HMCS408AC (high speed operation)
☐ Ceramic oscillator	☐ Ceramic oscillator	☐ Ceramic oscillator
☐ Crystal oscillator	☐ Crystal oscillator	☐ Crystal oscillator
☐ External clock	☐ External clock	☐ External clock

6. Stop mode

☐ Used
☐ Not used

7. Package

☐ DP-64S
☐ FP-64
☐ FP-64A