M37450S1SP/FP, M37450S2SP/FP M37450S4SP/FP

8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37450S1SP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or an 80-pin plastic molded QFP. In addition to its simple instruction sets, the ROM, RAM and I/O addresses are placed on the same memory map to enable easy programming. It is suited for office automation equipment and control devices. The low power consumption made possible by the use of a CMOS process makes it especially suitable for battery powered devices requiring low power consumption. It also has a unique feature that enables it to be used as a slave microcomputer.

M37450S1SP/FP, M37450S2SP/FP and M37450S4SP/FP have basically the same functions as M37450M2-XXXSP/FP except the RAM size and the fact that these three need external ROM area. The differences among M37450S1SP/FP, M37450S2SP/FP and M37450S4SP/FP are as shown below.

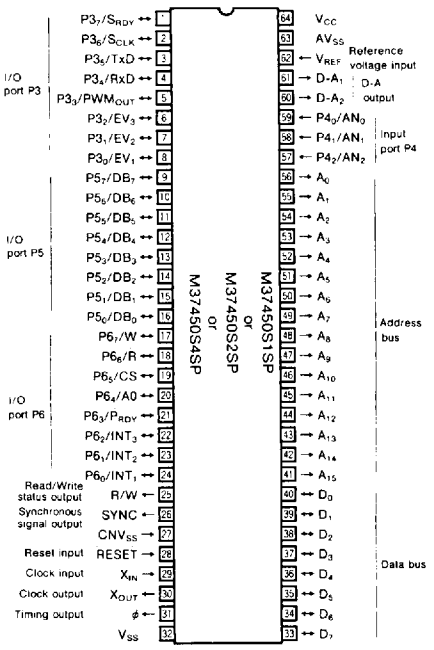
Type	RAM size
M37450S1SP/FP	128 bytes
M37450S2SP/FP	256 bytes
M37450S4SP/FP	448 bytes

Also M37450S1SP has the same function as M37450M2-XXXSP/FP in microprocessor mode and M37450S2SP/FP has the same function as M37450M4-XXXSP/FP in microprocessor mode.

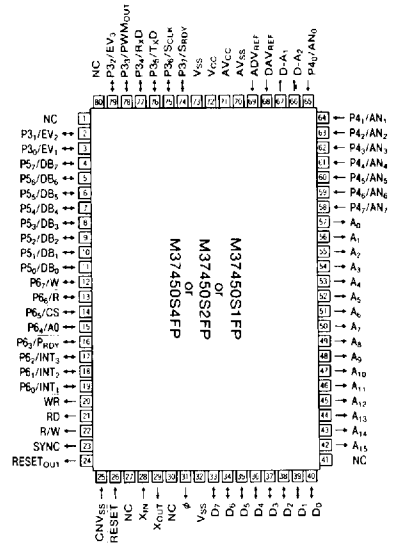
FEATURES

- Number of basic instructions 71
  69 MELPS 740 basic instructions + 2 multiply/divide instructions
- Memory size ROM ..... None
  RAM ..... 128 bytes (M37450S1SP/FP)
  256 bytes (M37450S2SP/FP)
  448 bytes (M37450S4SP/FP)
- Instruction execution time
  (minimum instructions at 10 MHz frequency) ..... 0.8 μs
- Single power supply ..... 5V $\pm$ 10%
- Power dissipation normal operation mode
  (at 10MHz frequency) 30mW
- Subroutine nesting ..... 64 levels max. (M37450S1SP/FP)
- Interrupt ..... 15 events
- Master CPU bus interface ..... 1 byte
- 16-bit timer 3
- 8-bit timer (Serial I/O use) 1
- Serial I/O (UART or clock synchronous) 1
- A-D converter (8bit resolution) ..... 3 channels (DIP)
  8 channels (QFP)
- D-A converter (8-bit resolution) ..... 2 channels
- PWM output (8-bit or 16-bit) 1
- Programmable I/O
  (Ports P0, P1, P2, P3, P5, P6) 48
- Input (Port P4) ..... 3 (DIP), 8 (QFP)
- Output (Port D-A_1, D-A_2) 2

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

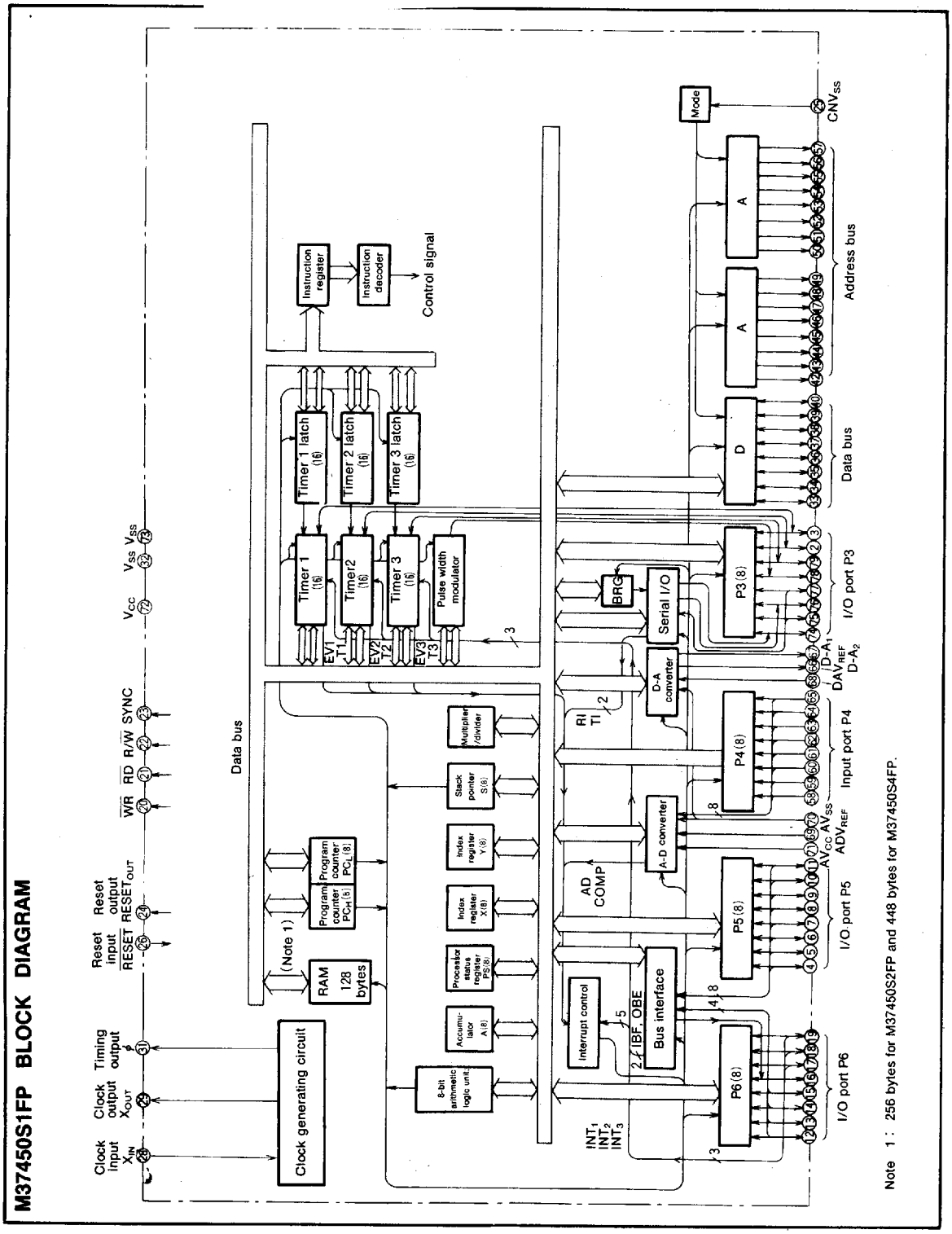


Outline 80P6 NC : No connection

APPICATION

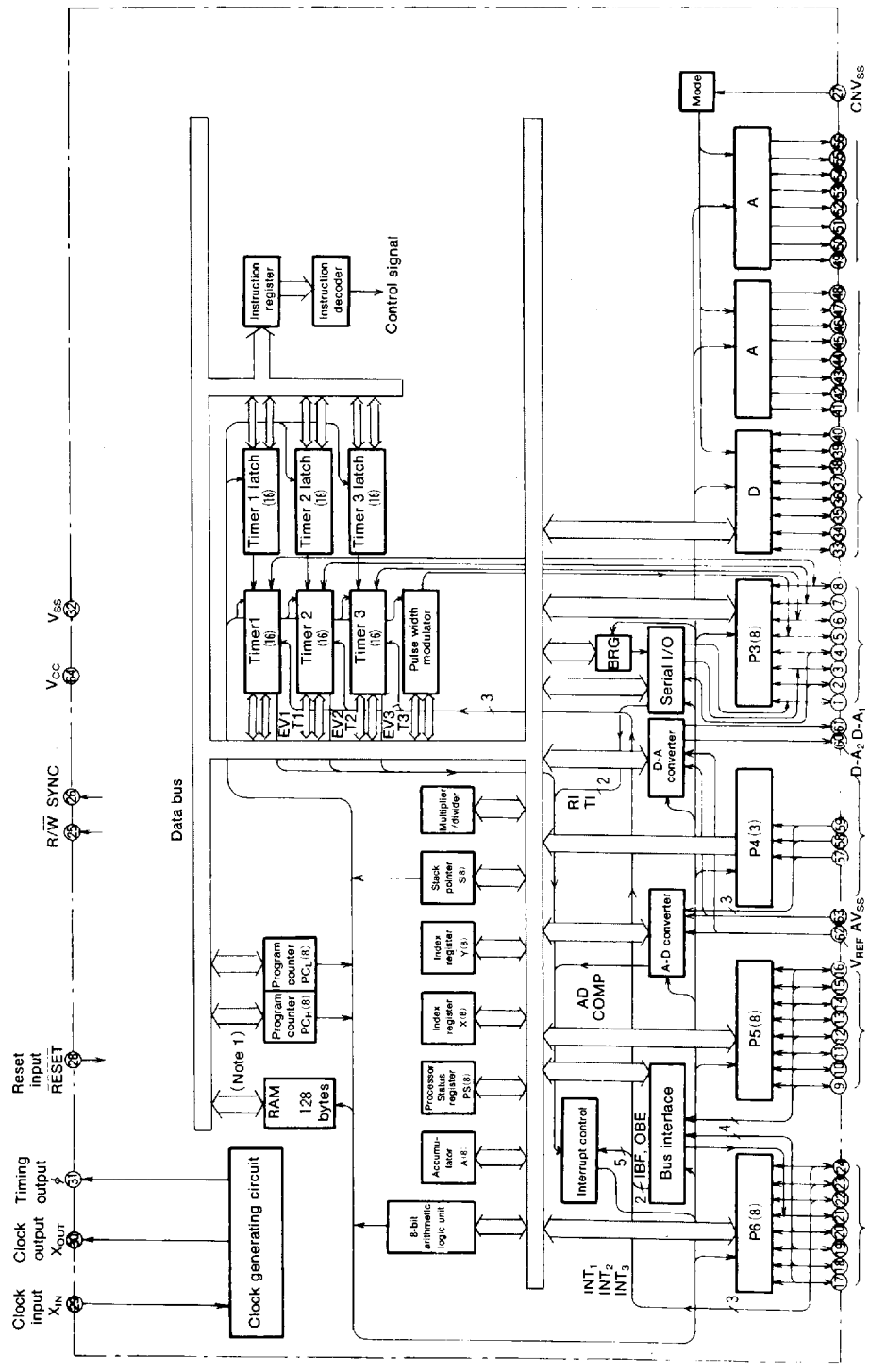
Slave controller for PPCs, facsimiles and page printers
HDD, optical disk, inverter and industrial motor controllers
Industrial robots and machines

M37450S1FP BLOCK DIAGRAM



Note 1 : 256 bytes for M37450S2FP and 448 bytes for M37450S4FP.

M37450S1SP BLOCK DIAGRAM



Note 1 : 256 bytes for M37450S2SP and 448 bytes for M37450S4SP.

FUNCTIONS OF M37450S1SP/FP, M37450S2SP/FP, M37450S4SP/FP

Parameter			Function
Number of basic instructions			71(69 MELPS 740 basic instructions+2)
Instruction execution time			0.8μs(minimum instructions, at 10MHz of frequency)
Clock frequency			10MHz(max.)
RAM size	M37450S1SP/FP		128 bytes
	M37450S2SP/FP		256 bytes
	M37450S4SP/FP		448 bytes
Input/Output port	P3, P5, P6	I/O	8-bit×3
	P4	Input	3-bit×1(8-bit×1 for 80-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer(serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels(8 channels for 80-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			64-levels(max. for M37450S1SP/FP)
			96-levels(max. for M37450S2SP/FP, M37450S4SP/FP)
Interrupt			6 external interrupts, 8 internal interrupts one software interrupt
Clock generating circuit			Built-in(ceramic or quarts crystal oscillator)
Supply voltage			5V±10%
Power dissipation			30mW(at 10MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA(max.)
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate
Package	M37450S1SP, M37450S2SP, M37450S4SP		64-pin shrink plastic molded DIP
	M37450S1FP, M37450S2FP, M37450S4FP		80-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}	Input	This is connected to V_{CC}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles(under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four.
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs.
R/$\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus. It is "H" during read and "L" during write
A_0~A_{15}	Address bus	Output	This is 16-bit address bus.
D_0~D_7	Data bus	I/O	This is 8-bit data bus.
$P3_0$~$P3_7$	Input/Output port P3	I/O	Port P3 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programed as input or output. The output structure is CMOS output. Serial I/O, PWM output, or even I/O function can be selected with a program.
$P4_0$~$P4_2$ ($P4_0$~$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter. The 64-pin model has three pins and the 80-pin model has eight pins. They may also be used as digital input pins.
$P5_0$~$P5_7$	Input/Output port P5	I/O	An 8-bit input/output port with the same function as P3. This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program.
$P6_0$~$P6_7$	Input/Output port P6	I/O	An 8-bit input/output port with the same function as P0. Pins $P6_3$~$P6_7$ change to a control bus for the master CPU when slave mode is selected with a program. Pins $P6_0$~$P6_2$ may be programmed as external interrupt input pins.
D-A_1, D-A_2	D-A output	Output	Analog signal from D-A converter is output.
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter. This pin is for 64-pin model only.
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter. This pin is for 80-pin model only.
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter. This pin is for 80-pin model only.
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter. Same voltage as V_{SS} is applied.
AV_{CC}	Analog power supply		Power supply input pin for A-D converter. This pin is for 80-pin model only. Same voltage as $V_{CC}$is applied. In the case of the 64-pin model AV_{CC} is connected to V_{CC} internally.
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus. This pin is for 80-pin model only.
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component. This pin is for 80-pin model only.
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset. It is used as a reset output signal for peripheral components. This pin is for 80-pin model only.

BASIC FUNCTION BLOCKS

The differences between M37450M2-XXXSP/FP and M37450S1SP/FP are noted below. Other functions are the same as M37450M2-XXXSP/FP in microprocessor mode.

MEMORY

A memory map for the M37450S1SP/FP is shown in Figure 1. Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $FFE0_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (This area must be located in ROM area).
Addresses 0000_{16}~$00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.
Addresses 0000_{16} to $007F_{16}$ are the RAM address area assigned to the M37450S1SP/FP and consist of 128 bytes.
Addresses 0000_{16} to $00BF_{16}$ and 0100_{16} to $013F_{16}$ are the RAM address area assigned to the M37450S2SP/FP and consist of 192 bytes and 64 bytes respectively.
Addresses 0000_{16} to $00BF_{16}$ and 0100_{16} to $01FF_{16}$ are the RAM address area assigned to the M37450S4SP/FP and consist of 192 bytes and 256 bytes respectively.
In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

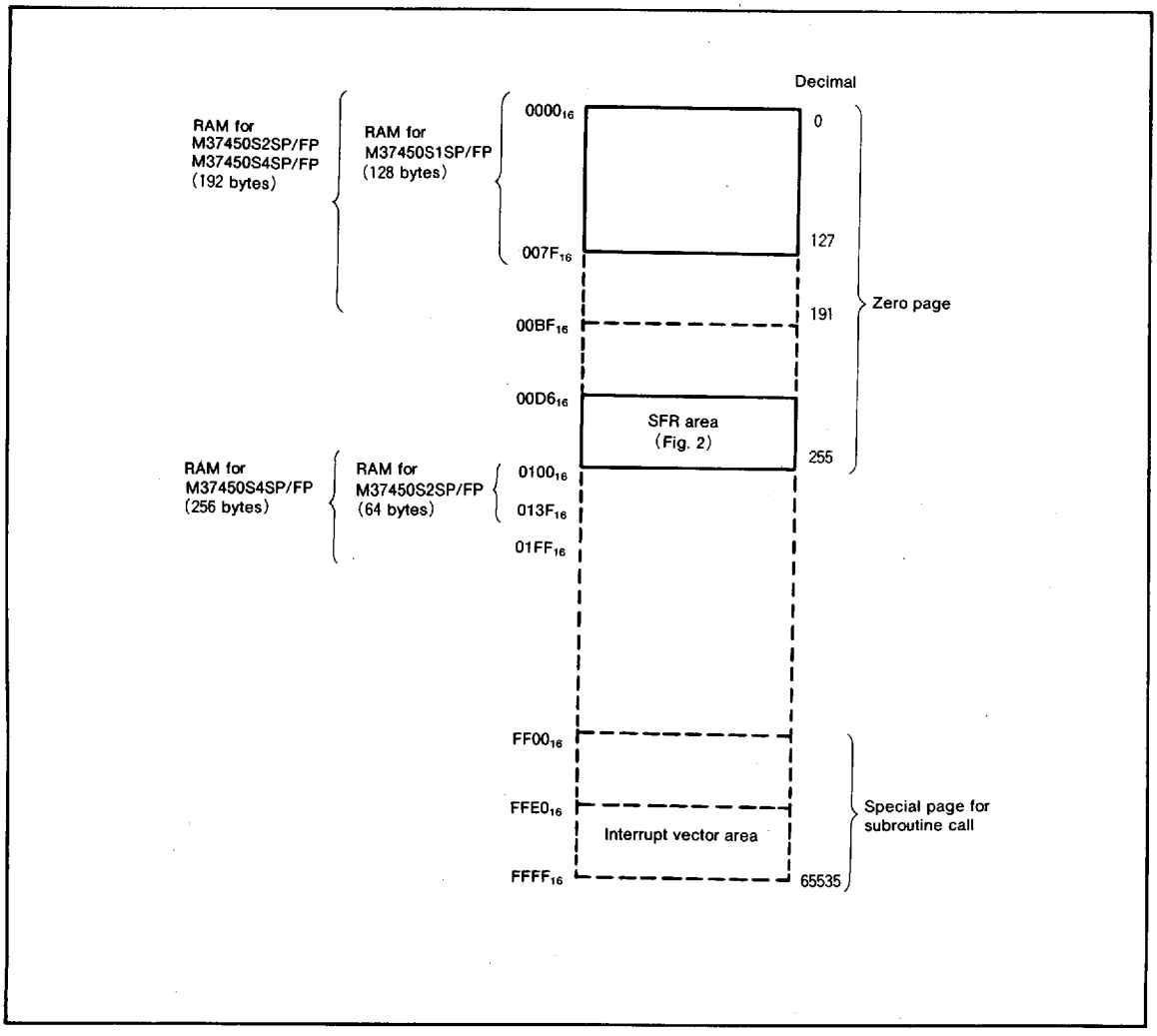


Fig. 1 Memory map

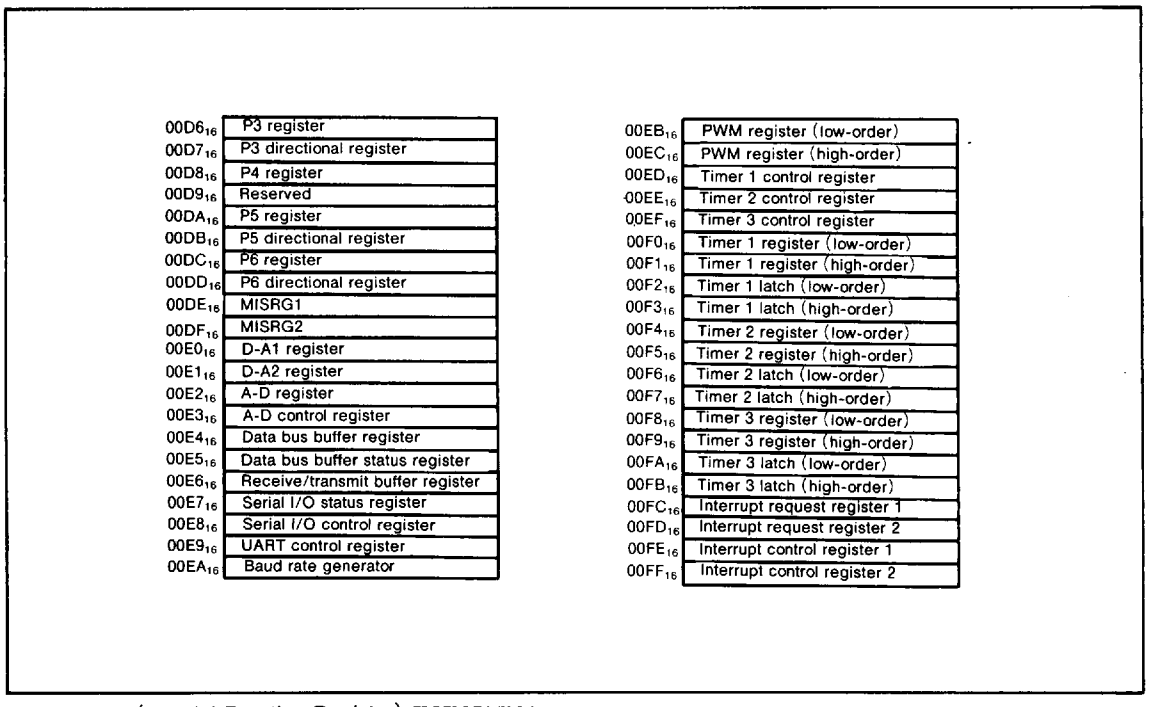


Fig. 2 SFR (Special Function Register) memory map

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state.	−0.3∼7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3∼7	V
V_I	Input voltage D_0∼D_7, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, ADV_{REF}, DAV_{REF}, V_{REF}, AV_{CC}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3∼13	V
V_O	Output voltage A_0∼A_{15}, D_0∼D_7, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, X_{OUT}, ϕ, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, $RESET_{OUT}$, SYNC		−0.3∼V_{CC}+0.3	V
Pd	Power dissipation	T_a = 25℃	1000 (Note 1)	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

Note 1 : 500mW for QFP type.

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=−10∼70℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" Input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 2)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage D_0∼D_7, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (except Note 2)	2.0		V_{CC}	V
V_{IL}	"L" Input voltage CNV_{SS} (Note 2)	0		0.2V_{CC}	V
V_{IL}	"L" Input voltage D_0∼D_7, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (except Note 2)	0		0.8	V
V_{IL}	"L" Input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" Input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current A_0∼A_{15}, D_0∼D_7, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current A_0∼A_{15}, D_0∼D_7, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 3)			5	mA
$I_{OH(peak)}$	"H" peak output current A_0∼A_{15}, D_0∼D_7, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current A_0∼A_{15}, D_0∼D_7, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 3)			−5	mA
$f(X_{IN})$	Clock oscillating frequency	1		10	MHz

Note 2 : Ports operate as INT_1∼INT_3($P6_0$∼$P6_2$), EV_1∼EV_3($P3_0$∼$P3_2$), R_xD($P3_4$) and S_{CLK}($P3_6$)

3 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms.

4 : The total of "L" output current $I_{OL(peak)}$ of port P3, P5, P6, R/$\overline{W}$ SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA.
The total of "H" output current $I_{OH(peak)}$ of port P3, P5, P6, R/$\overline{W}$ SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10~70℃, f(X_{IN}) = 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OH}=−2mA	V_{CC}−1			V
V_{OH}	"H" output voltage A_0~A_{15}, D_0~D_7, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OH}=−5mA	V_{CC}−1			V
V_{OL}	"L" output voltage A_0~A_{15}, D_0~D_7, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OL}=2mA			0.45	V
V_{OL}	"L" output voltage A_0~A_{15}, D_0~D_7, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OL}=5mA			1	V
$V_{T+}-V_{T-}$	Hysterisis INT_1~INT_3($P6_0$~$P6_2$), EV_1~EV_3($P3_0$~$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
$V_{T+}-V_{T-}$	Hysterisis $\overline{RESET}$				0.7	V
$V_{T+}-V_{T-}$	Hysterisis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current D_0~D_7, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{SS}	−5		5	μA
I_{IH}	"H" input current D_0~D_7, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	At system operation f(X_{IN})=10MHz		6	10	mA
		At stop mode (Note 5)		1	10	μA

Note 5 : The terminals $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ, D-A_1 and D-A_2 are all open. The other ports, which are in the input mode, are connected to V_{SS}. A-D converter is in the A-D completion state. The current through ADV_{REF} and DAV_{REF} is not included(Fig.6).

A-D CONVERTER CHARACTERISTICS

(V_{CC} = AV_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25℃, f(X_{IN})=10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=ADV_{REF}=5.12V		±1.5	±3	LSB
t_{CONV}	Conversion time				49	$t_C(\phi)$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	ADV_{REF}=5V	2	7.5	10	kΩ
$I_{IADVREF}$	Reference input current	ADV_{REF}=5V	0.5	0.7	2.5	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=DAV_{REF}=5.12V			1.0	%
t_{SU}	Setup time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
V_{DAVREF}	Reference input voltage		4		V_{CC}	V
I_{DAVREF}	Reference power input current		0	2.5	5	mA

TIMING REQUIREMENTS

Port/Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P3D-\phi)}$	Port P3 input setup time	Fig. 3	200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		200			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		200			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time		200			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time		40			ns
$t_C(X_{IN})$	External clock input cycle time		100		1000	ns
$t_W(X_{IN}L)$	External clock input "L" pulse width		30			ns
$t_W(X_{IN}H)$	External clock input "H" pulse width		30			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig. 3	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A_0 setup time		40			ns
$t_{su(A-W)}$	A_0 setup time		40			ns
$t_{h(R-A)}$	A_0 hold time		10			ns
$t_{h(W-A)}$	A_0 hold time		10			ns
$t_{W(R)}$	Read pulse width		160			ns
$t_{W(W)}$	Write pulse width		160			ns
$t_{su(D-W)}$	Date input setup time before write		100			ns
$t_{h(W-D)}$	Date input hold time after write		10			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig. 4	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A_0 setup time		40			ns
$t_{h(E-A)}$	A_0 hold time		10			ns
$t_{su(RW-E)}$	R/$\overline{W}$ setup time		40			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time		10			ns
$t_{W(EL)}$	Enable clock "L" pulse width		160			ns
$t_{W(EH)}$	Enable clock "H" pulse width		160			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		100			ns
$t_{h(E-D)}$	Data input hold time after write		10			ns

Local bus/Memory expansion mode, Microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(D-\phi)}$	Data input setup time	Fig. 5	100			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{su(D-RD)}$	Data input setup time		100			ns
$t_{h(RD-D)}$	Data input hold time		0			ns

SWITCHING CHARACTERISTICS

Port/Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig. 3			200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns
$t_{C(\phi)}$	Cycle time		400		4000	ns
$t_{W(\phi H)}$	ϕ clock pulse width ("H" level)		190			ns
$t_{W(\phi L)}$	ϕ clock pulse width ("L" level)		170			ns
$t_{r(\phi)}$	ϕ clock rising edge time				20	ns
$t_{f(\phi)}$	ϕ clock falling edge time				20	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{a(R-D)}$	Data output enable time after read	Fig. 4			120	ns
$t_{v(R-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(R-PR)}$	$\overline{P_{RDY}}$ output transmission time after read				150	ns
$t_{PLH(W-PR)}$	$\overline{P_{RDY}}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode) (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{a(E-D)}$	Data output enable time after read	Fig. 4			120	ns
$t_{v(E-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(E-PR)}$	$\overline{P_{RDY}}$ output transmission time after E clock				150	ns

Local bus/Memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-A)}$	address delay time after ϕ	Fig. 5			120	ns
$t_{v(\phi-A)}$	address effective time after ϕ		10			ns
$t_{v(RD-A)}$	address effective time after $\overline{RD}$		10			ns
$t_{v(WR-A)}$	address effective time after $\overline{WR}$		10			ns
$t_{d(\phi-D)}$	data output delay time after ϕ				140	ns
$t_{d(WR-D)}$	data output delay time after $\overline{WR}$				140	ns
$t_{v(\phi-D)}$	data output effective time after ϕ		20			ns
$t_{v(WR-D)}$	data output effective time after $\overline{WR}$		20			ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ delay time after ϕ				120	ns
$t_{d(\phi-SYNC)}$	SYNC delay time after ϕ				120	ns
$t_{W(RD)}$	$\overline{RD}$ pulse width		170			ns
$t_{W(WR)}$	$\overline{WR}$ pulse width		170			ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V
V_{IL} 0.45V
Output test level : V_{OH} 2.0V
V_{OL} 0.8V

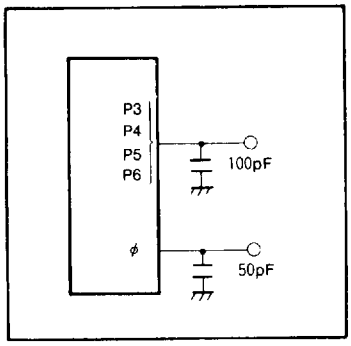


Fig. 3 Test circuit in single-chip mode

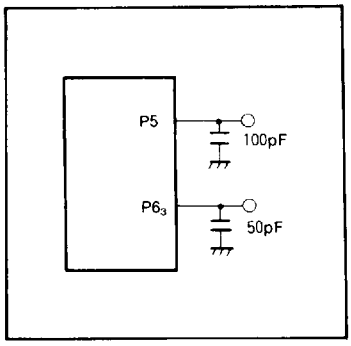


Fig. 4 Master CPU bus interface test circuit

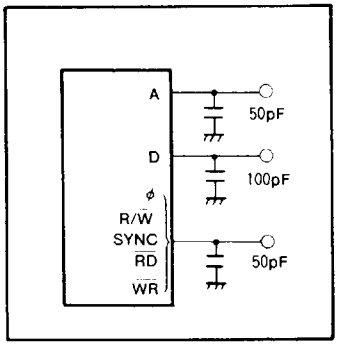


Fig. 5 Local bus test circuit

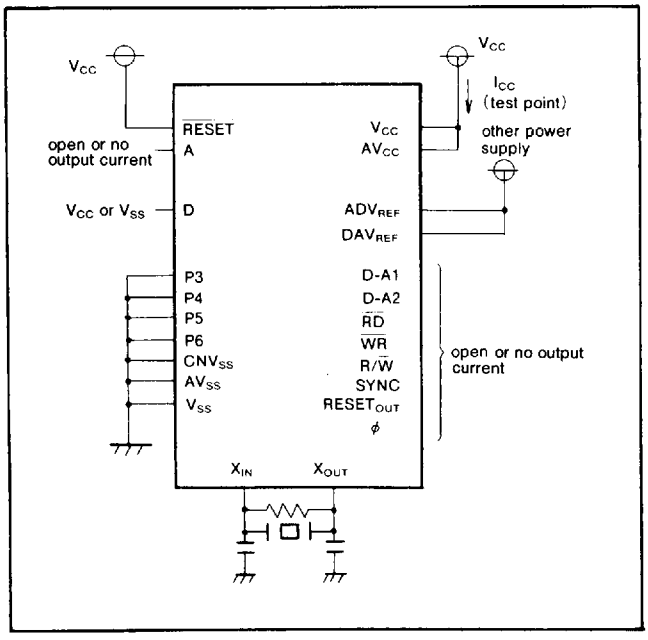
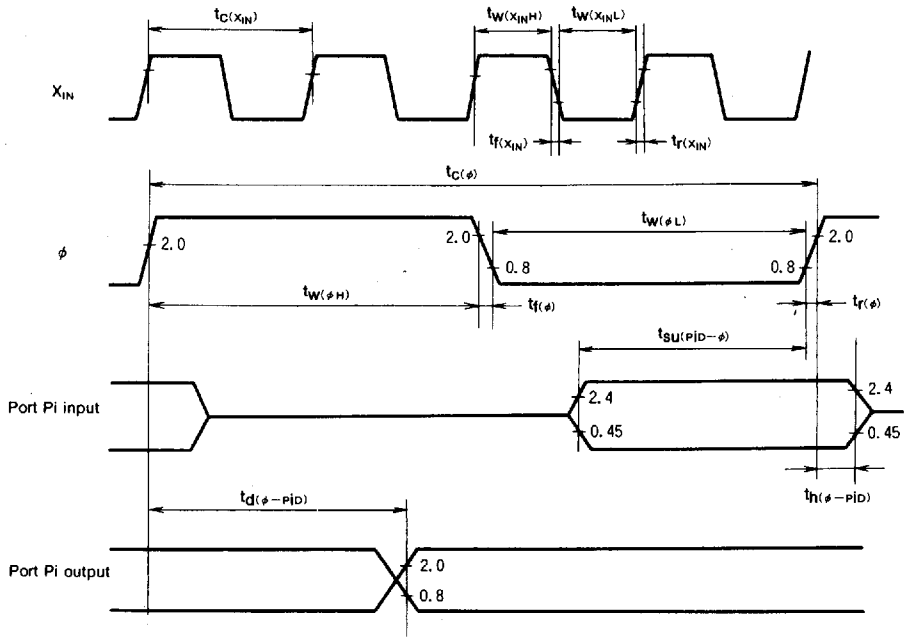


Fig. 6 I_{CC} (at stop mode) test condition

TIMING DIAGRAM

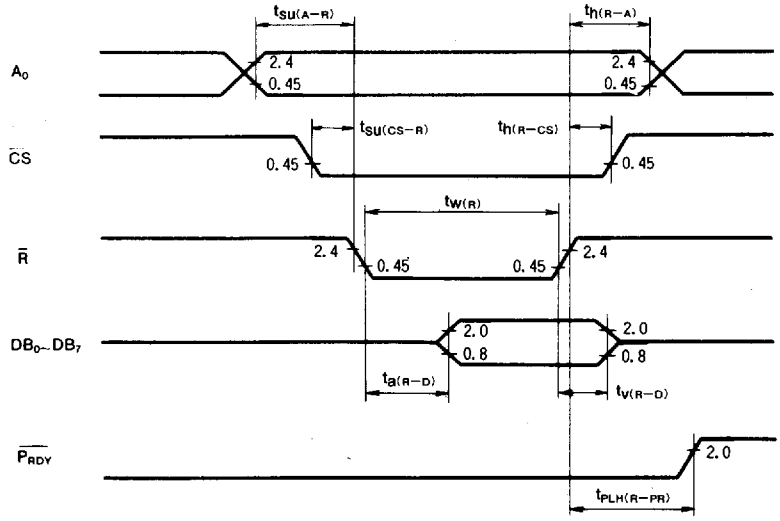
Port/single-chip mode timing diagram



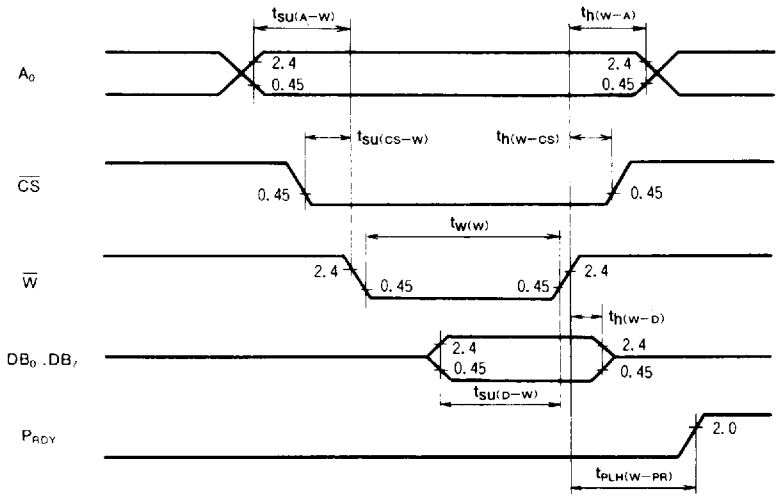
Note : V_{IH}=0.8V_{CC}, V_{IL}=0.16V_{CC} of X_{IN}

Master CPU bus interface/ $\overline{R}$ and W separation type timing diagram

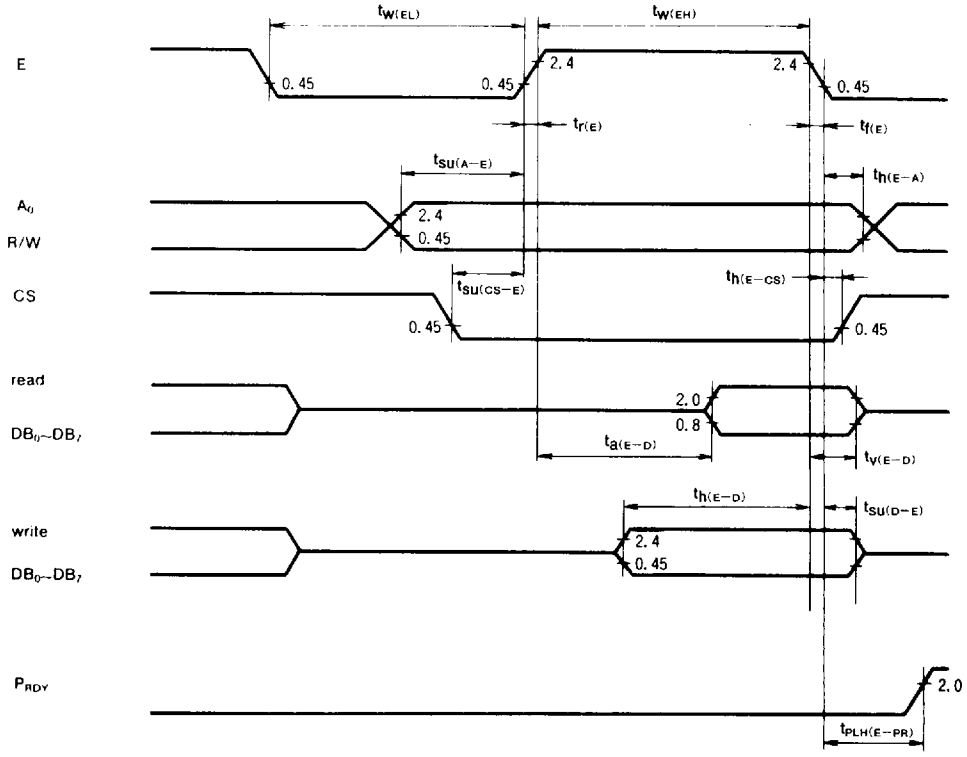
Read



Write



Master CPU interface/ R/W type timing diagram



Local bus timing diagram