

## Advance Information

MPC7410RXPEPNS/D  
Rev. 1, 10/2002

MPC7410 Part Number  
Specification for the  
MPC7410RXnnnPE Series



digital dna<sup>™</sup>

### *Motorola Part Numbers Affected:*

*MPC7410RX450PE  
MPC7410RX500PE  
MPC7410RX550PE*

This document describes part-number-specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC7410 Hardware Specifications* (order #: MPC7410EC/D).

Specifications provided in this document supersede those in the *MPC7410 Hardware Specifications*, for the part numbers listed in Table A only. Specifications not addressed herein are unchanged. Because this document is frequently updated, refer to <http://www.motorola.com/semiconductors> or to your Motorola sales office for the latest version.

Note that headings and table numbers in this document are not consecutively numbered. They are intended to correspond to the heading or table affected in the general hardware specification. Part numbers addressed in this document are listed in Table A. For more detailed ordering information see Table 17.

## Features

**Table A. Part Numbers Addressed by this Data Sheet**

Motorola Part Number	Operating Conditions			Significant Differences from Hardware Specification
	CPU Frequency	Vdd	T <sub>J</sub> (°C)	
MPC7410RX450PE	450 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 450Mhz frequency
MPC7410RX500PE	500 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 500Mhz frequency
MPC7410RX550PE	550 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 550Mhz frequency

## 1.2 Features

This section summarizes changes to the features of the MPC7410 described in the MPC7410 Hardware Specifications, of which there were none.

### 1.4.1 DC Electrical Characteristics

Table 3 provides the recommended operating conditions for the MPC7410 part numbers described herein.

**Table 3. Recommended Operating Conditions**

Characteristic		Symbol	Recommended Value	Unit
Core supply voltage		Vdd	2.0V ± 50mV	V
PLL supply voltage		AVdd	2.0V ± 50mV	V
L2 DLL supply voltage		L2AVdd	2.0V ± 50mV	V
Processor bus supply voltage	BVSEL = 1 or BVSEL = HRESET	OVdd	3.3V ± 165mV	
	BVSEL = $\overline{\text{HRESET}}$	OVdd	2.5V ± 125mV	V
	BVSEL = GND	OVdd	1.8V ± 90mV	V
L2 bus supply voltage	L2VSEL = 1 or L2VSEL = $\overline{\text{HRESET}}$	L2OVdd	2.5V ± 125mV	V
	L2VSEL = GND	L2OVdd	1.8V ± 90mV	V
Input voltage	Processor bus	V <sub>in</sub>	GND to OVdd	V
	L2 Bus	V <sub>in</sub>	GND to L2OVdd	V
	JTAG Signals	V <sub>in</sub>	GND to OVdd	V
Die-junction temperature		T <sub>j</sub>	0-65	°C

**Note:**

These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 6 provides the power consumption for the MPC7410 part at the frequencies described herein.

**Table 6. Power Consumption for MPC7410**

	Processor (CPU) Frequency	Processor (CPU) Frequency	Processor (CPU) Frequency	Unit	Notes
	450Mhz	500Mhz	550Mhz		
Full-On Mode					
Typical	5.9	6.5	7.1	W	1, 3
Maximum	13.2	14.7	16.2	W	1, 2
Doze Mode					
Maximum	4.5	5	5.5	W	1, 2
Nap Mode					
Maximum	2.13	2.25	2.37	W	1, 2
Sleep Mode					
Maximum	2.13	2.25	2.37	W	1, 2
Sleep Mode—PLL and DLL Disabled					
Typical	0.5	0.5	0.5	W	1, 3
Maximum	2.0	2.0	2.0	W	1, 2

**Notes:**

1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O Supply Power (OVdd and L2OVdd) or PLL/DLL supply power (AVdd and L2AVdd). OVdd and L2OVdd power is system dependent, but is typically <10% of Vdd power. Worst case power consumption for AVdd = 15 mw and L2AVdd = 15 mW.
2. Maximum power is measured at 65 °C and Vdd = 2.0V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, including AltiVec, maximally busy.
3. Typical power is an average value measured at 65 °C and Vdd = 2.0V in a system while running typical benchmarks.

### 1.4.2.1 Clock AC Specifications

Table 7 provides the additional clock AC timing specifications described in this document. Refer to the *MPC7410 Hardware Specification* for the remaining frequencies.

**Table 7. Clock AC Timing Specifications**

At recommended operating conditions (See Table 3)

Characteristic	Symbol	450 MHz		500 MHz		550 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Processor frequency	$f_{\text{core}}$	300	450	300	500	300	550	MHz	
VCO frequency	$f_{\text{VCO}}$	600	900	600	1000	600	1100	MHz	
SYSCLK frequency	$f_{\text{SYSCLK}}$	33	133	33	133	33	133	MHz	1
SYSCLK cycle time	$t_{\text{SYSCLK}}$	7.5	30	7.5	30	7.5	30	ns	
SYSCLK rise and fall time	$t_{\text{KR}}$	—	1.0	—	1.0	—	1.0	ns	2
	$t_{\text{KF}}$	—	0.5	—	0.5	—	0.5	ns	3
SYSCLK duty cycle measured at $OV_{\text{dd}}/2$	$t_{\text{KHKL}}/t_{\text{SYSCLK}}$	40	60	40	60	40	60	%	4
SYSCLK jitter		—	$\pm 150$	—	$\pm 150$	—	$\pm 150$	ps	5
Internal PLL relock time		—	100	—	100	—	100	$\mu\text{s}$	6

**Note:**

See general hardware specification.

## 1.4.2.2 Processor Bus AC Specifications

Table 8 provides the processor bus AC timing specifications for the MPC7410 part described in this document.

**Table 8. Processor Bus AC Timing Specifications**

At  $V_{dd}=AV_{dd}=2.0V\pm 50mV$ ;  $0 \leq T_j \leq 65^\circ C$ ,  $OV_{dd} = 2.5V\pm 0.125V$  and  $OV_{dd} = 1.8V\pm 0.090V$ , 60X bus at 133MHz

Parameter	Symbol	450, 500, 550 Mhz		Unit	Notes
		Min	Max		
Mode select input setup to $\overline{HRESET}$	$t_{MVRH}$	8	—	$t_{sysclk}$	2,3,4,5
$\overline{HRESET}$ to mode select input hold	$t_{MXRH}$	0	—	ns	2,3,5
Setup Times:				ns	10
Address/Transfer Attribute	$t_{AVKH}$	1.4	—		6
Transfer Start ( $\overline{TS}$ )	$t_{TSVKH}$	1.4	—		—
Data/Data Parity	$t_{DVKH}$	1.4	—		7
$\overline{ARTRY}/\overline{SHD0}/\overline{SHD1}$	$t_{ARVKH}$	1.4	—		—
All Other Inputs	$t_{IVKH}$	1.4	—		8
Input Hold Times:				ns	11
Address/Transfer Attribute	$t_{AXKH}$	0	—		6
Transfer Start ( $\overline{TS}$ )	$t_{TSXKH}$	0	—		—
Data/Data Parity	$t_{DXKH}$	0	—		7
$\overline{ARTRY}/\overline{SHD0}/\overline{SHD1}$	$t_{ARXKH}$	0	—		—
All Other Inputs	$t_{IXKH}$	0	—		8
Valid Times:				ns	12
Address/Transfer Attribute	$t_{KHAV}$	—	3.0		6
$\overline{TS}$ , $\overline{ABB}$ , $\overline{DBB}$	$t_{KHTSV}$	—	3.0		—
Data	$t_{KHdV}$	—	3.5		7
Data Parity	$t_{KHDPV}$	—	3.5		7
$\overline{ARTRY}/\overline{SHD0}/\overline{SHD1}$	$t_{KHARV}$	—	2.3		—
All Other Outputs	$t_{KHOV}$	—	3.0		9
Output Hold Times:				ns	13
Address/Transfer Attribute	$t_{KHAX}$	0.75	—		6
$\overline{TS}$ , $\overline{ABB}$ , $\overline{DBB}$	$t_{KHTSX}$	0.75	—		—
Data/Data Parity	$t_{KHdX}$	0.6	—		7
$\overline{ARTRY}/\overline{SHD0}/\overline{SHD1}$	$t_{KHARX}$	0.75	—		—
All Other Outputs	$t_{KHOX}$	0.75	—		9
SYSCLK to Output Enable	$t_{KHOE}$	0.5	—	ns	14
SYSCLK to Output High Impedance (all except $\overline{TS}$ , $\overline{ABB}/\overline{AMON}(0)$ , $\overline{ARTRY}/\overline{SHD}$ , $\overline{DBB}/\overline{DMON}(0)$ )	$t_{KHOZ}$	—	3.5	ns	15

## DC Electrical Characteristics

**Table 8. Processor Bus AC Timing Specifications (continued)**

At Vdd=AVdd=2.0V±50mV; 0 ≤ Tj ≤ 65°C, OVdd = 2.5V±0.125V and OVdd = 1.8V±0.090V, 60X bus at 133MHz

Parameter	Symbol	450, 500, 550 Mhz		Unit	Notes
		Min	Max		
SYSCLK to $\overline{TS}$ , $\overline{ABB/AMON}(0)$ , $\overline{DBB/DMON}(0)$ High Impedance after precharge	t <sub>KHABPZ</sub>	—	1.0	t <sub>sysclk</sub>	4,15,16,17
Maximum Delay to $\overline{ARTRY}/\overline{SHD0}/\overline{SHD1}$ Precharge	t <sub>KHARP</sub>	—	1	t <sub>sysclk</sub>	4,17
SYSCLK to $\overline{ARTRY}/\overline{SHD0}/\overline{SHD1}$ High Impedance After Precharge	t <sub>KHARPZ</sub>	—	2	t <sub>sysclk</sub>	4,17

Notes:

See General hardware specification.

### 1.4.2.3 L2 Clock AC Specifications

Table 9 provides the L2CLK Output AC Timing Specifications for the MPC7410 part described in this document.

**Table 9. L2CLK Output AC Timing Specifications**

At recommended operating conditions (See Table 3)

Parameter	Symbol	450 MHz		500 MHz		550 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
L2CLK frequency	f <sub>L2CLK</sub>	150	225	150	250	150	275	MHz	1
L2CLK cycle time	t <sub>L2CLK</sub>	4.4	6.67	4.0	6.67	3.64	6.67	ns	
L2CLK duty cycle	t <sub>CHCL</sub> /t <sub>L2CLK</sub>	50		50		50		%	2
Internal DLL-relock time		640	—	640	—	640	—	L2CLK	4
DLL capture window			±200		±200		±200	ns	5

**Note:**

See general hardware specification.

### 1.4.2.4 L2 Bus AC Specifications

Table 10 provides the L2 Bus Interface AC Timing Specifications for the frequencies described in this document.

**Table 10. L2 Bus Interface AC Timing Specifications**

At  $V_{dd}=AV_{dd}=L2AV_{dd}= 2.05V\pm 50mV$ ;  $0 \leq T_j \leq 65^\circ C$ ,  $L2OV_{dd} = 2.5V\pm 0.125V$  and  $L2OV_{dd} = 1.8V\pm 0.090V$

Parameter	Symbol	450, 500, 550 MHz		Unit	Notes
		Min	Max		
L2SYNC_IN rise and fall time	$t_{L2CR}$ & $t_{L2CF}$	—	1.0	ns	1
Setup Times: Data and parity	$t_{DVL2CH}$	1.250	—	ns	2
Input Hold Times: Data and parity	$t_{DXL2CH}$	—	0.0	ns	2
Valid Times: All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	$t_{L2CHOV}$	- - - -	2.25 2.50 2.75 3.25	ns	3,4
Output Hold Times All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	$t_{L2CHOX}$	0.5 0.9 1.3 1.7	- - - -	ns	3
L2SYNC_IN to high impedance: All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	$t_{L2CHOZ}$	- - - -	2.0 2.5 3.0 3.5	ns	

Notes: See General Hardware Specification

## 1.9 Document Revision History

Table 16 provides a revision history for this part number specification.

**Table 16. Document Revision History**

Document Revision	Substantive Change(s)
0	Initial release.
1	Minor formatting
	Section 1.10.1 - added Table 17 - Part Marking Nomenclature

## 1.10 Ordering Information

### 1.10.1 Part Numbers Addressed by this Specification

Table 17 provides the ordering information for the MPC7410 part described in this document.

**Table 17. Part Marking Nomenclature**

**MPC 7410    RX    xxx    X    X**

Product Code	Part Identifier	Package	Processor Frequency <sup>1</sup>	Application Modifier	Revision Level
MPC	7410	RX = CBGA	450 500 550	P: 2.0 V ± 50 mV 0 to 65 °C	E: 1.4; PVR = 800C 1104

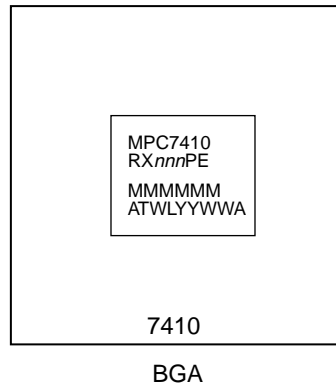
**Notes:**

1. Processor core frequencies supported by parts addressed by this specification only. Parts addressed by other specifications may support other maximum core frequencies.



### 1.10.3 Part Marking

Parts are marked as the example shown in Figure 26.



**Notes:**

*nnn* is the speed grade of the part

MMMMMM is the 6-digit mask number

ATWLYYWWA is the traceability code

CCCCC is the country of assembly (this space is left blank if parts are assembled in the United States)

**Figure 26. Motorola Part Marking for BGA Device**

**Ordering Information**



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