DS1500

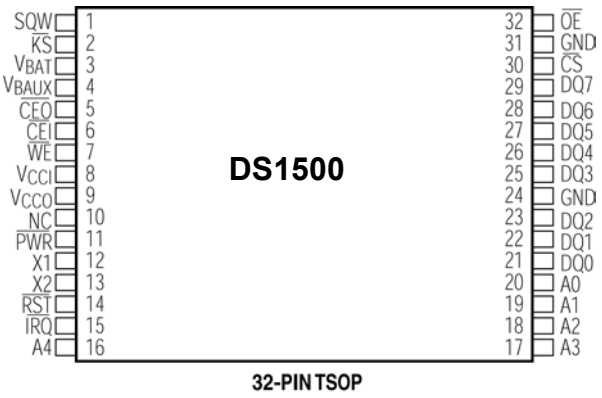
Y2KC Watchdog RTC with NV Control

www.maxim-ic.com

FEATURES

- BCD-coded century, year, month, date, day, hours, minutes, and seconds with automatic leap-year compensation valid up to the year 2100
- Programmable watchdog timer and real-time clock (RTC) alarm
- Century register; Y2K-compliant RTC
- Automatic battery backup and write protection to external SRAM
- +5V operation
- Precision power-on reset
- Power-control circuitry supports system power-on from date/day/time alarm or key closure
- 256 bytes user NV RAM
- Auxiliary battery input
- Accuracy is better than ±1 minute/month at +25°C
- Day of week/date alarm register
- Battery voltage-level indicator flags
- Optional industrial temperature range: -40°C to +85°C

PIN ASSIGNMENT (Top View)



32-PIN TSOP

Package dimension information can be found at:
http://www.maxim-ic.com/TechSupport/DallasPackInfo.htm

ORDERING INFORMATION

DS1500XXX

blank	Commercial Temp. Range
N	Industrial Temp. Range
E	32-Pin TSOP
Y	5V Operation

Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: http://www.maxim-ic.com/errata.

PIN DESCRIPTION

V_{CCI}	- Supply Voltage
A0 to A4	- Address Inputs
DQ0 to DQ7	- Data I/O
$\overline{CS}$	- RTC Chip-Select Input
$\overline{OE}$	- RTC Output-Enable Input
$\overline{WE}$	- RTC Write-Enable Input
$\overline{IRQ}$	- Interrupt Output (Open Drain)
$\overline{PWR}$	- Power-On Output (Open Drain)
$\overline{RST}$	- Reset Output (Open Drain)
$\overline{KS}$	- Kickstart Input
SQW	- Square-Wave Output
V_{BAT}	- Backup-Battery Supply
V_{BAUX}	- Auxiliary-Battery Supply
$\overline{CEI}$	- RAM Chip-Enable Input
$\overline{CEO}$	- RAM Chip-Enable Output
V_{CCO}	- RAM Power-Supply Output
X1, X2	- 32.768kHz Crystal Pins
GND	- Ground

DESCRIPTION

The DS1500 is a full-function, year 2000-compliant real-time clock/calendar (RTC) with an alarm, watchdog timer, power-on reset, battery monitors, 256 bytes of on-board NV SRAM, NV control for backing up an external SRAM, and a 32.768kHz output. User access to all registers within the DS1500 is accomplished with a bytewide interface as shown in Figure 1. The RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in 24-hour binary-coded decimal (BCD) format. Corrections for day of month and leap year are made automatically.

The RTC registers are double-buffered into an internal and external set. The user has direct access to the external set. Clock/calendar updates to the external set of registers can be disabled and enabled to allow the user to access static data. When the crystal oscillator is turned on, the internal set of registers are continuously updated; this occurs regardless of external register settings to guarantee that accurate RTC information is always maintained.

The DS1500 contains its own power-fail circuitry that automatically deselects the device when the V_{CCI} supply falls below a power-fail trip point. This feature provides a high degree of data security during unpredictable system operation caused by low V_{CCI} levels. An external SRAM can be made nonvolatile by using the V_{CCO} and $\overline{CEO}$ pins. Nonvolatile control of the external SRAM is analogous to that of the RTC registers. When V_{CCI} slews down during a power fail, $\overline{CEO}$ is driven to an inactive level regardless of $\overline{CEI}$. This write protection occurs when V_{CCI} is less than the power-fail trip point.

The DS1500 has interrupt ($\overline{IRQ}$), power control ($\overline{PWR}$), and reset ($\overline{RST}$) outputs that can be used to control CPU activity. The $\overline{IRQ}$ interrupt or $\overline{RST}$ outputs can be invoked as the result of a time-of-day alarm, CPU watchdog alarm, or a kickstart signal. The DS1500 power-control circuitry allows the system to be powered on by an external stimulus, such as a keyboard or by a time and date (wake-up) alarm. The $\overline{PWR}$ output pin can be triggered by one or either of these events, and can be used to turn on an external power supply. The $\overline{PWR}$ pin is under software control, so that when a task is complete, the system power can then be shut down. The DS1500 power-on reset can be used to detect a system power-down or failure and hold the CPU in a safe reset state until normal power returns and stabilizes; the $\overline{RST}$ output is used for this function.

The DS1500 is a clock/calendar chip with the features described above. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power.

Figure 1. **BLOCK DIAGRAM**

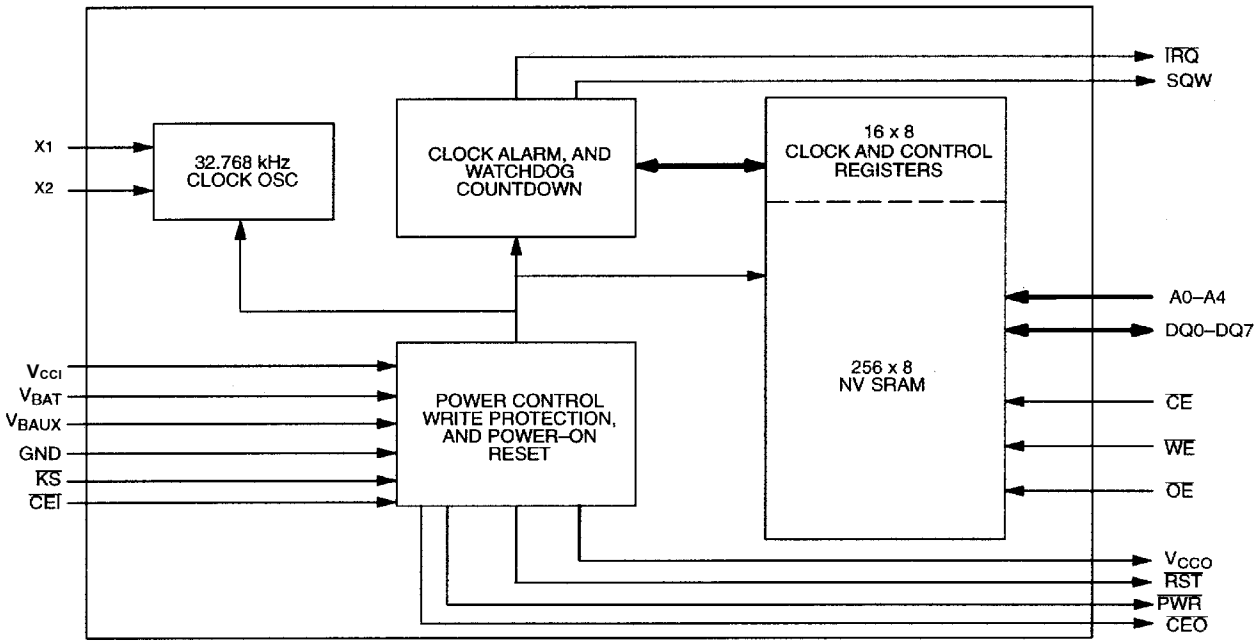


Table 1. **RTC OPERATING MODES**

V_{CCI}	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	DQ0–DQ7	A0–A4	MODE	POWER
$V_{CCI} > V_{PF}$	V_{IH}	X	X	High-Z	X	Deselect	Standby
	V_{IL}	X	V_{IL}	D_{IN}	A_{IN}	Write	Active
	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}	Read	Active
	V_{IL}	V_{IH}	V_{IH}	High-Z	A_{IN}	Read	Active
$V_{SO} < V_{CCI} < V_{PF}$	X	X	X	High-Z	X	Deselect	CMOS Standby
$V_{CCI} < V_{SO} < V_{PF}$	X	X	X	High-Z	X	Data Retention	Battery Current

RTC DATA READ MODE

The DS1500 is in the read mode whenever $\overline{CS}$ (chip select) is low and $\overline{WE}$ (write enable) is high. The device architecture allows ripple-through access to any valid address location. Valid data is available at the DQ pins within t_{AA} (address access) after the last address input is stable, provided that $\overline{CS}$ and $\overline{OE}$ access times are satisfied. If $\overline{CS}$ or $\overline{OE}$ access times are not met, valid data is available at the latter of chip-enable access (t_{CSA}) or at output-enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CS}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CS}$ and $\overline{OE}$ remain valid, output data remains valid for output-data hold time (t_{OH}) but then goes indeterminate until the next address access (Table 1).

RTC DATA WRITE MODE

The DS1500 is in the write mode whenever $\overline{WE}$ and $\overline{CS}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$ or $\overline{CS}$. The addresses must be held valid throughout the cycle. $\overline{CS}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of a subsequent read or write cycle. Data in must be valid t_{DS} prior to the end of the write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal is high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to a high-to-low transition on $\overline{WE}$, the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ then disables the outputs t_{WEZ} after $\overline{WE}$ goes active (Table 1).

DATA RETENTION MODE

The 5V device is fully accessible and data can be written and read only when V_{CCI} is greater than V_{PF}. However, when V_{CCI} falls below the power-fail point V_{PF} (point at which write protection occurs), the internal clock registers and SRAM are blocked from any access. While in the data retention mode, all inputs are “don’t cares” and outputs go to a high-Z state, with the exception of V_{CCO}, $\overline{CEO}$, and the possible exception of $\overline{KS}$, $\overline{PWR}$, SQW, and $\overline{RST}$. When V_{CCI} falls below the greater of V_{BAT} or V_{BAUX}, device power is switched from the V_{CCI} pin to the greater of V_{BAT} or V_{BAUX}. RTC operation and external SRAM data are maintained from the battery until V_{CCI} is returned to nominal levels (Table 1).

All control, data, and address signals must be no more than 0.3V above V_{CCI}.

AUXILIARY BATTERY

The V_{BAUX} input is provided to supply power from an auxiliary battery for the DS1500 kickstart and square-wave output features in the absence of V_{CCI}. This power source must be available to use these auxiliary features when no V_{CCI} is applied to the device.

This auxiliary battery can be used as the primary backup power source for maintaining the clock/calendar and external SRAM. This occurs if the V_{BAT} pin is at a lower voltage than V_{BAUX}. If the DS1500 is to be backed-up using a single battery with the auxiliary features enabled, then V_{BAUX} should be used and connected to V_{BAT}. If V_{BAUX} is not to be used, it should be grounded.

POWER ON RESET

A temperature-compensated comparator circuit monitors the level of V_{CCI}. When V_{CCI} falls to the power-fail trip point, the $\overline{RST}$ signal (open drain) is pulled low. When V_{CCI} returns to nominal levels, the $\overline{RST}$ signal continues to be pulled low for a period of 40ms to 200ms. The power-on reset function is independent of the RTC oscillator and therefore operational whether or not the oscillator is enabled.

CLOCK OSCILLATOR CONTROL

The clock oscillator can be stopped at any time. To increase the shelf life of a backup lithium-battery source, the oscillator can be turned off to minimize current drain from the battery. The $\overline{EOSC}$ bit is used to control the state of the oscillator, and must be set to a 0 for the oscillator to function.

READING THE CLOCK

When reading the clock and calendar data, it is recommended to halt updates to the external set of double-buffered RTC registers. This puts the external registers into a static state allowing data to be read without register values changing during the read process. Normal updates to the internal registers continue while in this state. External updates are halted when a 0 is written into the read (TE) bit of control register B (0Fh). As long as a 0 remains in the control register B (TE) bit, updating is halted. After a halt is issued, the registers reflect the RTC count (day, date, and time) that was current at the moment the halt command was issued. Normal updates to the external set of registers resume within 1 second after the (TE) bit is set to a 1.

SETTING THE CLOCK

It is also recommended to halt updates to the external set of double-buffered RTC registers when writing to the clock. The TE bit should be used as described above before loading the RTC registers with the desired RTC count (day, date, and time) in 24-hour BCD format. Setting the TE bit to a 1 transfers the values written to the internal RTC registers and allows normal operation to resume.

CLOCK ACCURACY

A standard 32.768kHz quartz crystal should be directly connected to the DS1500 X1 and X2 oscillator pins. The crystal selected for use should have a specified load capacitance (C_L) of either 6pF or 12.5pF, and the crystal select (CS) bit set accordingly. For more information about crystal selection and crystal layout considerations, please consult Application Note 58, “Crystal Considerations with Dallas Real-Time

Clocks." The DS1500 can also be driven by an external 32.768kHz oscillator. In order to achieve low-power operation when using an external oscillator, it may be necessary to connect the X1 pin to the external oscillator signal through a series connection consisting of a resistor and a capacitor. A typical configuration consists of a 1.0Meg resistor in series with a 100pF ceramic capacitor. When using an external oscillator the X2 pin must be left open. Accuracy of DS1510 is better than ±1 min/month at +25°C.

USING THE CLOCK ALARM

The alarm settings and control reside within registers 08h to 0Bh (Table 3). The TIE bit and alarm mask bits AM1 to AM4 must be set as described below for the $\overline{IRQ}$ or $\overline{PWR}$ outputs to be activated for a matched alarm condition.

The alarm can be programmed to activate on a specific day of the month, day of the week, or repeat every day, hour, minute, or second. It can also be programmed to go off while the DS1500 is in the battery-backed state of operation to serve as a system wake-up. Alarm mask bits AM1 to AM4 control the alarm mode. Table 2 shows the possible settings. Configurations not listed in the table default to the once-per-second mode to notify the user of an incorrect alarm setting. When the RTC register values match alarm register settings, the time-of-day/date alarm flag TDF bit is set to a 1. Once the TDF flag is set, the TIE bit enables the alarm to activate the $\overline{IRQ}$ pin. The TPE bit enables the alarm flag to activate the $\overline{PWR}$ pin. The alarm functions on V_{CC}, V_{BATT}, and V_{BAUX}.

Table 2. **ALARM MASK BITS**

DY/DT	AM4	AM3	AM2	AM1	ALARM RATE
X	1	1	1	1	Once per second
X	1	1	1	0	When seconds match
X	1	1	0	0	When minutes and seconds match
X	1	0	0	0	When hours, minutes, and seconds match
0	0	0	0	0	When date, hours, minutes, and seconds match
1	0	0	0	0	When day, hours, minutes, and seconds match

USING THE WATCHDOG TIMER

The watchdog timer can be used to restart an out-of-control processor. The watchdog timer is user programmable in 10ms intervals ranging from 0.01 seconds to 99.99 seconds. The user programs the watchdog timer by setting the desired amount of time-out into the two BCD watchdog registers (Address 0Ch and 0Dh). For example, writing 60h in the watchdog register 0Ch and 00h to watchdog register 0Dh sets the watchdog time-out to 600ms. If the processor does not access the timer with a write within the specified period, both the watchdog flag (WDF) and the interrupt request flag (IRQF) are set. If the watchdog enable bit (WDE) is enabled, then either $\overline{IRQ}$ or $\overline{RST}$ go active depending on the state of the watchdog steering bit (WDS). The watchdog is reloaded and restarted whenever the watchdog times out. The WDF bit is set to a 1 regardless of the state of WDE to serve as an indication to the processor that a watchdog time out has occurred.

The watchdog timer is reloaded when the processor performs a write of the watchdog registers. The time-out period then starts over. The watchdog timer is disabled by writing a value of 00h to both watchdog registers. The watchdog function is automatically disabled upon power-up.

The following summarizes the configurations in which the watchdog can be used:

1) **WDE = 0 and WDS = 0:** WDF is set.
2) **WDE = 0 and WDS = 1:** WDF is set.
3) **WDE = 1 and WDS = 0:** WDF and IRQF are set, and the $\overline{\text{IRQ}}$ pin is pulled low.
4) **WDE = 1 and WDS = 1:** WDF is set, the $\overline{\text{RST}}$ pin is pulled low for a duration of 40ms to 200ms, and WDE is reset to 0.

CLEARING IRQ AND FLAGS

The time-of-day/date alarm flag (TDF), watchdog flag (WDF), and interrupt request flag (IRQF) are cleared by reading the flag register (0EH) as shown in Figures 2a, 2b, and 2c. The address must be stable for a minimum of 15ns (t_{IRQZ}). After the t_{IRQZ} requirement is met, either a change in address (Figure 2a), a rising edge of $\overline{OE}$ (Figure 2b), or a rising edge of $\overline{CS}$ causes the flags to be cleared. The $\overline{IRQ}$ pin goes inactive after the IRQF flag is cleared.

Figure 2a. **IRQ AND FLAG WAVEFORMS (ADDRESS RELATED)**

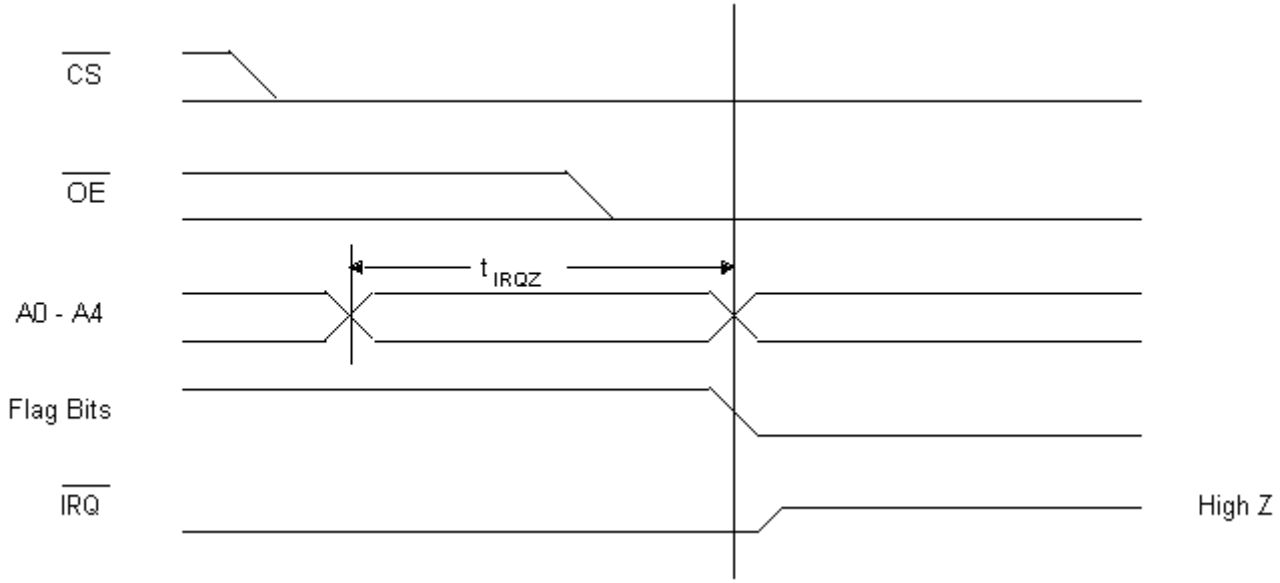


Figure 2b. **IRQ AND FLAG WAVEFORMS ($\overline{OE}$ RELATED)**

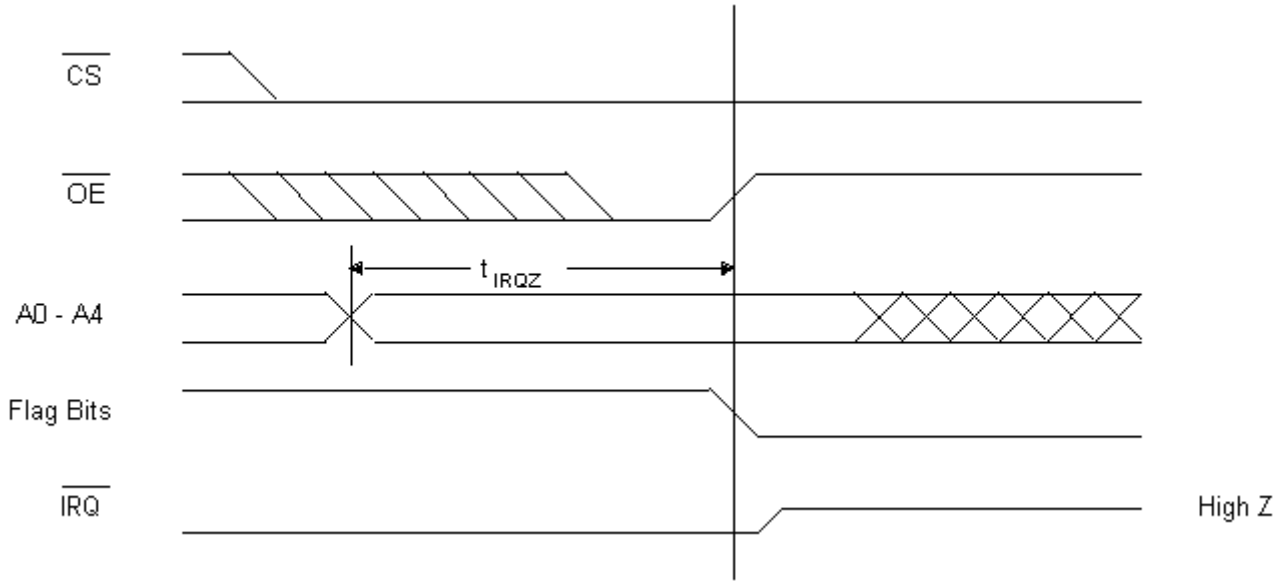
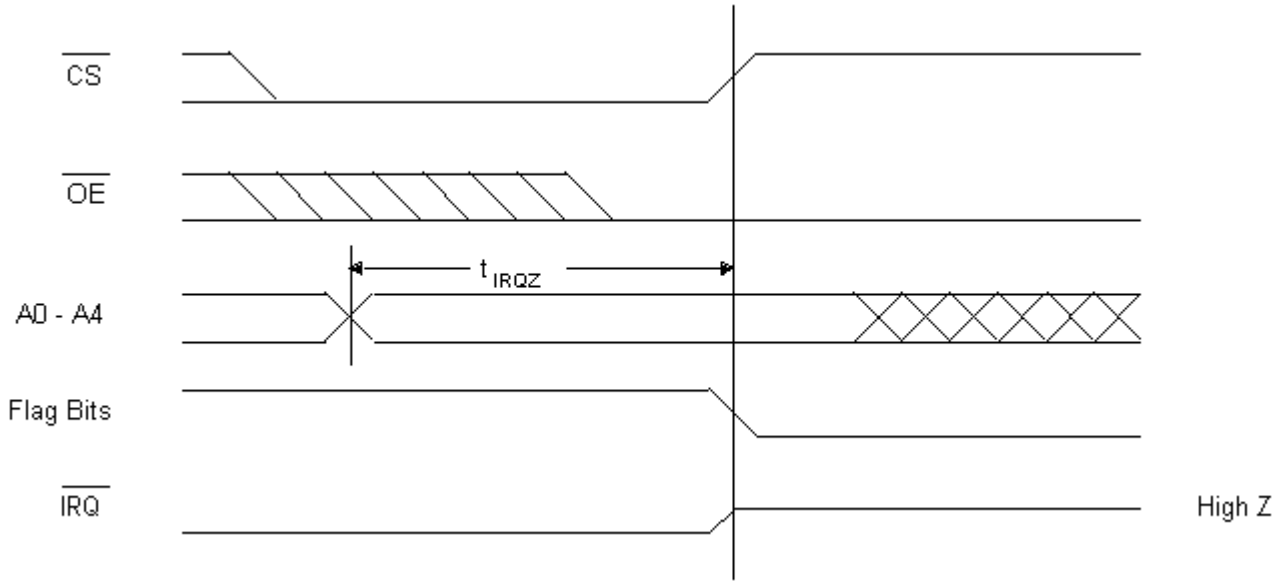


Figure 2c. **IRQ AND FLAG WAVEFORMS ($\overline{CS}$ RELATED)**



WAKE-UP/KICKSTART

The DS1500 incorporates a wake-up feature, which powers on at a predetermined date by activating the $\overline{PWR}$ output pin. In addition, the kickstart feature allows the system to be powered up in response to a low-going transition on the $\overline{KS}$ pin, without operating voltage applied to the V_{CCI} pin. As a result, system power can be applied upon such events as key closure, or a modem ring-detects signal. In order to use either the wake-up or the kickstart features, the DS1500 must have an auxiliary battery connected to the V_{BAUX} pin and the oscillator must be running.

The wake-up feature is controlled through the time-of-day/date power-enable bit (TPE). Setting TPE to 1 enables the wake-up feature. Writing TPE to 0 disables the wake-up feature. Similarly, the kickstart feature is controlled through the kickstart interrupt enable bit (KIE).

If the wake-up feature is enabled, while the system is powered down (no V_{CCI} voltage), the clock/calendar monitors the current day or date for a match condition with day/date alarm register (0Bh). In conjunction with the day/date alarm register, the hours, minutes, and seconds alarm bytes in the clock-calendar register map (02h, 01h, and 00h) are also monitored. As a result, a wake-up occurs at the day or date and time specified by the day/date, hours, minutes, and seconds alarm-register values. This additional alarm occurs regardless of the programming of the TIE bit. When the match condition occurs, the $\overline{PWR}$ pin is automatically driven low. This output can be used to turn on the main system power supply, which provides V_{CCI} voltage to the DS1500 as well as the other major components in the system. Also, at this time, the time-of-day/date alarm flag is set, indicating that a wake-up condition has occurred.

If the kickstart feature is enabled with the KSE bit and V_{BAUX} is present, while V_{CCI} is low, the $\overline{KS}$ input pin is monitored for a low-going transition of minimum pulse width t_{KSPW}. When such a transition is detected, the $\overline{PWR}$ line is pulled low, as it is for a wake-up condition. Also at this time, the kickstart flag

(KSF) is set, indicating that a kickstart condition has occurred. The $\overline{KS}$ input pin is always enabled and must not be allowed to float.

The timing associated with both the wake-up and kickstarting sequence is illustrated in Figure 7. The timing associated with these functions is divided into five intervals, labeled 1 to 5 on the diagram.

The occurrence of either a kickstart or wake-up condition causes the $\overline{PWR}$ pin to be driven low, as described above. During Interval 1, if the supply voltage on the V_{CCI} pin rises above the greater of V_{BAT} or V_{PF} before the power-on timeout period (t_{POTO}) expires, then $\overline{PWR}$ remains at the active-low level. If V_{CCI} does not rise above the greater of V_{BAT} or V_{PF} in this time, then the $\overline{PWR}$ output pin is turned off and returns to its high-impedance level. In this event, the $\overline{IRQ}$ pin also remains tristated. The interrupt flag bit (either TDF or KSF) associated with the attempted power-on sequence remains set until cleared by software during a subsequent system power-on.

If V_{CCI} is applied within the time-out period, then the system power-on sequence continues as shown in Intervals 2 to 5 in the timing diagram. During Interval 2, $\overline{PWR}$ remains active and $\overline{IRQ}$ is driven to its active-low level, indicating that either TDF or KSF was set in initiating the power-on. In the diagram, $\overline{KS}$ is assumed to be pulled up to the V_{BAUX} supply. Also at this time, the PAB bit is automatically cleared to 0 in response to a successful power-on. The $\overline{PWR}$ line remains active as long as the PAB remains cleared to 0.

At the beginning of Interval 3, the system processor has begun code execution and clears the interrupt condition of TDF and/or KSF by writing 0's to both of these control bits. As long as no other interrupt within the DS1500 is pending, the $\overline{IRQ}$ line is taken inactive once these bits are reset, and execution of the application software can proceed. During this time, both the wake-up and kickstart functions can be used to generate status and interrupts. TDF is set in response to a day/date, hours, minutes, and seconds match condition. KSF is set in response to a low-going transition on $\overline{KS}$. If the associated interrupt-enable bit is set (TDE and/or KIE), then the $\overline{IRQ}$ line is driven low in response to enabled event. In addition, the other possible interrupt sources within the DS1500 can cause $\overline{IRQ}$ to be driven low. While system power is applied, the on-chip logic always attempts to drive the $\overline{PWR}$ pin active in response to the enabled kickstart or wake-up condition. This is true even if $\overline{PWR}$ was previously inactive as the result of power being applied by some means other than wake-up or kickstart.

The system can be powered down under software control by setting the PAB bit to a 1. This causes the open-drain $\overline{PWR}$ pin to be placed in a high-impedance state, as shown at the beginning of Interval 4 in the timing diagram. As V_{CCI} voltage decays, the $\overline{IRQ}$ output pin is placed in a high-impedance state when V_{CCI} goes below V_{PF}. If the system is to be again powered on in response to a wake-up or kickstart, then both the TDF and KSF flags should be cleared, and TPE and/or KIE should be enabled prior to setting the PAB bit.

During Interval 5, the system is fully powered down. Battery backup of the clock calendar and NV RAM is in effect and $\overline{IRQ}$ is tristated, and monitoring of wake-up and kickstart takes place. If PRS =1, $\overline{PWR}$ stays active; otherwise, if PRS = 0, $\overline{PWR}$ is tristated.

SQUARE-WAVE OUTPUT

The square-wave output is enabled and disabled through the $\overline{E32K}$ bit. If the square wave is enabled ($\overline{E32K}$ = 0) and the oscillator is running, then a 32.768kHz square wave is output on the SQW pin. If the battery-backup 32kHz-enable bit (BB32) is enabled, and voltage is applied to V_{BAUX}, then the 32.768kHz square wave is output on the SQW pin in the absence of V_{CCI}.

BATTERY MONITOR

The DS1500 constantly monitors the battery voltage of the backup-battery sources (V_{BAT} and V_{BAUX}). The battery low flags VRT1 and VRT2 are set to a 1 if the battery voltage on V_{BAT} and V_{BAUX} are less than 2.5V (typical); otherwise, VRT1 and VRT2 are a 0. VRT1 monitors V_{BAT} and VRT2 monitors V_{BAUX}.

POWER-UP DEFAULT STATES

These bits are set upon power-up: $\overline{EOSC}$ = 0, $\overline{E32K}$ = 0, TIE = 0, KIE = 0, WDE = 0, and WDS = 0.

256 x 8 EXTENDED RAM

The DS1500 provides 256 x 8 of on-chip SRAM, which is controlled as nonvolatile storage sustained from a lithium battery. On power-up, the RAM is taken out of write-protect status by an internal signal.

Access to the SRAM is controlled by two on-chip latch registers. One register is used to hold the SRAM address; the other is used to hold read/write data. The SRAM address space is from 00h to FFh. The 8-bit address of the RAM location to be accessed must be loaded into the extended RAM address register located at 10h. Data in the addressed location can be read by performing a read operation from location 13h, or written-to by performing a write operation to location 13h. Data in any addressed location can be read or written repeatedly with changing the address in location 10h.

To read or write consecutive extended RAM locations, a burst mode feature can be enabled to increment the extended RAM address. To enable the burst mode feature, set the BME bit to a 1. With burst mode enabled, write the extended RAM starting address location to register 10h. Then read or write the extended RAM data from/to register 13h. The extended RAM address locations are automatically incremented on the rising edge of $\overline{OE}$, $\overline{WE}$, or $\overline{CS}$ only when register 13h is being accessed. Refer to the *Burst Mode Timing Waveform* (Figure 5) section. The address pointer wraps around after the last address is accessed.

Table 3. **DS1500 REGISTER MAP**

	DATA									BCD
Address	B7	B6	B5	B4	B3	B2	B1	B0	Function	Range
00H	0	10 SECONDS			SECONDS				Seconds	00 to 59
01H	0	10 MINUTES			MINUTES				Minutes	00 to 59
02H	0	0	10 HOURS		HOUR				Hours	00 to 23
03H	0	0	0	0	0	DAY			Day	1-7
04H	0	0	10 DATE		DATE				Date	01 to 31
05H	$\overline{\text{EOSC}}$	$\overline{\text{E32K}}$	BB32	10 MO	MONTH				Month	01 to 12
06H	10 YEAR				YEAR				Year	00 to 99
07H	10 CENTURY				CENTURY				Century	00 to 39
08H	AM1	10 SECONDS			SECONDS				Alarm Seconds	00 to 59
09H	AM2	10 MINUTES			MINUTES				Alarm Minutes	00 to 59
0AH	AM3	0	10 HOURS		HOUR				Alarm Hours	00 to 23
0BH	AM4	DY/DT	10 DATE		DAY/DATE				Alarm Day/Date	1 to 7/ 1 to 31
0CH	0.1 SECOND				0.01 SECOND				Watchdog	00 to 99
0DH	10 SECOND				SECOND				Watchdog	00 to 99
0EH	VRT1	VRT2	PRS	PAB	TDF	KSF	WDF	IRQF	Control A	
0FH	TE	CS	BME	TPE	TIE	KIE	WDE	WDS	Control B	
10H	EXTENDED RAM ADDRESS								RAM ADDR LSB	00 to FF
11H	RESERVED									
12H	RESERVED									
13H	EXTENDED RAM DATA								RAM DATA	00 to FF
14H	RESERVED									
15H	RESERVED									
16H	RESERVED									
17H	RESERVED									
18H	RESERVED									
19H	RESERVED									
1AH	RESERVED									
1BH	RESERVED									
1CH	RESERVED									
1DH	RESERVED									
1EH	RESERVED									
1FH	RESERVED									

0 = “0” and are read only

Note: Unless otherwise specified, the state of the control/RTC/SRAM bits in the DS1500 is not defined upon initial power application; the DS1500 should be properly configured/defined during initial configuration.

CONTROL REGISTERS

The controls and status information for the features offered by the DS1500 are maintained in the following register bits:

$\overline{\text{EOSC}}$ – Oscillator Start/Stop Bit (05H Bit 7)
This bit is used to turn the oscillator on and off.

1 – oscillator off
0 – oscillator on

$\overline{\text{E32K}}$ – Enable 32.768kHz Output (05H Bit 6)
This bit, when written to a 0, enables the 32.768kHz oscillator frequency to be output on the SQW pin if the oscillator is running.

BB32 – Battery-Backup 32kHz-Enable Bit (05H Bit 5)
When the BB32 bit is written to a 1, it enables a 32kHz signal to be output on the SQW pin while the part is in battery-backup mode if voltage is applied to V_{BAUX}.

AM1 to AM4 – Alarm Mask Bits (08H Bit 7; 09H Bit 7; 0AH Bit 7; 0BH Bit 7)
Bit 7 of registers 08h to 0Bh contains an alarm mask bit, AM1 to AM4. These bits, in conjunction with the TIE described later, allow the $\overline{\text{IRQ}}$ output to be activated for a matched-alarm condition.

The alarm can be programmed to activate on a specific day of the month, day of the week, or repeat every day, hour, minute, or second. Table 2 shows the possible settings for AM1 to AM4 and the resulting alarm rates. Configurations not listed in the table default to the once-per-second mode to notify the user of an incorrect alarm setting.

DY/DT – Day/Date Bit (0BH Bit 6)
The DY/DT bit controls whether the alarm value stored in bits 0 to 5 of 0BH reflects the day of the week or the date of the month. If DY/DT is written to a 0, the alarm is the result of a match with the date of the month. If DY/DT is written to a 1, the alarm is the result of a match with the day of the week.

VRT1 – Valid RAM and Time Bit 1 (0EH Bit 7)
VRT2 – Valid RAM and Time Bit 2 (0EH Bit 6)
These status bits give the condition of any batteries attached to the V_{BAT} or V_{BAUX} pins. The DS1500 constantly monitors the battery voltage of the backup-battery sources (V_{BAT} and V_{BAUX}). The VRT1 and VRT2 bits are set to a 1 if the battery voltage on V_{BAT} and V_{BAUX} are less than 2.5V (typical); otherwise, VRT1 and VRT2 bits are a 0. VRT1 reflects the condition of V_{BAT} with VRT2 reflecting V_{BAUX}. If either bit is read as a 0, the voltage on the respective pin is inadequate to maintain the RAM memory or clock functions.

PRS – Reset Select Bit (0EH Bit 5)
When set to a 0, the PWR pin is set high-Z when the DS1500 goes into power fail. When set to a 1, the $\overline{\text{PWR}}$ pin remains active upon entering power fail.

PAB – Power Active Bar Control Bit (0EH Bit 4)
When this bit is 0, the $\overline{\text{PWR}}$ pin is in the active-low state. When this bit is 1, the $\overline{\text{PWR}}$ pin is in the high-impedance state. This bit can be written to a 1 or 0 by the user. If either WF and WIE = 1 or KF and KSE = 1, the PAB bit is cleared to a 0.

TDF – Time-of-Day/Date Alarm Flag (0EH Bit 3)
A 1 in the TDF bit indicates that the current time has matched the alarm time. If the TIE bit is also a 1, the $\overline{\text{IRQ}}$ pin goes low and a 1 appears in the IRQF bit.

KSF – Kickstart Flag (0 EH Bit 2)
This bit is set to a 1 when a kickstart condition occurs or when the user writes it to a 1. This bit is cleared by writing it to a 0.

WDF – Watchdog Flag (0 EH Bit 1)
If the processor does not access the DS1500 with a write within the period specified in addresses 0CH and 0DH, the WDF bit is set to a 1. WDF is cleared by writing it to a 0.

IRQF – Interrupt Request Flag (0 EH Bit 0)
The interrupt request flag (IRQF) bit is set to a 1 when one or more of the following are true:
TDF = TIE = 1
KSF = KIE = 1
WDF = WDE = 1

i.e., IRQF = (TDF x TIE) + (KSF x KIE) + (WDF x WDE)

Any time the IRQF bit is a 1, the $\overline{\text{IRQ}}$ pin is driven low.

TE – Transfer Enable Bit (0 FH Bit 7)
When the TE bit is a 1, the update transfer functions normally by advancing the counts once per second. When the TE bit is written to a 0, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. TE is a read/write bit that is not modified by internal functions of the DS1500.

CS – Crystal Select Bit (0 FH Bit 6)
When CS is set to a 0, the oscillator is configured for operation with a crystal that has a 6pF specified load capacitance. When CS = 1, the oscillator is configured for a 12.5pF crystal. CS is disabled in the DS1510 module and should be set to CS = 0.

BME – Burst-Mode Enable Bit (0 FH Bit 5)
The burst-mode enable bit allows the extended user RAM address registers to automatically increment for consecutive reads and writes. When BME is set to a 1, the automatic incrementing is enabled; when BME is set to a 0, the automatic incrementing is disabled.

TPE – Time-of-Day/Date Alarm Power-Enable Bit (0 FH Bit 4)
The wake-up feature is controlled through the TPE bit. When the TDF flag bit is set to a 1, if TPE is a 1, the $\overline{PWR}$ pin is driven active. Therefore, setting TPE to 1 enables the wake-up feature. Writing a 0 to TPE disables the wake-up feature.

TIE – Time-of-Day/Date Alarm Interrupt-Enable Bit (0 FH Bit 3)
The TIE bit allows the TDF flag to assert an interrupt. When the TDF flag bit is set to a 1, if TIE is a 1, the IRQF flag bit is set to a 1. Writing a 0 to the TIE bit prevents the TDF flag from setting the IRQF flag.

KIE – Kickstart Enable-Interrupt Bit (0 FH Bit 2)
When V_{CCI} voltage is absent and KIE is set to a 1, the $\overline{PWR}$ pin is driven active-low when a kickstart condition occurs ($\overline{KS}$ pulsed low), causing the KSF bit to be set to 1. When V_{CCI} is then applied, the $\overline{IRQ}$ pin is also driven low. If KIE is set to 1 while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ are driven low in response to KSF being set to 1. When KIE is cleared to a 0, the KSF bit has no affect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

WDE – Watchdog Enable Bit (0 FH Bit 1)
When WDE is set to a 1, the watchdog function is enabled, and either the $\overline{IRQ}$ pin or $\overline{RST}$ pin is pulled active based on the state of the WDS bit.

WDS – Watchdog Steering Bit (0 FH Bit 0)
If WDS is a 0 when the WDF bit is set to a 1, the $\overline{IRQ}$ pin is pulled low. If WDS is a 1 when WDF is set to a 1, the watchdog outputs a negative pulse on the $\overline{RST}$ output for 40ms to 200ms, and the IRQF flag is set when the watchdog times out. The WDE bit is reset to a 0 immediately after $\overline{RST}$ goes active.

ABSOLUTE MAXIMUM RATINGS*

Voltage Range on Any Pin Relative to Ground	-0.5V to +6.0V
Commercial Operating Temperature Range	0°C to +70°C
Industrial Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature Range	See IPC/JEDEC J-STD-020A

* This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

OPERATING RANGE

RANGE	TEMP. RANGE	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial	-40°C to +85°C	5V ±10%

RECOMMENDED DC OPERATING CONDITIONS (Over the operating range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power-Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Voltage All Inputs V_{CCI} = 5V ±10%	V_{IH}	2.2		V_{CCI} + 0.3	V	1
Logic 0 Voltage All Inputs V_{CCI} = 5V ±10%	V_{IL}	-0.3		0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	1
Auxiliary-Battery Voltage	V_{BAUX}	2.5		5.3	V	1

DC ELECTRICAL CHARACTERISTICS

(Over the operating range; V_{CCI} = 5.0V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CC}			15	mA	2
TTL Standby Current ($\overline{CS}$ = V_{IH})	I_{CC1}			5	mA	2
CMOS Standby Current ($\overline{CS}$ ≥ V_{CCI} - 0.2V)	I_{CC2}			5	mA	2
Battery Current, Oscillator On	I_{BAT1}			1.0	µA	9
Battery Current, Oscillator Off	I_{BAT2}			0.1	µA	9
Input-Leakage Current (Any Input)	I_{IL}	-1		1	µA	
Output-Leakage Current (Any Output)	I_{OL}	-1		1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4			V	1
Output Logic 0 Voltage I_{OUT} = 2.1mA, DQ0–7 Outputs, $\overline{CEO}$	V_{OL1}			0.4	V	1
I_{OUT} = 7.0mA, $\overline{IRQ}$, $\overline{PWR}$, and $\overline{RST}$ Outputs	V_{OL2}			0.4	V	1, 3
Output Voltage	V_{CCO1}	V_{CCI} - 0.3			V	7
Output Current	I_{CCO1}			85	mA	7
Write-Protection Voltage	V_{PF}	4.25		4.50	V	1
Battery-Switchover Voltage	V_{SO}		V_{BAT}, V_{BAUX}		V	1, 4
Output Voltage	V_{CCO2}	V_{BAT} - 0.3			V	8
Output Current	I_{CCO2}			50	µA	8

AC OPERATING CHARACTERISTICS

(Over the operating range; V_{CCI} = 5.0V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	70			ns	
Address Access Time	t_{AA}			70	ns	
$\overline{CS}$ to DQ Low-Z	t_{CSL}	5			ns	10
$\overline{CS}$ Access Time	t_{CSA}			70	ns	
$\overline{CS}$ Data Off Time	t_{CSZ}			25	ns	10
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5			ns	10
$\overline{OE}$ Access Time	t_{OEA}			35	ns	
$\overline{OE}$ Data Off Time	t_{OEZ}			25	ns	10
Output Hold from Address	t_{OH}	5			ns	
Write Cycle Time	t_{WC}	70			ns	
Address Setup Time	t_{AS}	0			ns	
$\overline{WE}$ Pulse Width	t_{WEW}	50			ns	
$\overline{CS}$ Pulse Width	t_{CSW}	55			ns	
Data Setup Time	t_{DS}	30			ns	
Data Hold Time	t_{DH}	0			ns	
Address Hold Time	t_{AH}	0			ns	
$\overline{WE}$ Data Off Time	t_{WEZ}			25	ns	10
Write Recovery Time	t_{WR}	5			ns	
$\overline{CEI}$ to $\overline{CEO}$ Propagation Delay	t_{CEPD}			10	ns	

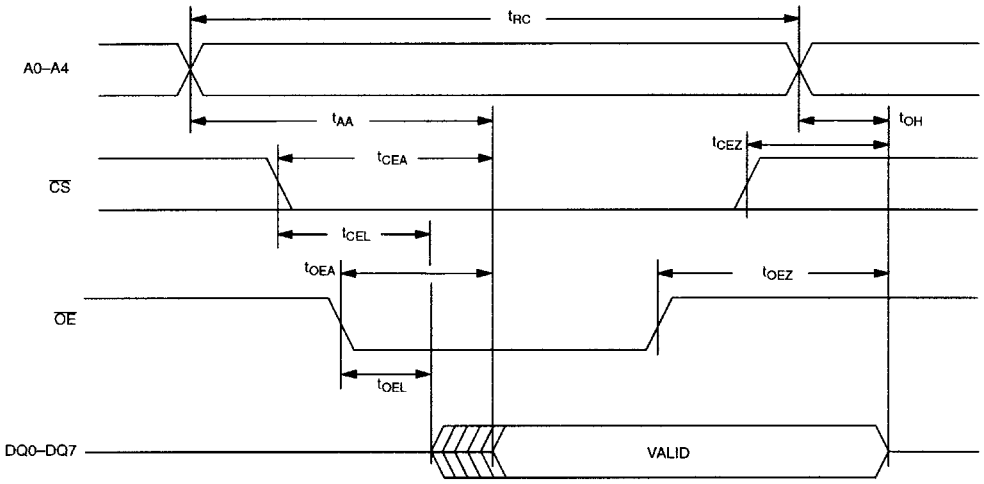


Figure 3. **WRITE CYCLE TIMING, WRITE ENABLE-CONTROLLED**

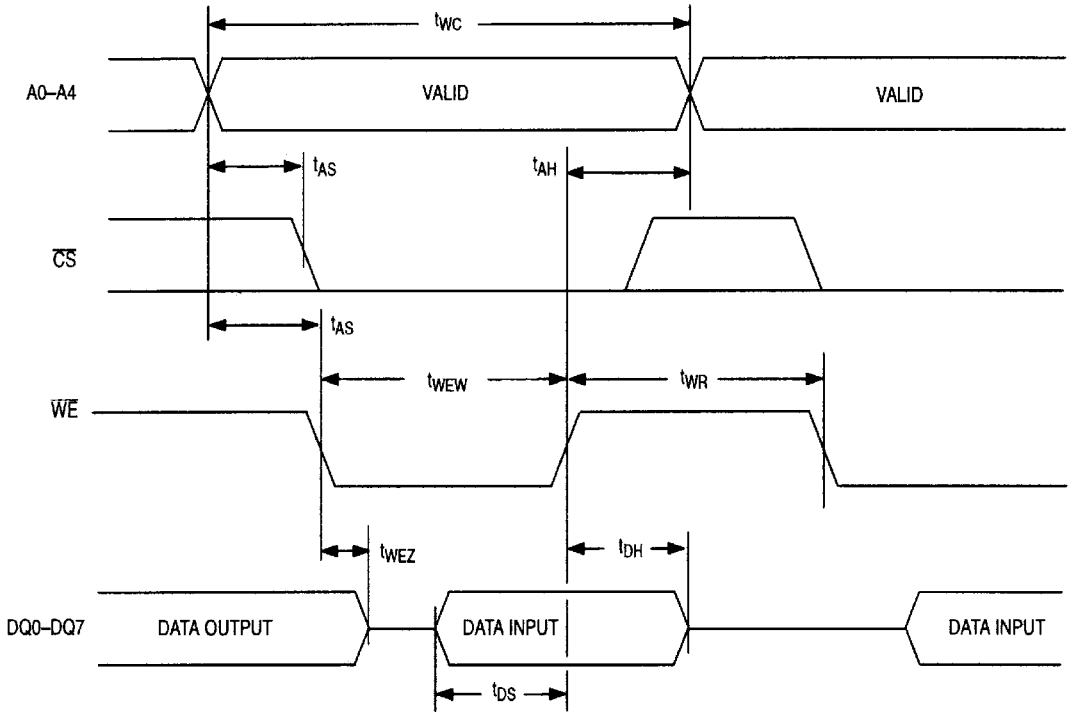
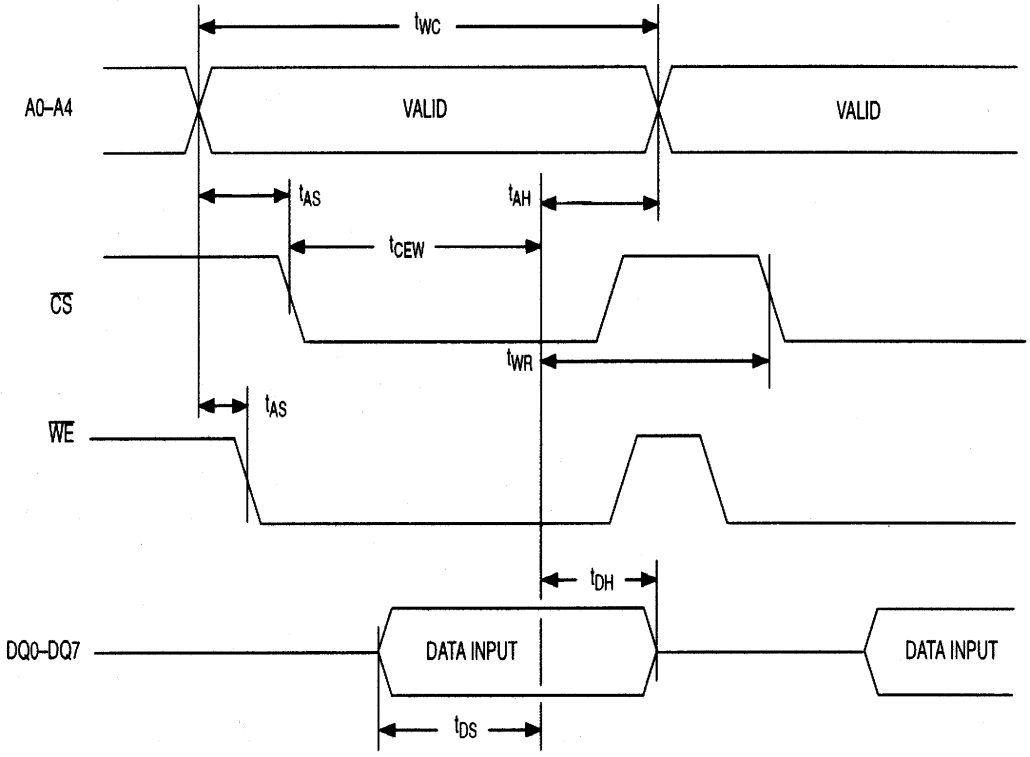


Figure 4. **WRITE CYCLE TIMING, CHIP ENABLE-CONTROLLED**



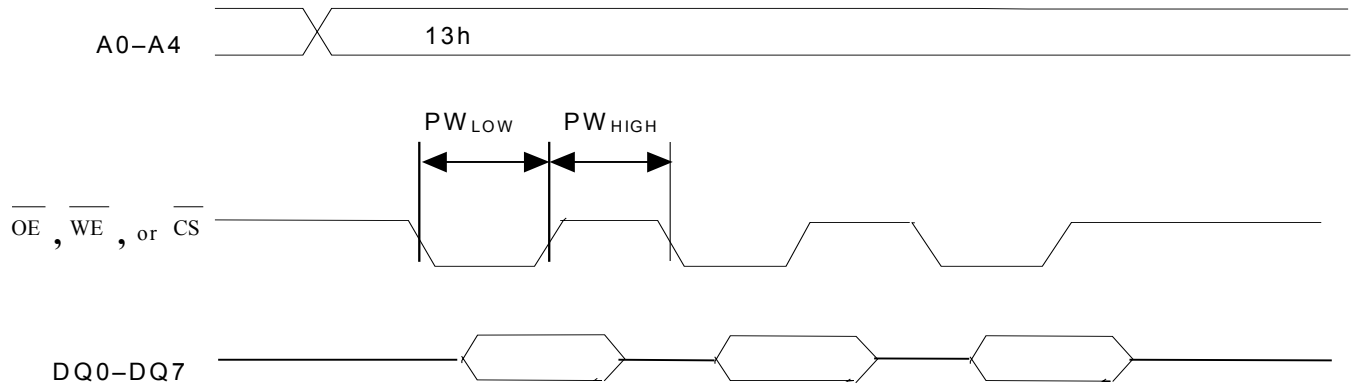
BURST MODE TIMING CHARACTERISTICS (V_{CCI} = 5.0V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pulse Width, $\overline{OE}$, $\overline{WE}$, or $\overline{CS}$ High	PW_{HIGH}	**TBD**			ns	
Pulse Width, $\overline{OE}$, $\overline{WE}$, or $\overline{CS}$ Low	PW_{LOW}	**TBD**			ns	

BURST MODE TIMING CHARACTERISTICS (V_{CCI} = 3.3V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pulse Width, $\overline{OE}$, $\overline{WE}$, or $\overline{CS}$ High	PW_{HIGH}	**TBD**			ns	
Pulse Width, $\overline{OE}$, $\overline{WE}$, or $\overline{CS}$ Low	PW_{LOW}	**TBD**			ns	

Figure 5. **BURST MODE TIMING WAVEFORM**



POWER-UP/DOWN CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$, $\overline{CEI}$, or $\overline{WE}$ at V_{IH} before Power Fail	t_{PF}	0			µs	
V_{CCI} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CCI} Fall Time: $V_{PF(MIN)}$ to V_{SO}	t_{FB}	10			µs	
V_{CCI} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	
V_{PF} to $\overline{RST}$ High	t_{REC}	40		200	ms	

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data-Retention Time (Oscillator On)	t_{DR}	10			years	6

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on All Input Pins	C_{IN}			10	pF	
Capacitance on $\overline{IRQ}$, $\overline{PWR}$, $\overline{RST}$, and DQ pins	C_{IO}			10	pF	

AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0V to 3.0V for 5V operation

Timing Measurement Reference Levels:
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

Figure 6. **POWER-UP/DOWN WAVEFORM TIMING, 5V**

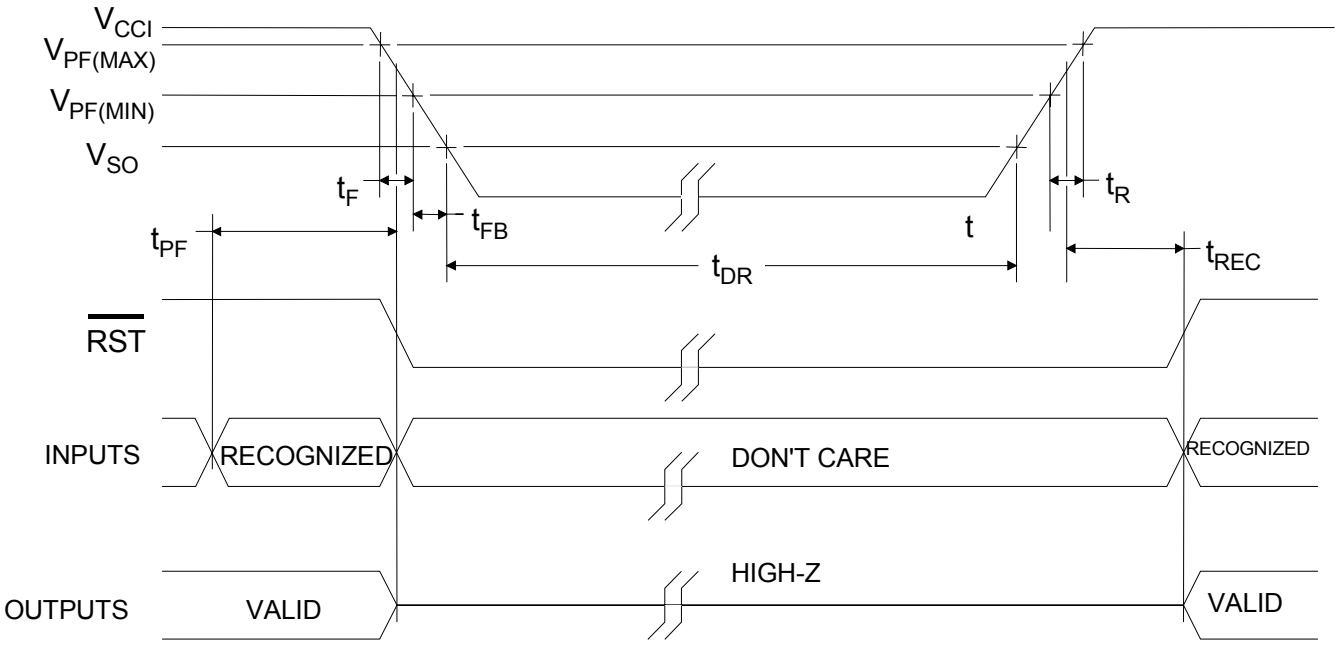
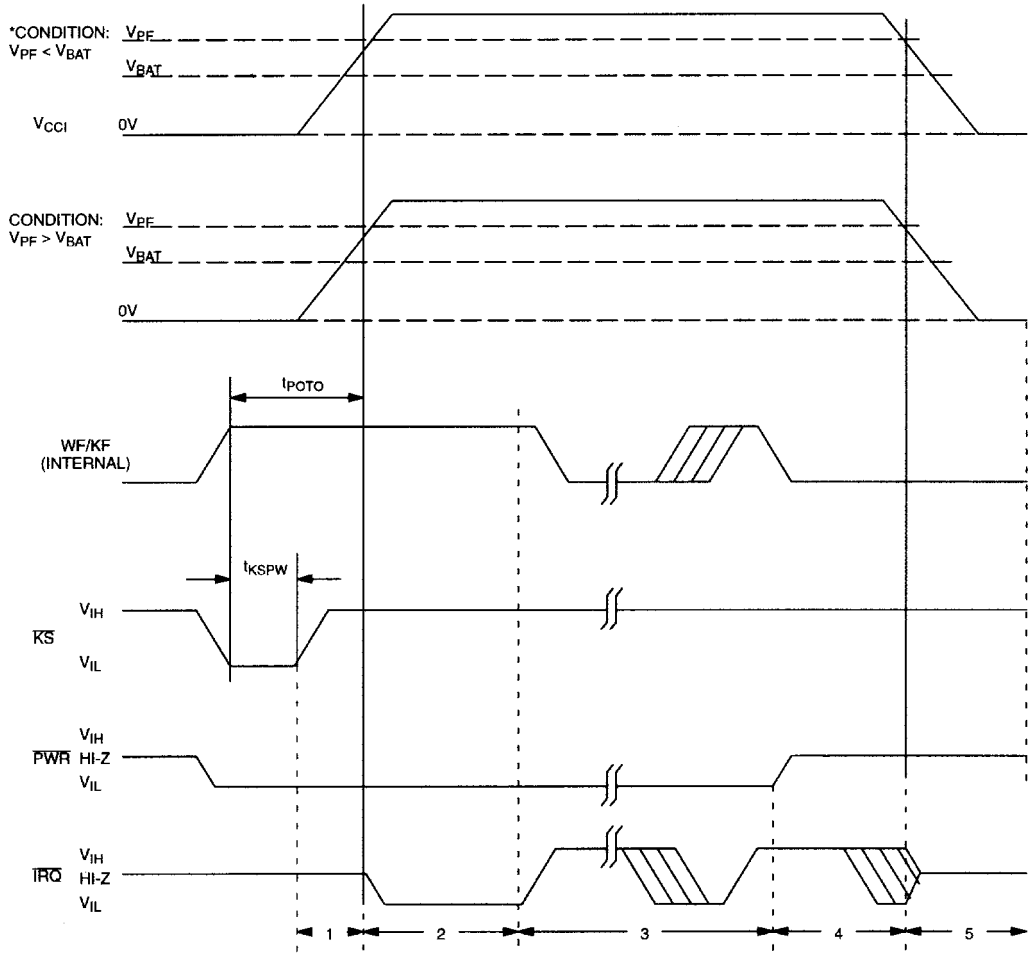


Figure 7. **WAKE-UP/KICKSTART TIMING DIAGRAM**



Note: Time intervals shown above are referenced in the *Wake-Up/Kickstart* section.

WAKE-UP/KICKSTART TIMING

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Kickstart-Input Pulse-Width	t_{KSPW}	2			µs	
Wake-Up/Kickstart Power-On Timeout	t_{POTO}	2			s	5

NOTES:

1) Voltage referenced to ground.
2) Outputs are open.
3) The $\overline{IRQ}$, $\overline{PWR}$, and $\overline{RST}$ outputs are open drain.
4) Battery switchover occurs at the battery terminal-voltage level.
5) Wake-up/kickstart timeout generated only when the oscillator is enabled and the countdown chain is not reset.
6) t_{DR} is specified with V_{CCO} floating. If V_{CCO} is powering an external SRAM, an auxiliary battery should be connected to the V_{BAUX} pin. The auxiliary battery should be sized such that it can power the external SRAM for the t_{DR} period.
7) Value for voltage and currents is from the V_{CCI} input pin to the V_{CCO} pin.
8) Value for voltage and currents is from the V_{BAT} or V_{BAUX} input pin to the V_{CCO} pin.
9) I_{BAT1} and I_{BAT2} are specified with V_{CCO} floating and do not include any RAM current.
10) These parameters are sampled with a 5pF load and are not 100% tested.