

### 32768-word × 8-bit High Speed CMOS Static RAM *Preliminary*

#### Description

The CXK5T8257BTM/BYM/BM is 262,144 bits high speed CMOS static RAM organized as 32768-words by 8 bits.

Special feature are low power consumption and high speed.

The CXK5T8257BTM/BYM/BM is a suitable RAM for portable equipment with battery back up.

#### Features

- Extended operating temperature range: -25 to +85°C
- Wide supply voltage range operation: 2.7 to 3.6V
- Fast access time: (Access time)
 

3.0V operation	-10LLX	100ns (Max.)
	-12LLX	120ns (Max.)
3.3V operation	-10LLX	85ns (Max.)
	-12LLX	100ns (Max.)
- Low standby current: 7.0μA (Max.)
- Low power data retention: 2.0V (Min.)
- Available in many packages

CXK5T8257BTM/BYM

8mm × 13.4mm 28 pin TSOP Package

CXK5T8257BM

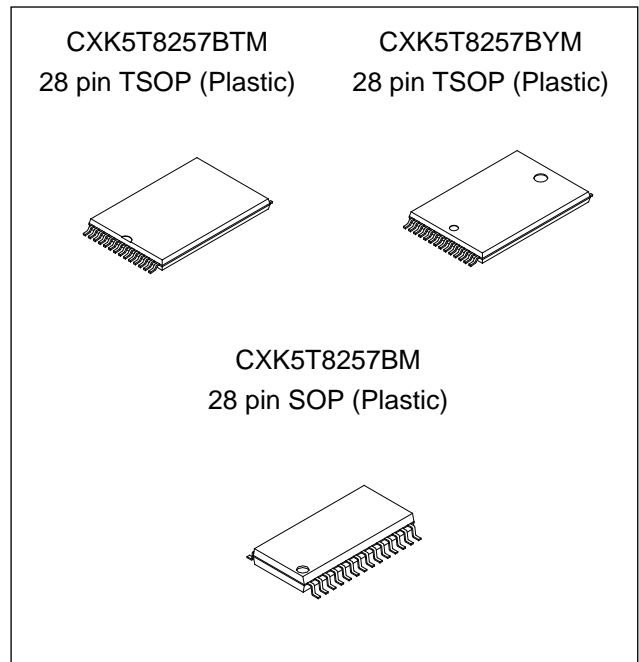
450mil 28 pin SOP Package

#### Function

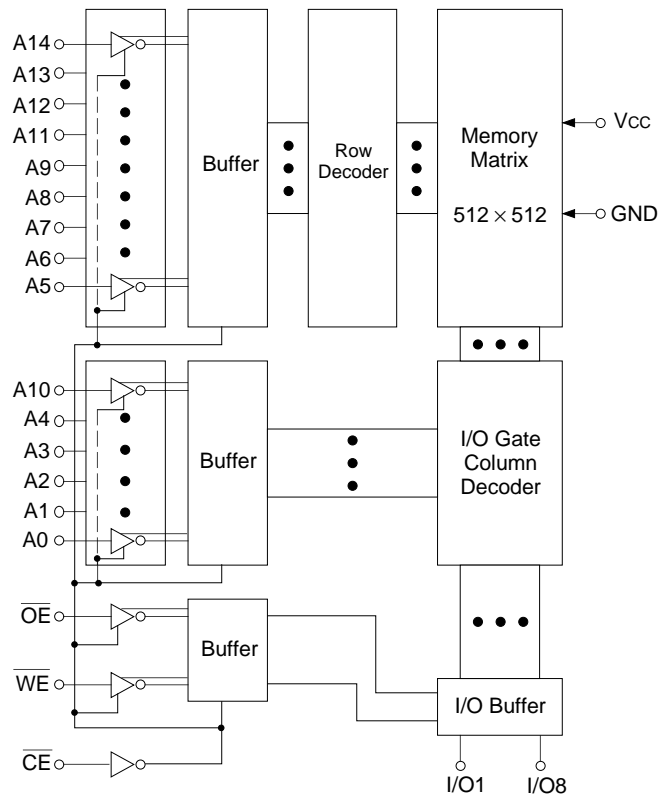
32768-word × 8 bit static RAM

#### Structure

Silicon gate CMOS IC

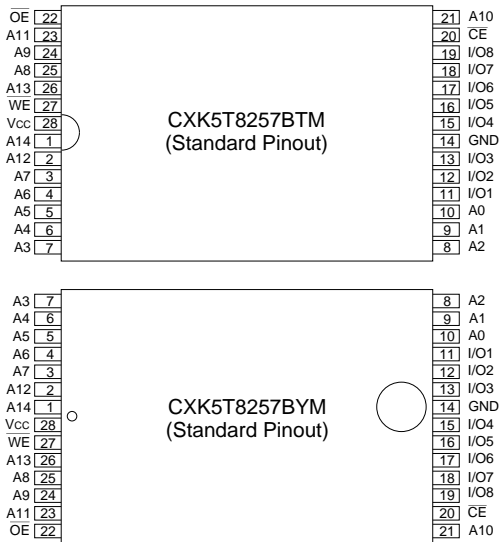


#### Block Diagram



Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply
GND	Ground

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	-0.5 to +4.6	V
Input voltage	V <sub>IN</sub>	-0.5*1 to V <sub>CC</sub> + 0.5	V
Input and output voltage	V <sub>I/O</sub>	-0.5*1 to V <sub>CC</sub> + 0.5	V
Allowable power dissipation	P <sub>D</sub>	0.7	W
Operating temperature	T <sub>opr</sub>	-25 to +85	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C
Soldering temperature · time	T <sub>solder</sub>	235 · 10	°C · s

\*1 V<sub>IN</sub>, V<sub>I/O</sub> = -3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	×	×	Not selected	High Z	I <sub>SB1</sub> , I <sub>SB2</sub>
L	H	H	Output disable	High Z	I <sub>CC1</sub> , I <sub>CC2</sub>
L	L	H	Read	Data out	I <sub>CC1</sub> , I <sub>CC2</sub>
L	×	L	Write	Data in	I <sub>CC1</sub> , I <sub>CC2</sub>

x: "H" or "L"

**DC Recommended Operating Conditions**

(Ta = -25 to +85°C, GND = 0V)

Item	Symbol	Vcc = 2.7 to 3.6V			Vcc = 3.3V ± 0.3V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	Vcc	2.7	3.3	3.6	3.0	3.3	3.6	V
Input high voltage	V <sub>IH</sub>	2.4	—	Vcc + 0.3	2.2	—	Vcc + 0.3	
Input low voltage	V <sub>IL</sub>	-0.3*1	—	0.4	-0.3*1	—	0.6	

\*1 V<sub>IL</sub> = -3.0V Min. for pulse width less than 50ns.

**Electrical Characteristics**

• **DC characteristics**

(Vcc = 2.7 to 3.6V, GND = 0V, Ta = -25 to +85°C)

Item	Symbol	Test Conditions	Min.	Typ.*2	Max.	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = GND to Vcc	-0.5	—	0.5	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CE} = V_{IH}$ OE = V <sub>IH</sub> or $\overline{WE} = V_{IL}$ V <sub>I/O</sub> = GND to Vcc	-0.5	—	0.5		
Operating power supply current	I <sub>CC1</sub>	$\overline{CE} = V_{IL}$ V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OUT</sub> = 0mA	—	0.9	2	mA	
Average operating current	I <sub>CC2</sub>	Min. cycle duty = 100%, I <sub>OUT</sub> = 0mA	—	18*3	35*4		
Standby current	I <sub>SB1</sub>	$\overline{CE} \geq V_{CC} - 0.2V$	-25 to +85°C	—	—	7.0	μA
			-25 to +70°C	—	—	3.5	
			+25°C	—	0.12	—	
	I <sub>SB2</sub>	$\overline{CE} = V_{IH}$	—	0.06	0.7	mA	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2mA	2.4	—	—	V	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.0mA	—	—	0.4		

\*2 Vcc = 3.3V, Ta = 25°C

\*3 I<sub>CC2</sub> = 21mA for 3.3V operation (Vcc = 3.3V ± 0.3V)

\*4 I<sub>CC3</sub> = 40mA for 3.3V operation (Vcc = 3.3V ± 0.3V)

**I/O capacitance**

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	—	—	8	pF
I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	—	—	10	pF

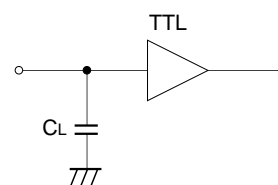
**Note)** This parameter is sampled and is not 100% tested.

**AC Characteristics**

• **AC test conditions**

(Ta = -25 to +85°C)

Item	Conditions		
	V <sub>CC</sub> = 2.7 to 3.6V	V <sub>CC</sub> = 3.3V ± 0.3V	
Input pulse high level	V <sub>IH</sub> = 2.4V	V <sub>IH</sub> = 2.2V	
Input pulse low level	V <sub>IL</sub> = 0.4V	V <sub>IL</sub> = 0.6V	
Input rise time	t <sub>r</sub> = 5ns	t <sub>r</sub> = 5ns	
Input fall time	t <sub>f</sub> = 5ns	t <sub>f</sub> = 5ns	
Input and output reference level	1.4V	1.4V	
Output load conditions	-10LLX	C <sub>L</sub> *1 = 100pF, 1TTL	C <sub>L</sub> *1 = 30pF, 1TTL
	-12LLX	C <sub>L</sub> *1 = 100pF, 1TTL	C <sub>L</sub> *1 = 100pF, 1TTL



\*1 C<sub>L</sub> includes scope and jig capacitances.

• Read cycle ( $\overline{WE} = "H"$ )

Item	Symbol	V <sub>CC</sub> = 2.7 to 3.6V				V <sub>CC</sub> = 3.3V ± 0.3V				Unit
		-10LLX		-12LLX		-10LLX		-12LLX		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t <sub>RC</sub>	100	—	120	—	85	—	100	—	ns
Address access time	t <sub>AA</sub>	—	100	—	120	—	85	—	100	
Chip enable access time ( $\overline{CE}$ )	t <sub>CO</sub>	—	100	—	120	—	85	—	100	
Chip enable to output valid	t <sub>OE</sub>	—	50	—	60	—	50	—	50	
Chip hold from address change	t <sub>OH</sub>	20	—	20	—	20	—	20	—	
Chip enable to output in low Z ( $\overline{CE}$ )	t <sub>LZ</sub>	10	—	10	—	10	—	10	—	
Output enable to output in low Z ( $\overline{OE}$ )	t <sub>OLZ</sub>	10	—	10	—	10	—	10	—	
Chip disable to output in high Z ( $\overline{CE}$ )	t <sub>HZ</sub> *1	—	35	—	40	—	35	—	35	
Output disable to output in high Z ( $\overline{OE}$ )	t <sub>OHZ</sub> *1	—	35	—	35	—	35	—	35	

\*1 t<sub>HZ</sub> and t<sub>OHZ</sub> are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

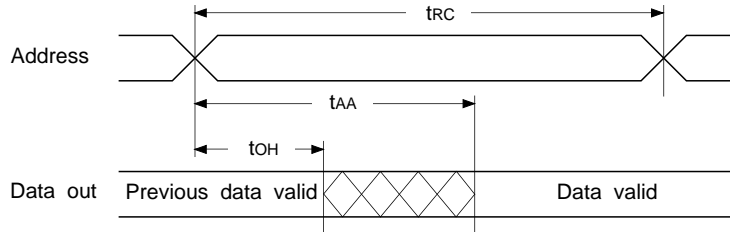
• Write cycle

Item	Symbol	V <sub>CC</sub> = 2.7 to 3.6V				V <sub>CC</sub> = 3.3V ± 0.3V				Unit
		-10LLX		-12LLX		-10LLX		-12LLX		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t <sub>WC</sub>	100	—	120	—	85	—	100	—	ns
Address valid to end of write	t <sub>AW</sub>	80	—	100	—	80	—	80	—	
Chip enable to end of write	t <sub>CW</sub>	80	—	100	—	80	—	80	—	
Data to write time overlap	t <sub>DW</sub>	35	—	50	—	35	—	35	—	
Data hold from write time	t <sub>DH</sub>	0	—	0	—	0	—	0	—	
Write pulse width	t <sub>WP</sub>	60	—	70	—	60	—	60	—	
Address setup time	t <sub>AS</sub>	0	—	0	—	0	—	0	—	
Write recovery time ( $\overline{WE}$ )	t <sub>WR</sub>	0	—	0	—	0	—	0	—	
Write recovery time ( $\overline{CE}$ )	t <sub>WR1</sub>	0	—	0	—	0	—	0	—	
Output active from end of write	t <sub>OW</sub>	10	—	10	—	10	—	10	—	
Write to output in high Z	t <sub>WHZ</sub> *2	—	35	—	40	—	35	—	35	

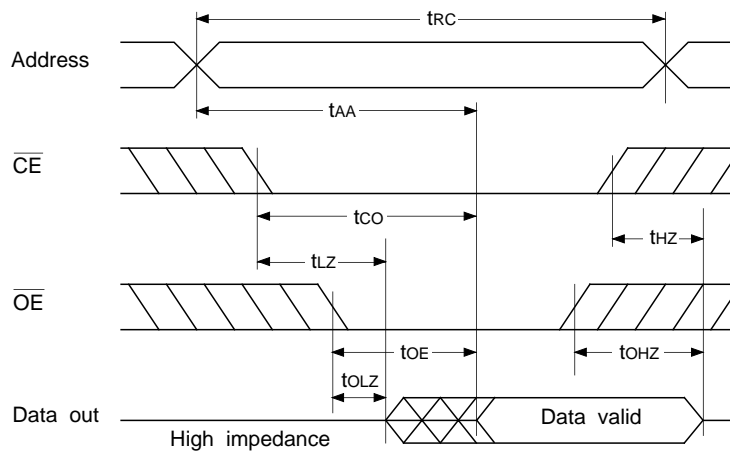
\*2 t<sub>WHZ</sub> is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing waveform

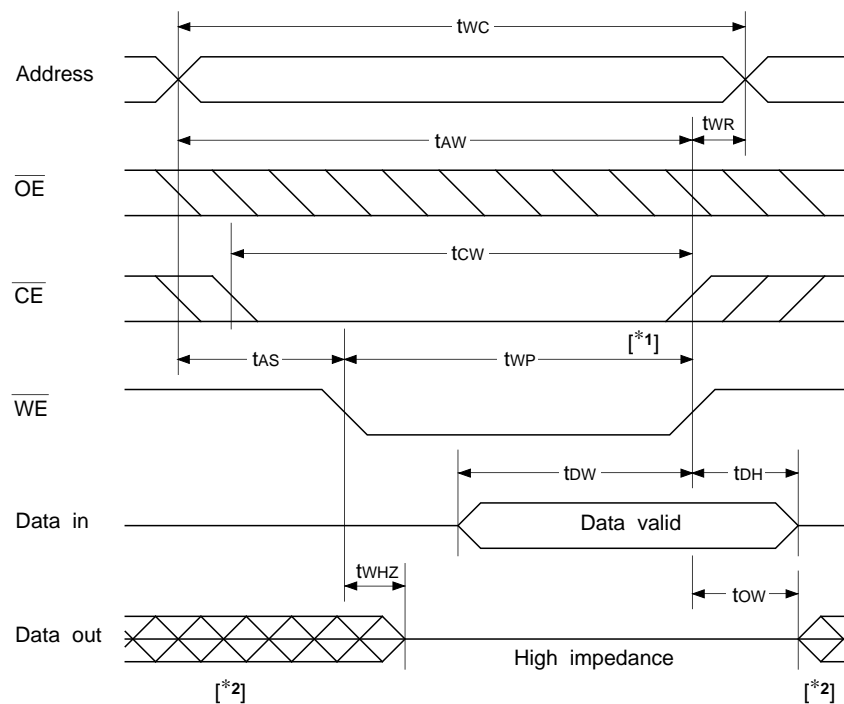
- Read cycle (1) :  $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$



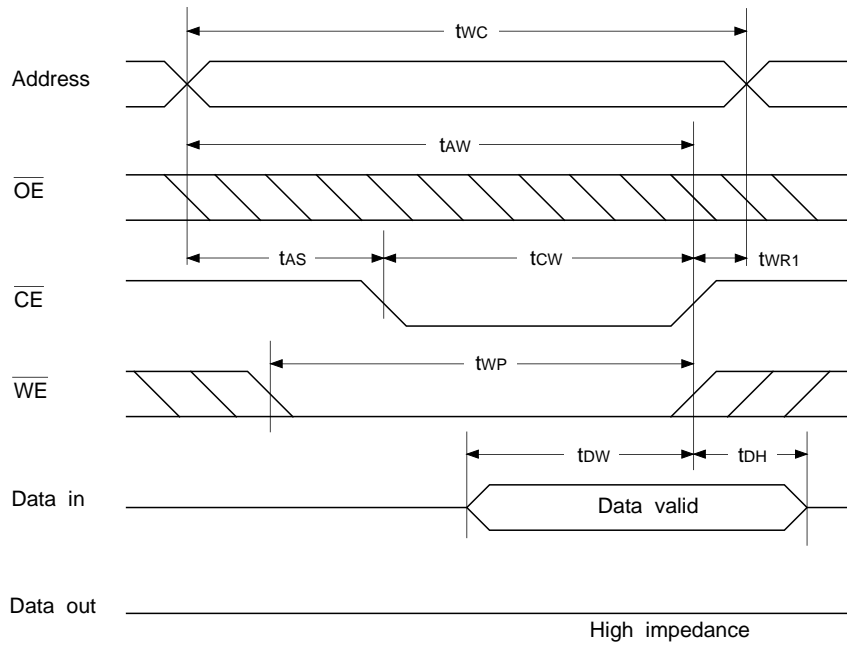
- Read cycle (2):  $\overline{WE} = V_{IH}$



- Write cycle (1) :  $\overline{WE}$  control



• Write cycle (2):  $\overline{CE}$  control

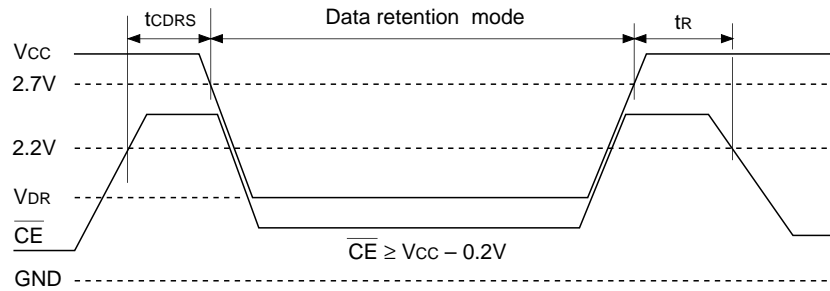


\*1 Write is executed when both  $\overline{CE}$  and  $\overline{WE}$  are at low simultaneously.

\*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is output condition.

**Data Retention Waveform**

- Low supply voltage data retention waveform



**Data Retention Characteristics**

(Ta = -25 to +85°C)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit	
Data retention voltage	V <sub>DR</sub>	$\overline{CE} \geq V_{CC} - 0.2V$	2	—	3.6	V	
Data retention current	I <sub>CCDR1</sub>	$V_{CC} = 3.0V$ $\overline{CE} \geq 2.8V$	-25 to +85°C	—	—	6	μA
			-25 to +70°C	—	—	3	
			+25°C	—	0.1	—	
	I <sub>CCDR2</sub>	$V_{CC} = 2.0 \text{ to } 3.6V$ $\overline{CE} \geq V_{CC} - 0.2V$	—	0.12*1	7.0		
Data retention setup time	t <sub>CDRS</sub>	Chip disable to data retention mode	0	—	—	ns	
Recovery time	t <sub>R</sub>		5	—	—	ms	

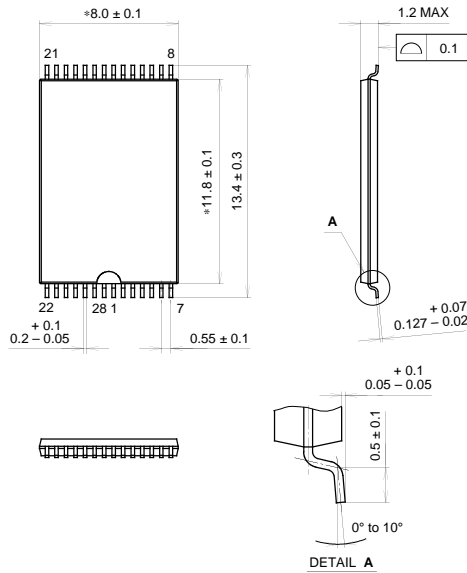
\*1 V<sub>CC</sub> = 3.3V, Ta = 25°C



Package Outline Unit: mm

CXK5T8257BTM

28PIN TSOP (Plastic)



NOTE: Dimension "\*" does not include mold protrusion.

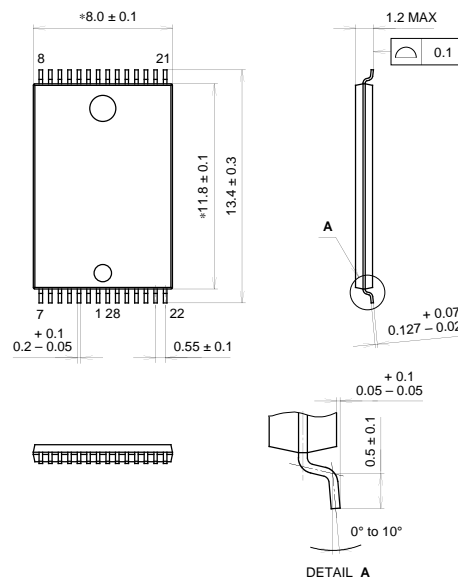
PACKAGE STRUCTURE

SONY CODE	TSOP-28P-L01
EIAJ CODE	TSOP028-P-0000-A
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.2g

CXK5T8257BYM

28PIN TSOP (Plastic)



NOTE: Dimension "\*" does not include mold protrusion.

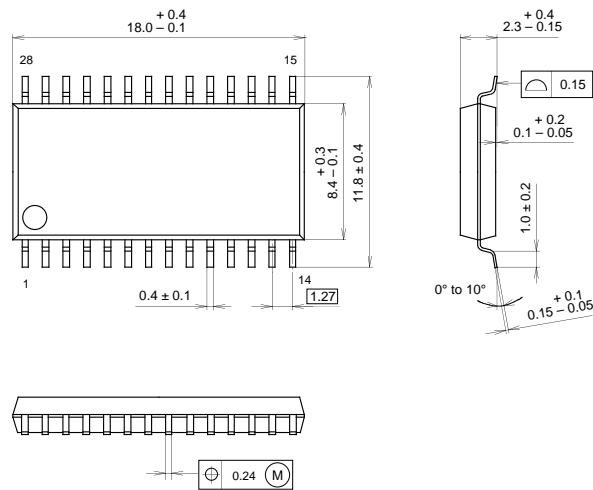
PACKAGE STRUCTURE

SONY CODE	TSOP-28P-L01R
EIAJ CODE	TSOP028-P-0000-B
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.2g

CXK5T8257BM

28PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-28P-L05
EIAJ CODE	+SOP028-P-0450
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.7g