FUJITSU

CMOS 262144-BIT STATIC RANDOM ACCESS MEMORY

MB 84256-10/10L/10LL
MB 84256-12/12L/12LL
MB 84256-15/15L/15LL

T-46-23-14

August 1986
Edition 2.0

256K-BIT (32,768 x 8) CMOS STATIC RANDOM ACCESS MEMORY WITH DATA RETENTION AND LOW POWER

The Fujitsu MB 84256 is a 32,768-word by 8-bit static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronouse circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5 volts power supply is required.

The MB 84256 is ideally suited for use in microprocesser systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

- Organization: 32,768 x 8 bits
- Fast access time: 100 ns max. (MB 84256-10/10L/10LL)
  120 ns max. (MB 84256-12/12L/12LL)
  150 ns max. (MB 84256-15/15L/15LL)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three-state outputs
- Single +5V power supply, ±10% tolerance
- Low power standby:
  CMOS level: 5.5 mW max. (MB 84256-10/12/15)
  0.55 mW max. (MB 84256-10L/10LL/12L/12LL/15L/15LL)
  TTL level: 16.5 mW max. (MB 84256-10/10L/10LL/12/12L/12LL/15/15L/15LL)
- Data retention: 2.0V
- Standard 28-pin DIP (600 mil) (Suffix: -P)
- Standard 28-pin Bend-type Plastic Flat Package (450 mil) (Suffix: -PF)
- Standard 32-pad LCC (Suffix: -CV)

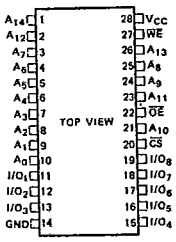
PLASTIC PACKAGE
DIP-28P-M02

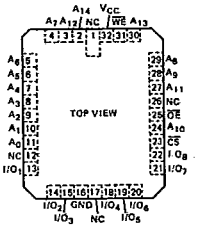
PLASTIC PACKAGE
FPT-28P-M02

CERAMIC PACKAGE
LCC-32C-A02

3F

PIN ASSIGNMENT





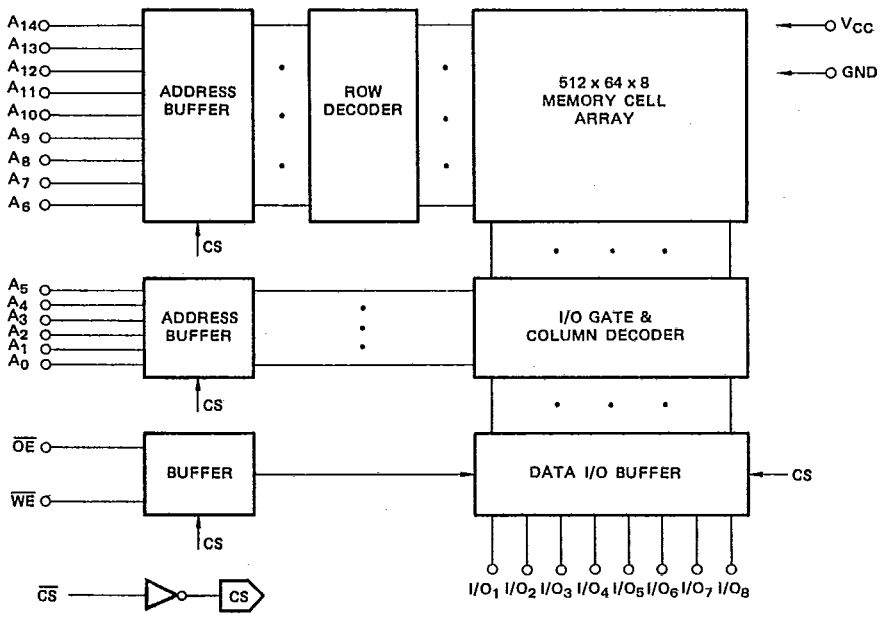
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage		V_{IN}	−0.5 to V_{CC}+0.5	V
Output Voltage		V_{OUT}	−0.5 to V_{CC}+0.5	V
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	CERAMIC	T_{STG}	−65 to +150	°C
	PLASTIC		−40 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 84256 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	NOT SELECTED	I_{SB}	HIGH-Z
L	H	H	DOUT DISABLE	I_{CC}	HIGH-Z
L	L	H	READ	I_{CC}	D_{OUT}
L	X	L	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0 *		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V
Ambient Temperature	T_A	0		70	°C

* -2.0 V Min. for pulse width less than 20 ns. (V_{IL} Min = -0.3 V at DC level)

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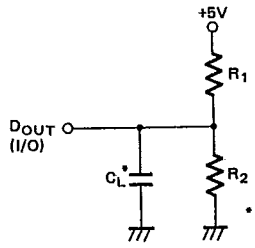
DC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter	Symbol	MB 84256-10/12/15		MB 84256-10L/10LL/12L/12LL/15L/15LL		Unit	Test Conditions
		Min	Max	Min	Max		
Standby Supply Current	I_{SB1}		1		0.1	mA	$\overline{CS} \geqq V_{CC}$-0.2V
	I_{SB2}		3		3		$\overline{CS} = V_{IH}$
Active Supply Current	I_{CC1}		45		45	mA	$\overline{CS} = V_{IL}$, $V_{IN} = V_{IH}$ or V_{IL}, I_{OUT} = 0 mA
Operating Supply Current	I_{CC2}		70		70		Cycle = Min., Duty = 100%, I_{OUT} = 0 mA
Input Leakage Current	I_{LI}	-1	1	-1	1	μA	V_{IN} = 0V to V_{CC}
Output Leakage Current	$I_{LI/O}$	-1	1	-1	1	μA	$V_{I/O}$ = 0V to V_{CC}, $\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Output High Voltage	V_{OH}	2.4		2.4		V	I_{OH} = -1.0 mA
Output Low Voltage	V_{OL}		0.4		0.4	V	I_{OL} = 2.1 mA

Note: All voltages are referenced to GND

Fig. 2 – AC TEST CONDITIONS



- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V; Output: V_{OL} = 0.8V, V_{OH} = 2.0V
- Output Load

* Including Jig and stray capacitance

	R_1	R_2	C_L	Parameters Measured
Load I	1.8KΩ	990Ω	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}
Load II	1.8KΩ	990Ω	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}

AC CHARACTERISTICS

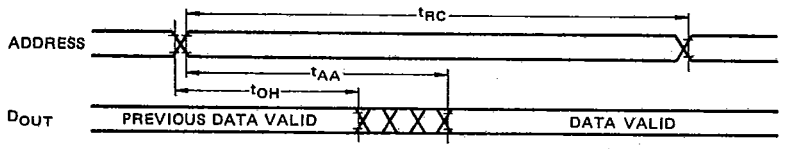
(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

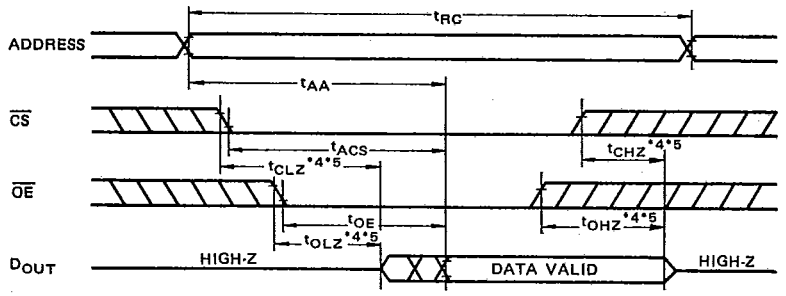
Parameter	Symbol	MB 84256-10/ 10L/10LL		MB 84256-12/ 12L/12LL		MB 84256-15/ 15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time*2	t_{AA}		100		120		150	ns
$\overline{CS}$ Access Time*3	t_{ACS}		100		120		150	ns
Output Enable to Output Valid	t_{OE}		40		50		60	ns
Output Hold from Address Change	t_{OH}	20		20		20		ns
Chip Select to Output Low-Z*4*5	t_{CLZ}	10		10		10		ns
Output Enable to Output Low-Z*4*5	t_{OLZ}	5		5		5		ns
Chip Select to Output High-Z*4*5	t_{CHZ}		40		40		50	ns
Output Enable to Output High-Z*4*5	t_{OHZ}		40		40		50	ns

READ CYCLE TIMING DIAGRAM *1

READ CYCLE I: ADDRESS CONTROLLED*2



READ CYCLE II: $\overline{CS}$ CONTROLLED*3



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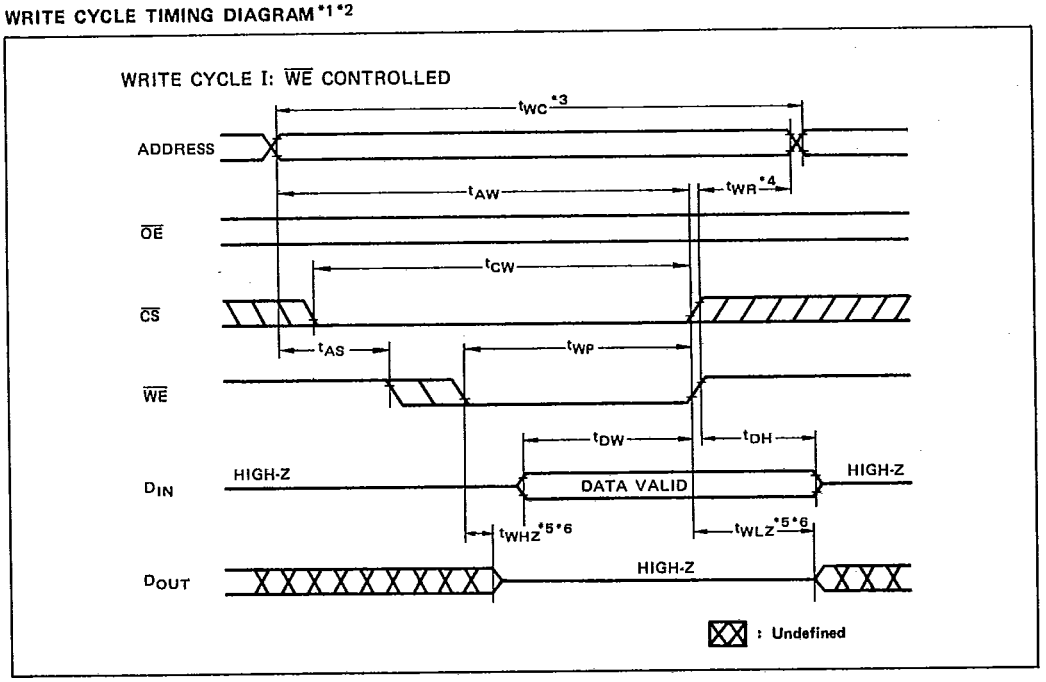
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS} = \overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE*1*2

Parameter	Symbol	MB 84256-10/ 10L/10LL		MB 84256-12/ 12L/12LL		MB 84256-15/ 15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time*3	t_{WC}	100		120		150		ns
Address Valid to End of Write	t_{AW}	80		85		100		ns
Chip Select to End of Write	t_{CW}	80		85		100		ns
Data Valid to End of Write	t_{DW}	40		45		50		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Pulse Width	t_{WP}	60		70		90		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Recovery Time*4	t_{WR}	5		5		5		ns
$\overline{WE}$ to Output Low-Z*5*6	t_{WLZ}	5		5		5		ns
$\overline{WE}$ to Output High-Z*5*6	t_{WHZ}		40		40		50	ns

WRITE CYCLE TIMING DIAGRAM*1*2



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All write cycle are determined form last address transition to the first address transition of the next address.
*4 t_{WR} is defined from the end point of WRITE Mode.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is specified with Load II in Fig. 2.

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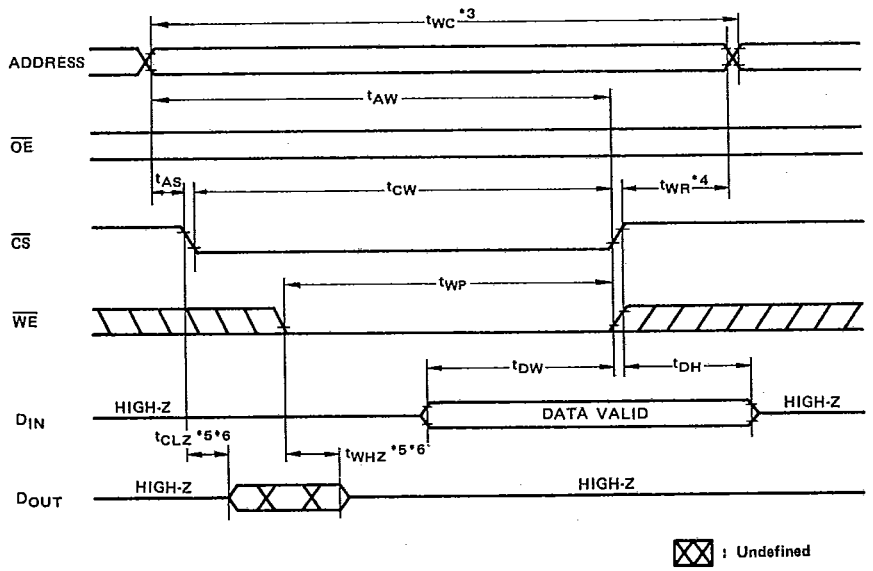
MB 84256-12/12L/12LL
MB 84256-15/15L/15LL

WRITE CYCLE II: $\overline{CS}$ CONTROLLED*1*2



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All write cycle are determined from last address transition to the first address transition of the next address.
*4 t_{WR} is defined from the end point of WRITE Mode.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is specified with Load II in Fig. 2.

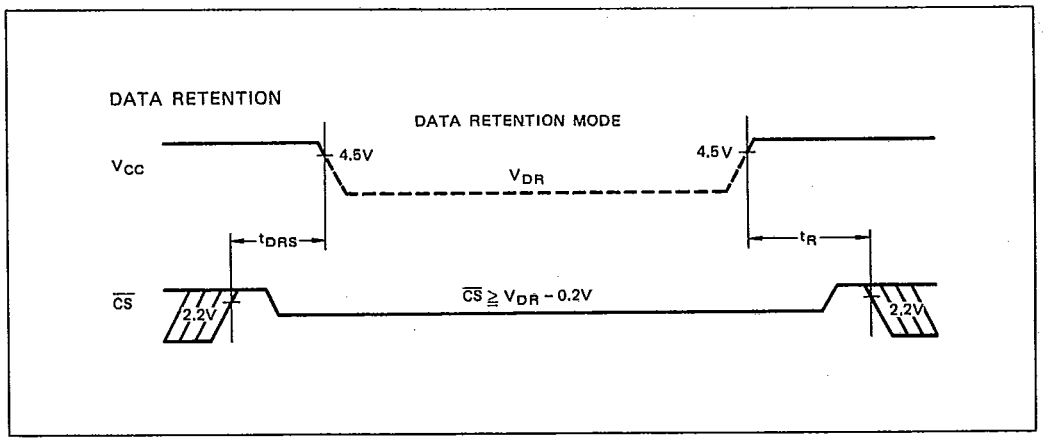
DATA RETENTION CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Data Retention Supply Voltage*1		V_{DR}	2.0	5.5	V
Data Retention*2 Supply Current	Standard	I_{DR}		1	mA
	L-Version			50	μA
	LL-Version*3			5	
Data Retention Setup Time		t_{DRS}	0		ns
Operation Recovery Time		t_R	t_{RC}		ns

Note: *1 $\overline{CS} \geqq V_{DR}-0.2V$
*2 $V_{DR} = 3.0V$, $\overline{CS} \geqq V_{DR}-0.2V$
*3 $V_{DR} = 3.0V$, $T_A = 40°C$

DATA RETENTION TIMING



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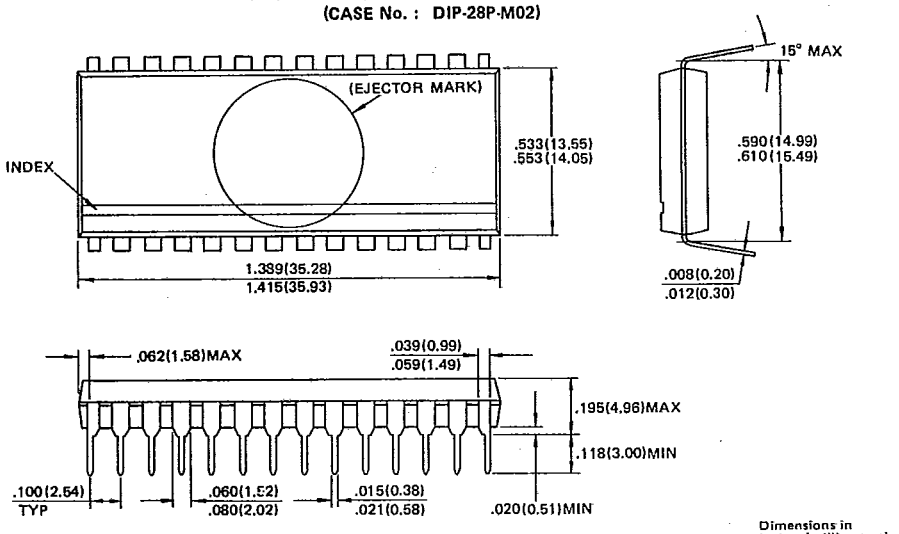
MB 84256-10/10L/10LL
MB 84256-12/12L/12LL
MB 84256-15/15L/15LL

PACKAGE DIMENSIONS

(Suffix: P)

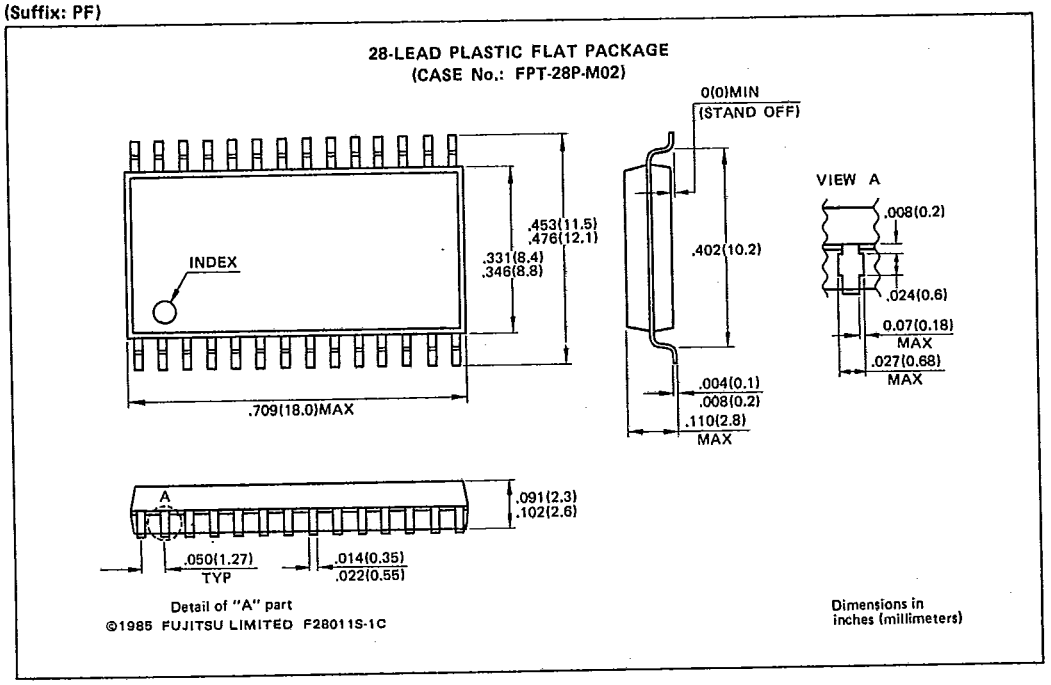
28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M02)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: PF)



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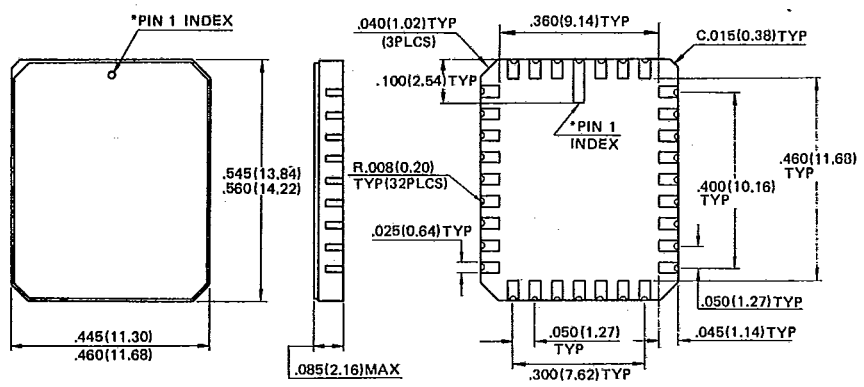
FUJITSU MB 84256-10/10L/10LL
MB 84256-12/12L/12LL
MB 84256-15/15L/15LL

PACKAGE DIMENSIONS

(Suffix: CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



Dimensions in inches
(millimeters)

*Shape of Pin 1 index : Subject to change without notice