SL2150F
Front end power splitter with AGC
Datasheet

DS5535 ISSUE 1.6 November 2001

Features
- Single chip quadruple power splitter (primary channel, secondary channel, OOB channel and loop through)
- Wide dynamic range on all channels
- Independent AGC facility incorporated into all channel paths
- CSO, CTB, CXM all better than -62dBc for +3dBmV agc attack point
- Full ESD protection. (Normal ESD handling procedures should be observed)

Applications
- Multi-tuner cable set top box and cable modem applications
- Data communications systems
- Terrestrial TV tuner loop though

Description
The SL2150F is a wide dynamic range single chip power splitter for cable set top box multi-tuner applications.

The device offers four buffered outputs from a single input.

All signal paths contain an independently controllable AGC facility.

Ordering Information
SL2150F/KG/LH2S (tubes)
SL2150F/KG/LH2T (tape and reel)

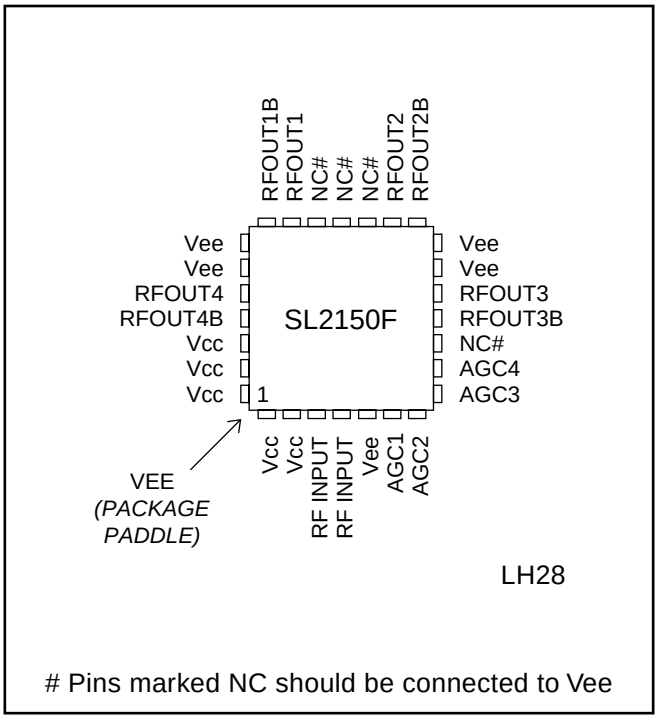


Figure 1 - Pin allocation

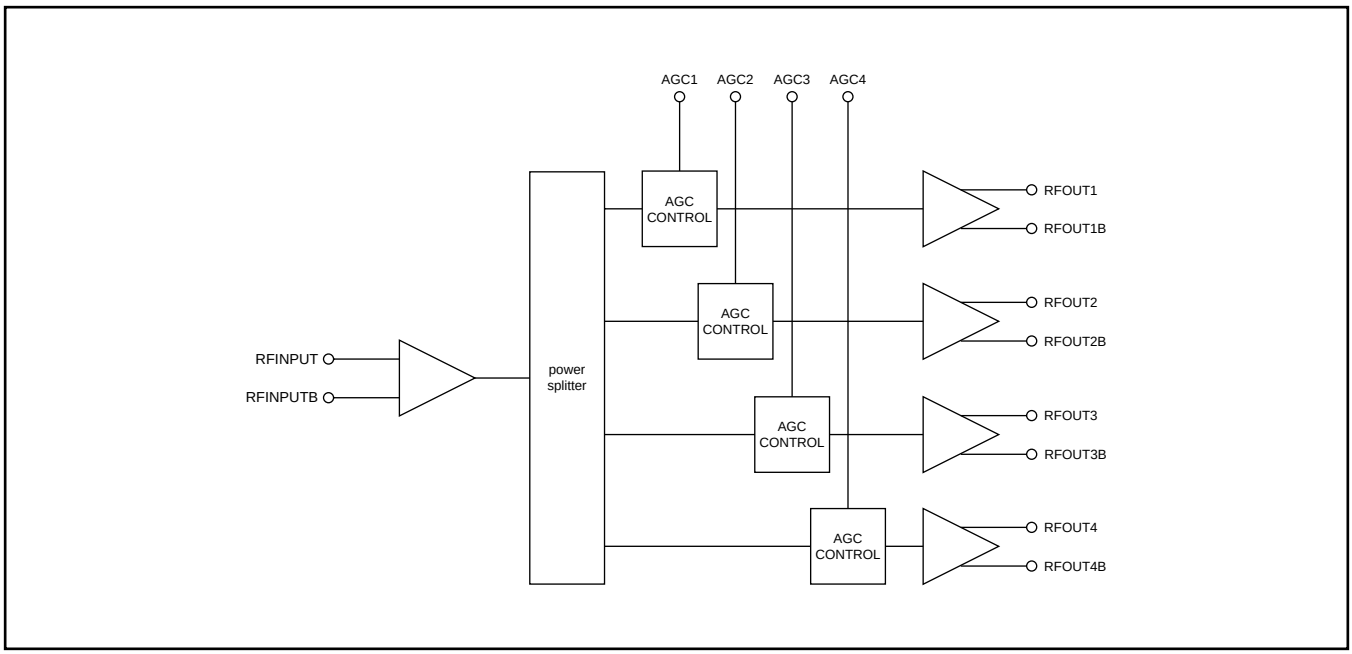


Figure 2 - SL2150F block diagram

Quick Reference Data

NB all data applies with differential termination and single ended source both of 75Ω

Characteristic		Units
RF input operating range	50-860	MHz
Conversion gain, with external load as in figure (12)		
maximum	5.5	dB
minimum	-25	dB
Input NF, all signal paths at maximum conversion gain	7	dB
IPIP3, all paths	127	dBµV
IPIP2, all paths	151	dBµV
CTB *	-66	dBc
CSO *	-64	dBc
CXM *	-66	dBc
Input impedance	75	Ω
Input VSWR	8	dB
Output impedance differential, all loops (requires external load for example as in figure (12)	440	Ω
Input to output isolation (all loops)	30	dB
Output to output isolation (all loops)	25	dB

* 132 channel matrix at +15 dBmV per channel, 75Ω source impedance, all paths, max gain

Functional Description

The SL2150F is a broadband wide dynamic range power splitter with AGC and is optimised for application in multi tuner cable set top box applications. It also has application in any system where a wide dynamic range broadband power splitter is required.

The pin assignment is contained in figure (1) and the block diagram in figure (2). The port internal peripheral circuits are contained in figure (14)

In normal application the RF input is interfaced to the device input. The input preamplifier is designed for low noise figure, within the operating region of 50 to 860 MHz and for high intermodulation distortion intercept so offering good signal to noise plus composite distortion spurious performance when loaded with a multi carrier system. The preamplifier when combined with the input network shown in figure (3) provides an impedance match to a 75Ω source. The typical impedance is shown in figure (4).

The input NF and input referred two-tone intermodulation test condition spectrum are shown in figures (5) and (6) respectively.

The output of the preamplifier is then power split to four independently controlled AGC stages.

Each AGC stage provides for a minimum of 30 dB of gain control across the input frequency range. The typical AGC characteristic and NF versus gain setting are contained in figures (7) and (8) respectively.

The input referred third order intercept point is independent of gain setting.

Finally each of the AGC stages drive an output buffer of nominal differential output impedance of 440Ω, which provides a nominal 5.5 dB of conversion gain when terminated into a differential 75Ω load.

In application it is important to avoid saturation of the output stage, therefore it is recommended that the output standing current be sunk to Vcc through an inductor. A resistive pull up can also be used as shown in figure (13b), however the resistor values should not exceed 38 ohm single ended.

If an inductive current sink is used the maximum available gain from the device is circa 20 dB. This gain can be reduced by application of an external load between the differential output ports. The gain can be approximately calculated from the following formula;

GAIN = 20*log ((Parallel combination of 440 ohm and external load between ports) / 44 ohm) + 2dB

For example when driving a 200 ohm load as in figure (13a), the gain equals;

Gain = 20 *log ((440 * 200)/(440+200)/44) +2dB
= 12dB

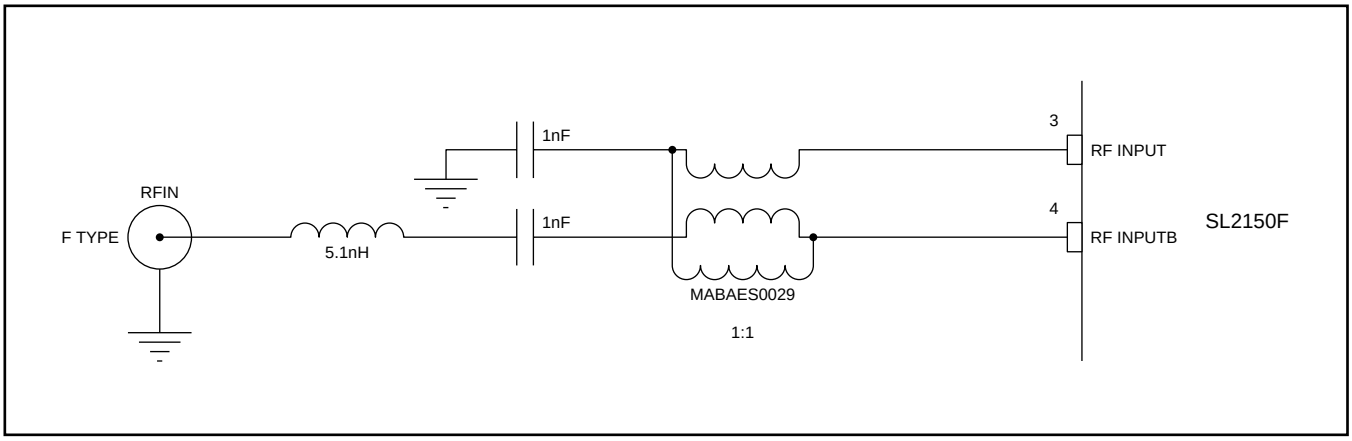


Figure 3 - RF input matching network

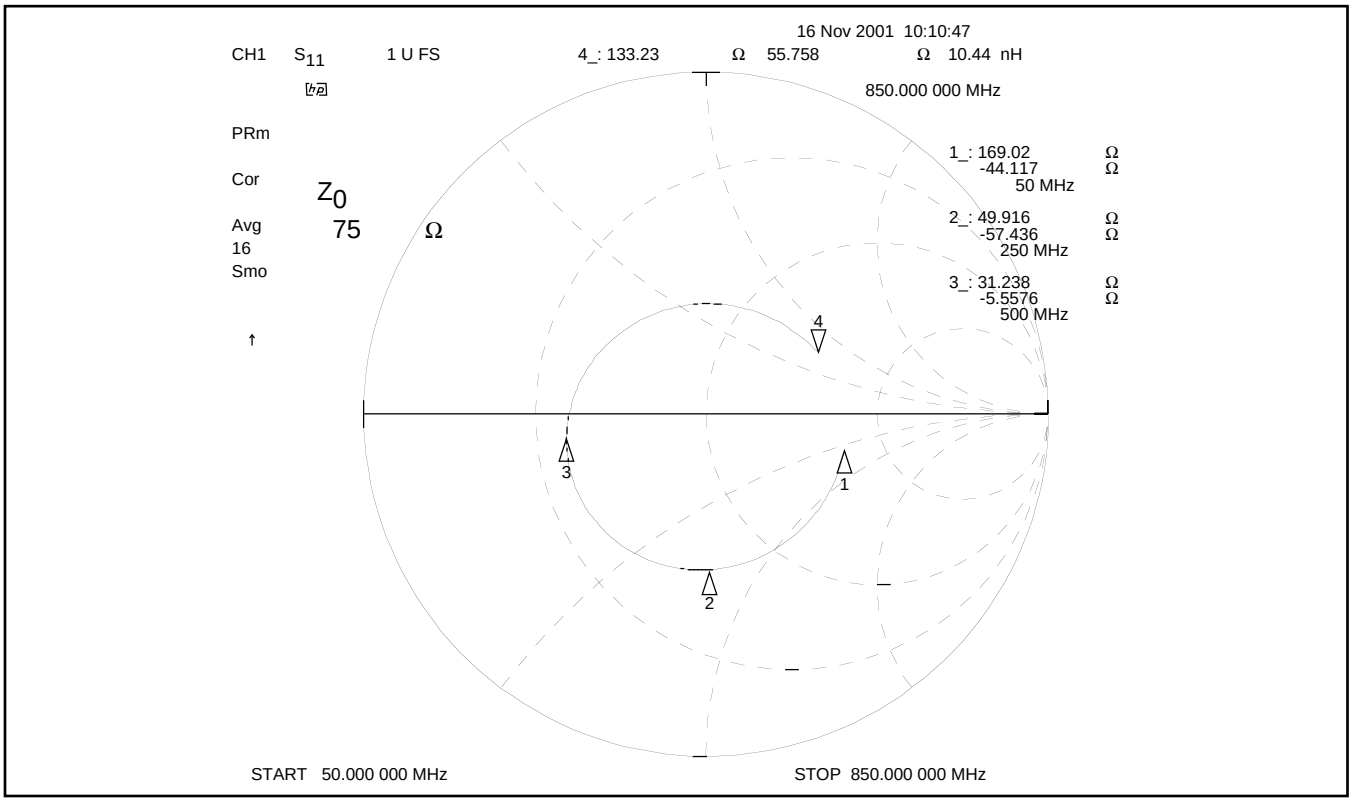


Figure 4 - Typical single-ended RF input impedance with input match

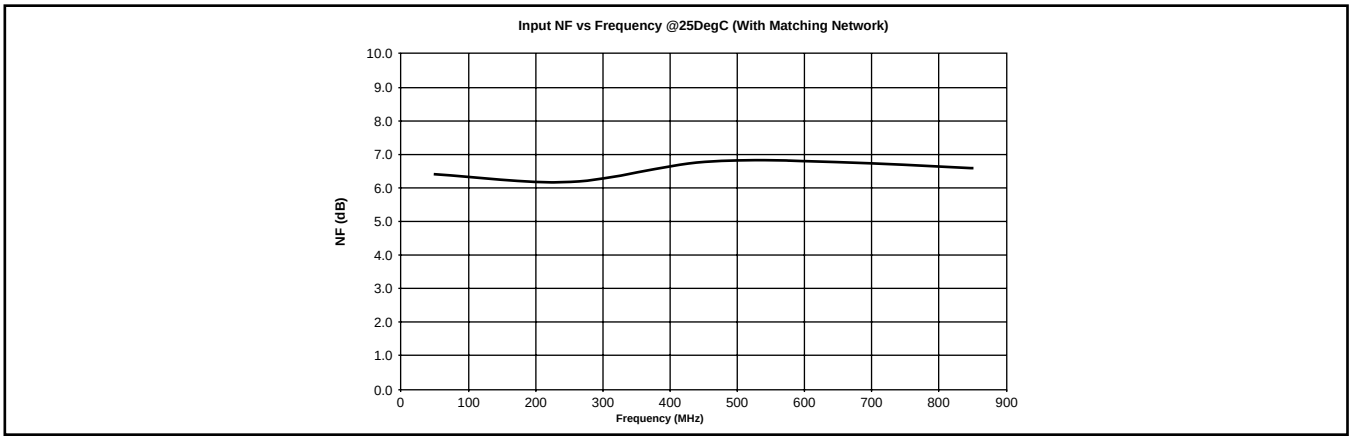


Figure 5 - Input NF at 25 deg C

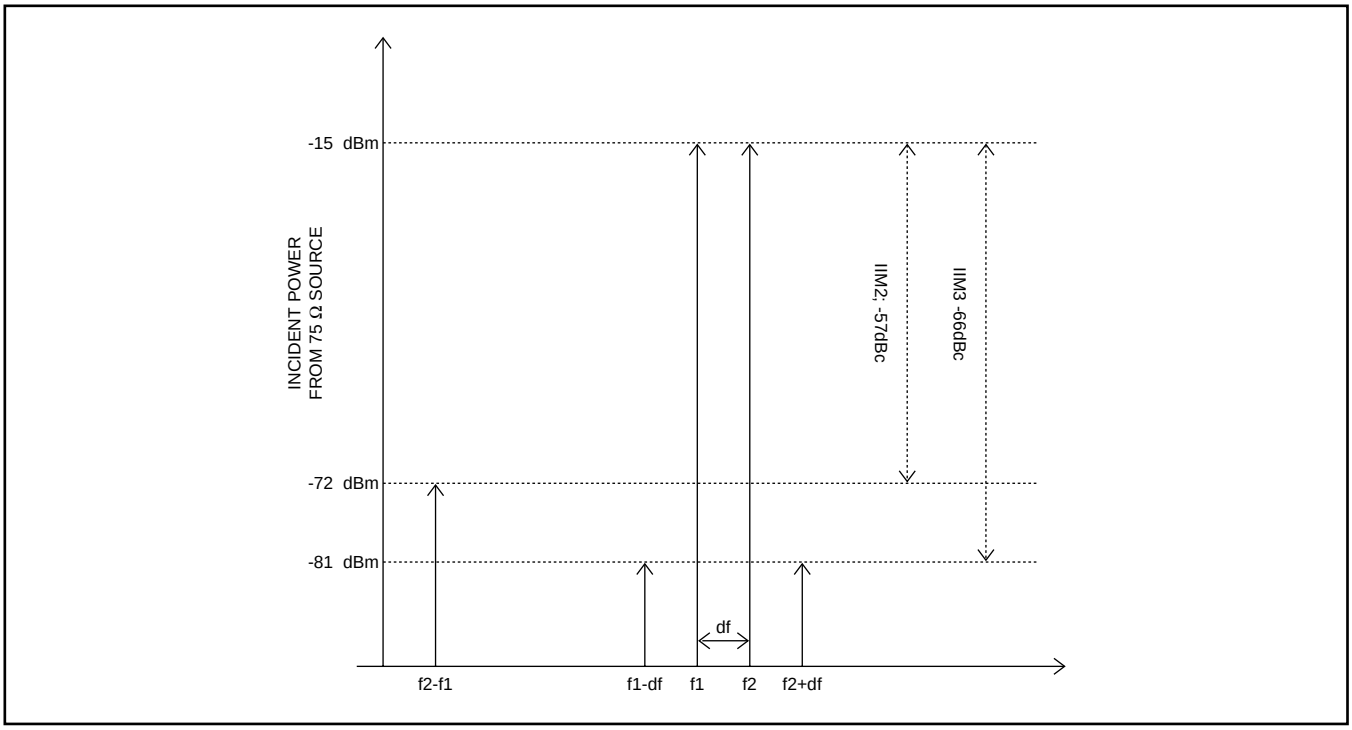


Figure 6 - Two tone intermodulation test condition spectrum, input referred

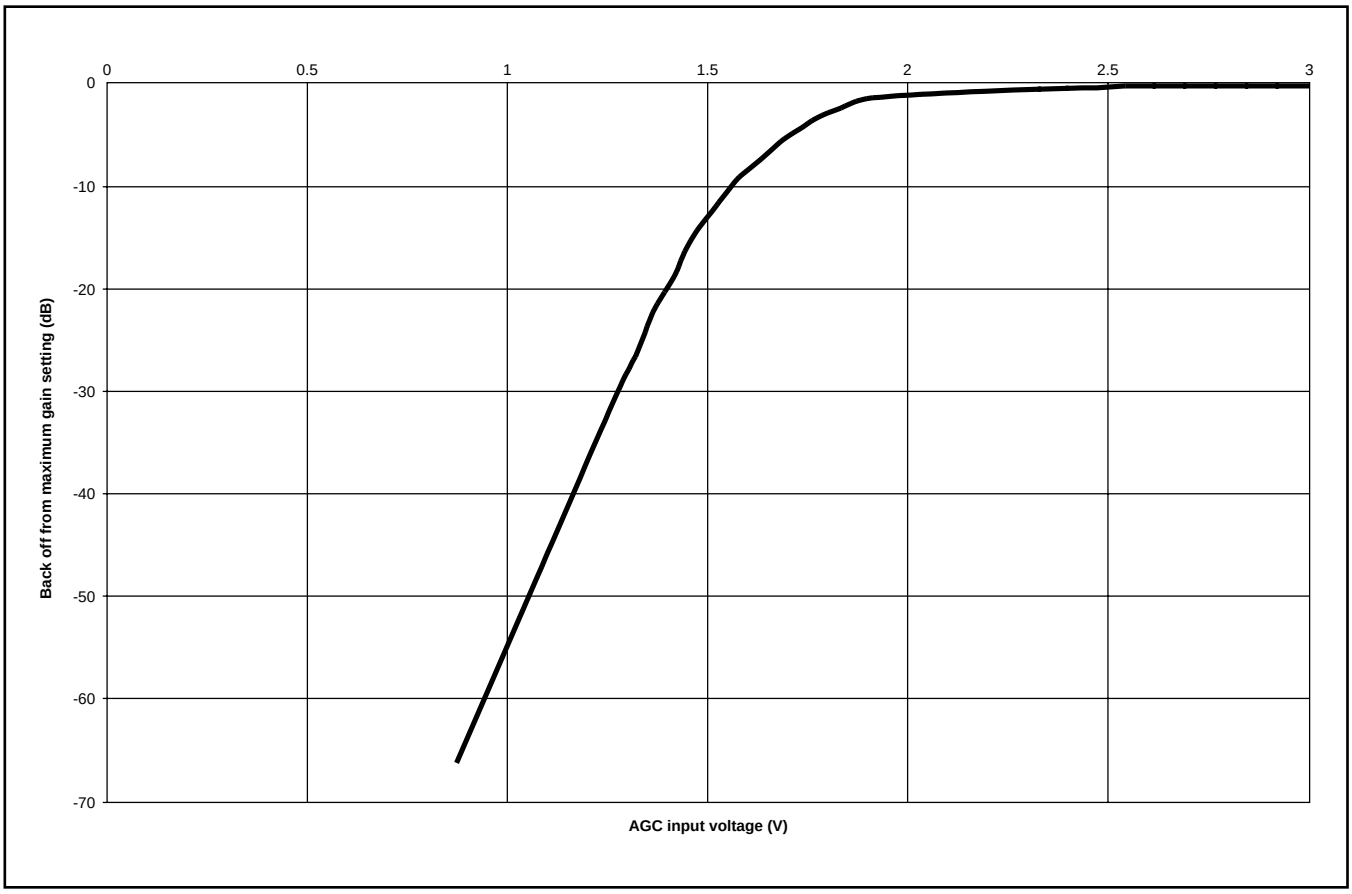


Figure 7 - Typical AGC versus control voltage characteristic

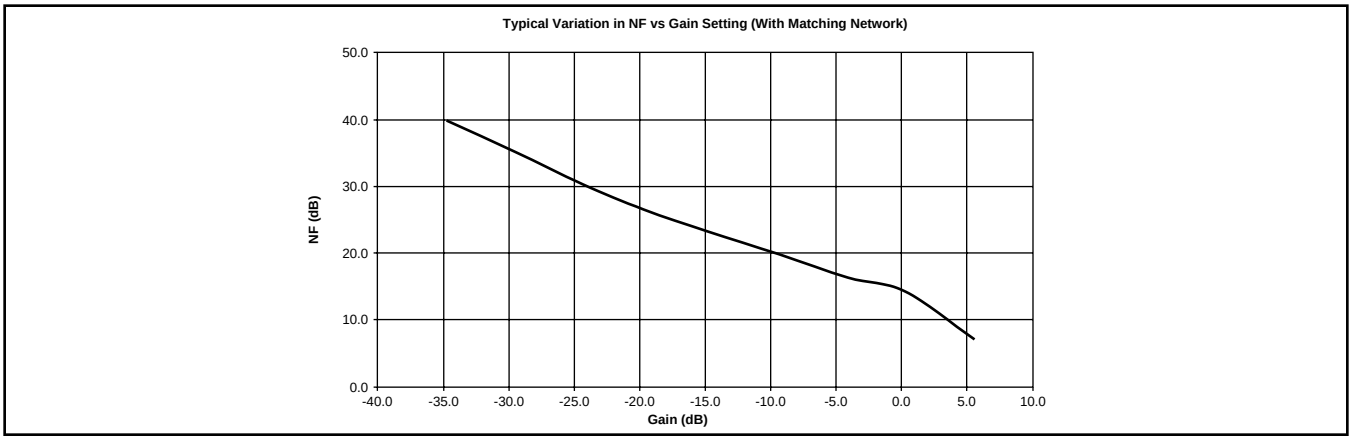


Figure 8 - Typical variation in NF versus gain setting

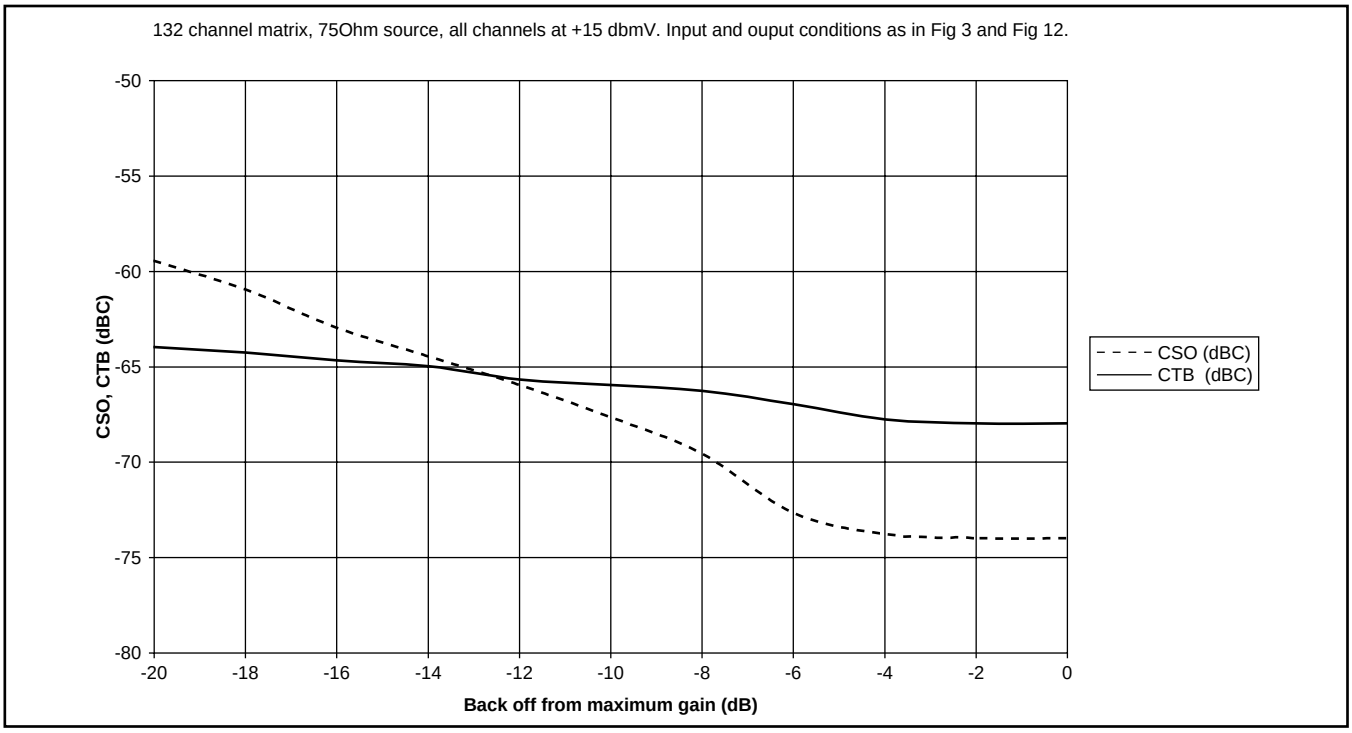


Figure 9 - Typical variation in CSO and CTB versus back off from maximum gain

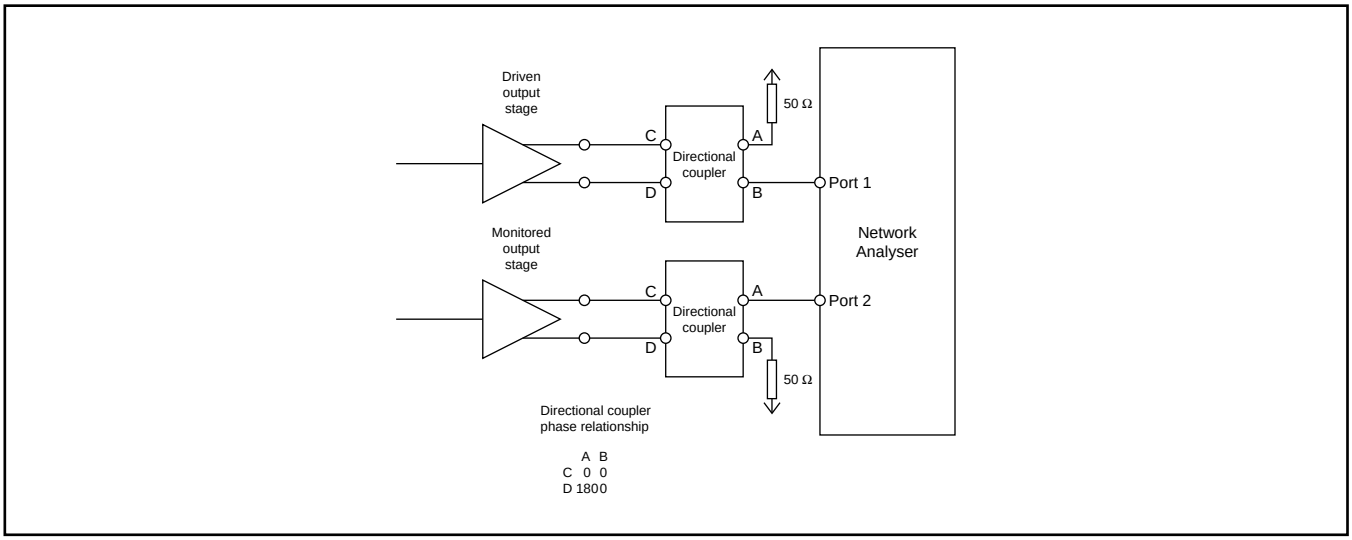


Figure 10 - Test condition for output crosstalk

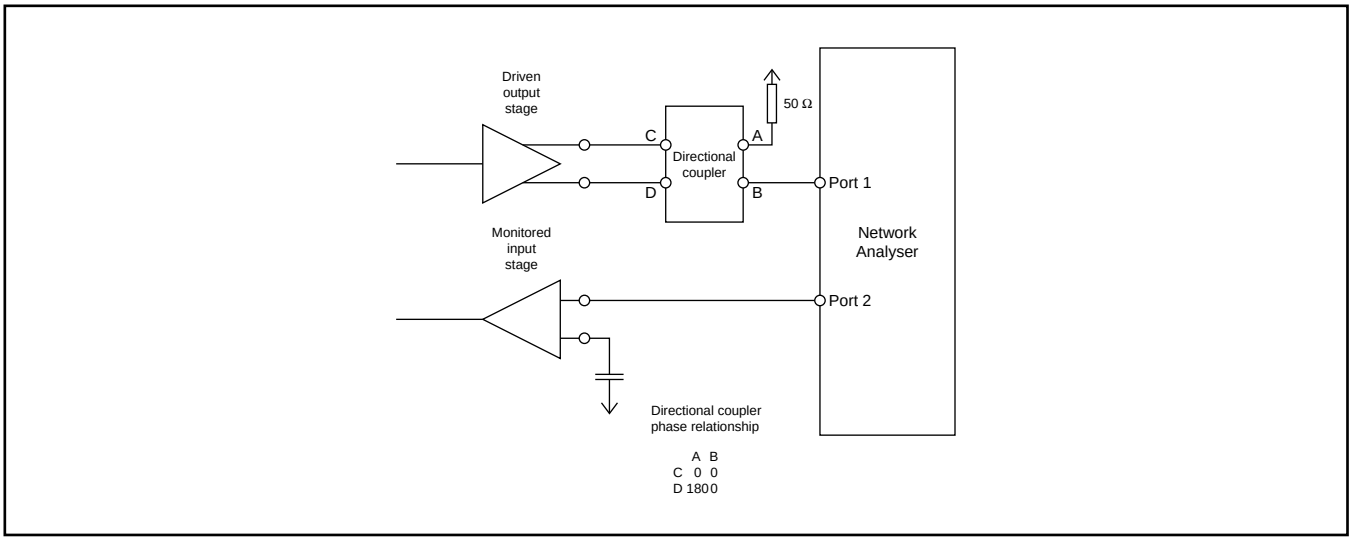


Figure 11 - Test condition for output to input crosstalk

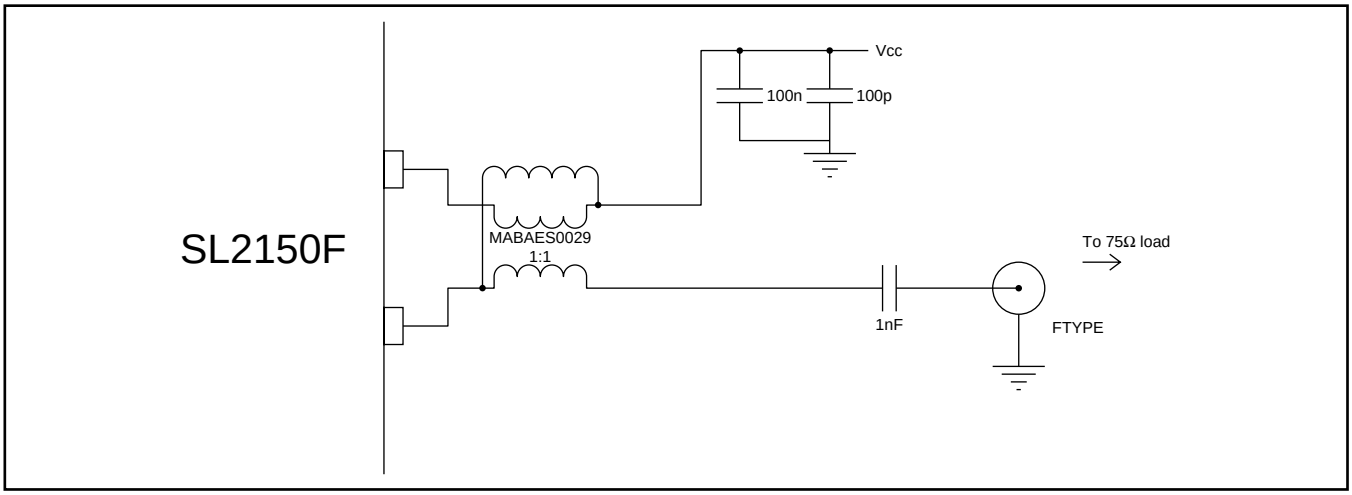


Figure 12 - Example application driving 75Ω load

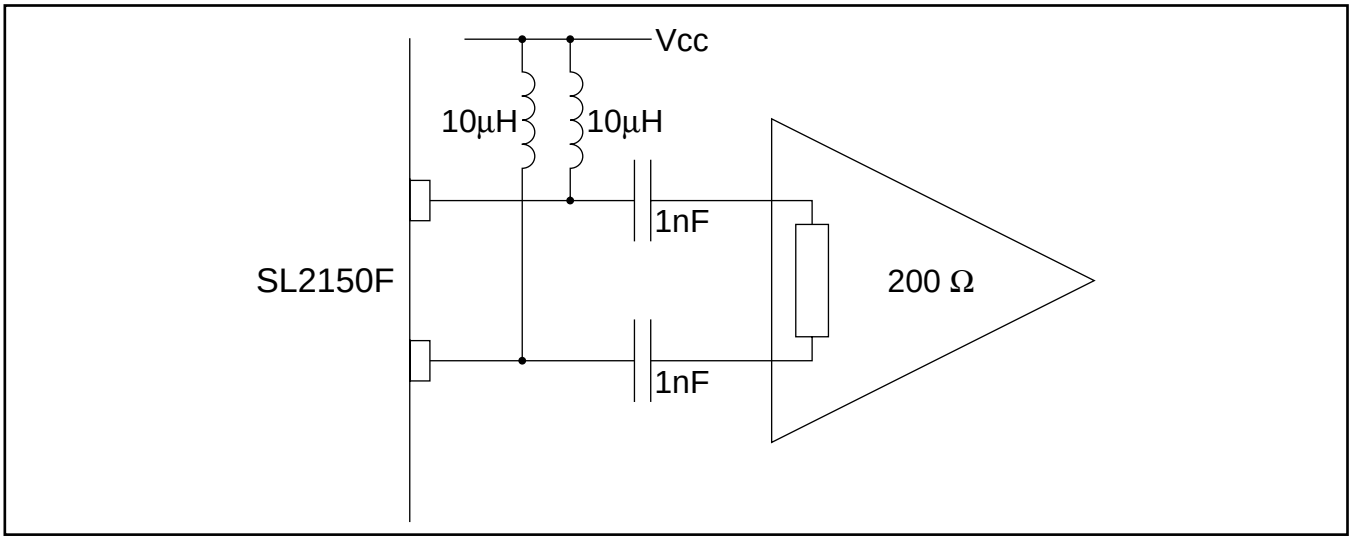


Figure 13a - Example application driving 200Ω load with inductive pull up

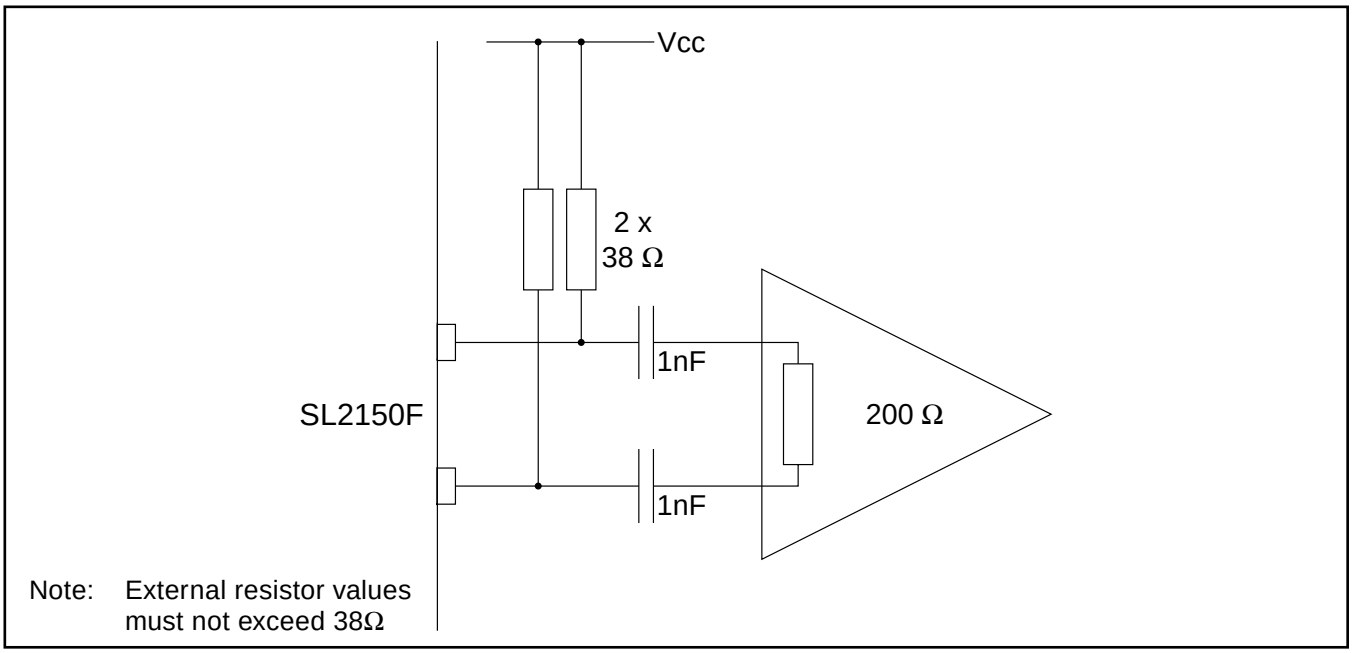


Figure 13b - Example application driving 200Ω load with resistive pull up

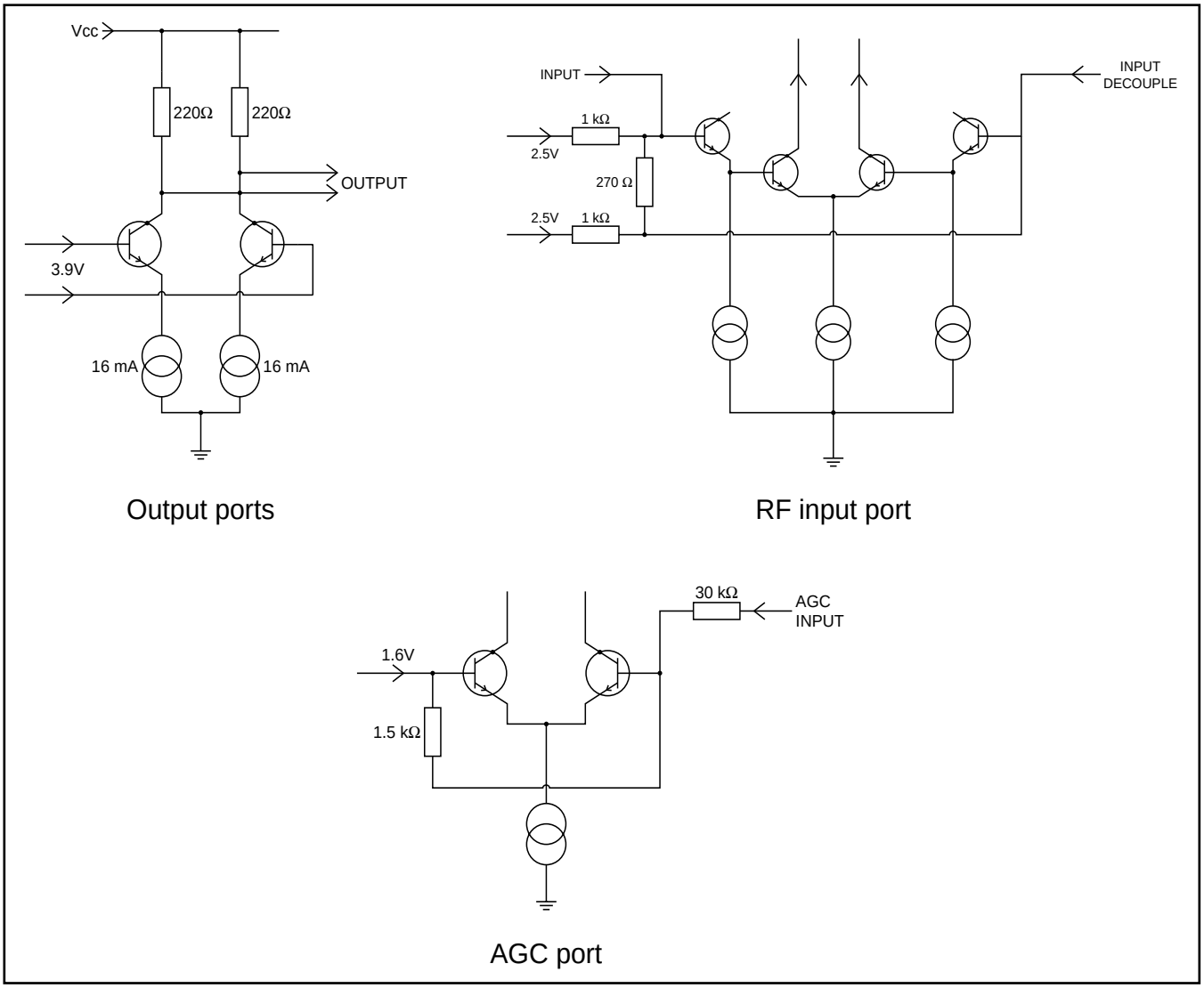


Figure 14 - Port peripheral circuitry

Electrical Characteristics

Test conditions (unless otherwise stated)

Tamb = -40˚ to 85˚C, Vee= 0V, Vcc=5V+-5%

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	pin	min	typ	max	units	Conditions
Supply current			190	228	mA	
Input frequency range		50		860	MHz	
Input impedance	3,4		75		Ω	See figure (4)
Input return loss			8		dB	
Input Noise Figure				8	dB	Tamb=27˚C, see figure (5) All loops at maximum conversion gain
Variation in NF with gain adjust				-1	dB/dB	See figure (8)
Gain						Power gain from 75Ω single ended source to differential 75Ω load
maximum		4	5.5	7	dB	Vagcip=3.0V
minimum				-25	dB	Vagcip=0.5V
minimum			-65		dB	Vagcip=Vee
						AGC monotonic from Vee to Vcc
						Refer to 'Functional description' section for information on calculating maximum gain with other load conditions
Input referred IP2		42			dBm	Assuming ideal power match. See note (2) and figure (6)
Input referred IP3		18			dBm	Assuming ideal power match. See note (2) and figure (6)
Input referred IM2				-57	dBc	See note (2) and figure (6)
				-37	dBc	See note (3) and figure (6)
Input referred IM3				-66	dBc	See note (2) and figure (6)
				-46	dBc	See note (3) and figure (6) All gain settings
CSO				-62	dBc	See note (4) and figure (9)
CTB				-64	dBc	See note (4)
CXM				-64	dBc	See note (4)

Characteristic	pin	min	typ	max	units	Conditions
Input P1dB			+9		dBm	All gain settings, with load as in figure (12)
Gain variation within channel			0.25		dB	Channel bandwidth 8 MHz within operating frequency range, all loops, all gain settings
Output impedance	11,12 15,16 20,21 24,25		440		Ω	Differential
Output port DC standing current	11,12 15,16 20,21 24,25			25	mA	Standing current that any external load has to sustain
AGC input leakage current	6,7 8,9	-150		150	µA	Vagcip = Vee to Vcc, all control inputs
Crosstalk between all loop outputs				-25	dB	All gain settings, measured differential output to differential output, driven ports in phase and monitored ports out of phase, see figure (10)
Crosstalk between all loop outputs and RF input				-30	dB	All gain settings, measured differential output to single ended input, driven ports in phase, see figure (11)

Notes

(1) All power levels are referred to 75Ω and 0 dBm = 109 dBµV

(2) Any two tones within RF operating range at -15 dBm, from single-ended 75 ohm source into differential 75Ω load as in figure (12), gain setting between maximum and -15dB backoff.

(3) Any two tones within RF operating range at -5 dBm, from single-ended 75 ohm source into differential 75Ω load as in figure (12)

(4) Load as in figures (12) & (13), max gain, 132 channel matrix, 75 ohm source with all channels at +15 dBmV, assuming power match

Absolute Maximum Ratings

All voltages are referred to Vee at 0V

Characteristic	min	max	units	conditions
Supply voltage	-0.3	6	V	
RF input voltage		8	dBm	Differential
All I/O port DC offsets	-0.3	Vcc+0.3	V	
Storage temperature	-55	150	˚C	
Junction temperature		125	˚C	Power applied
Package thermal resistance, chip to ambient		35	˚C/W	Paddle to be soldered to ground plane
Power consumption at 5.25V		1200	mW	
ESD protection	1.5		kV	Mil-std 883B method 3015 cat1

Evaluation Board

Figures 15 and 16 show schematic and PCB layout for a 4 layer evaluation board.

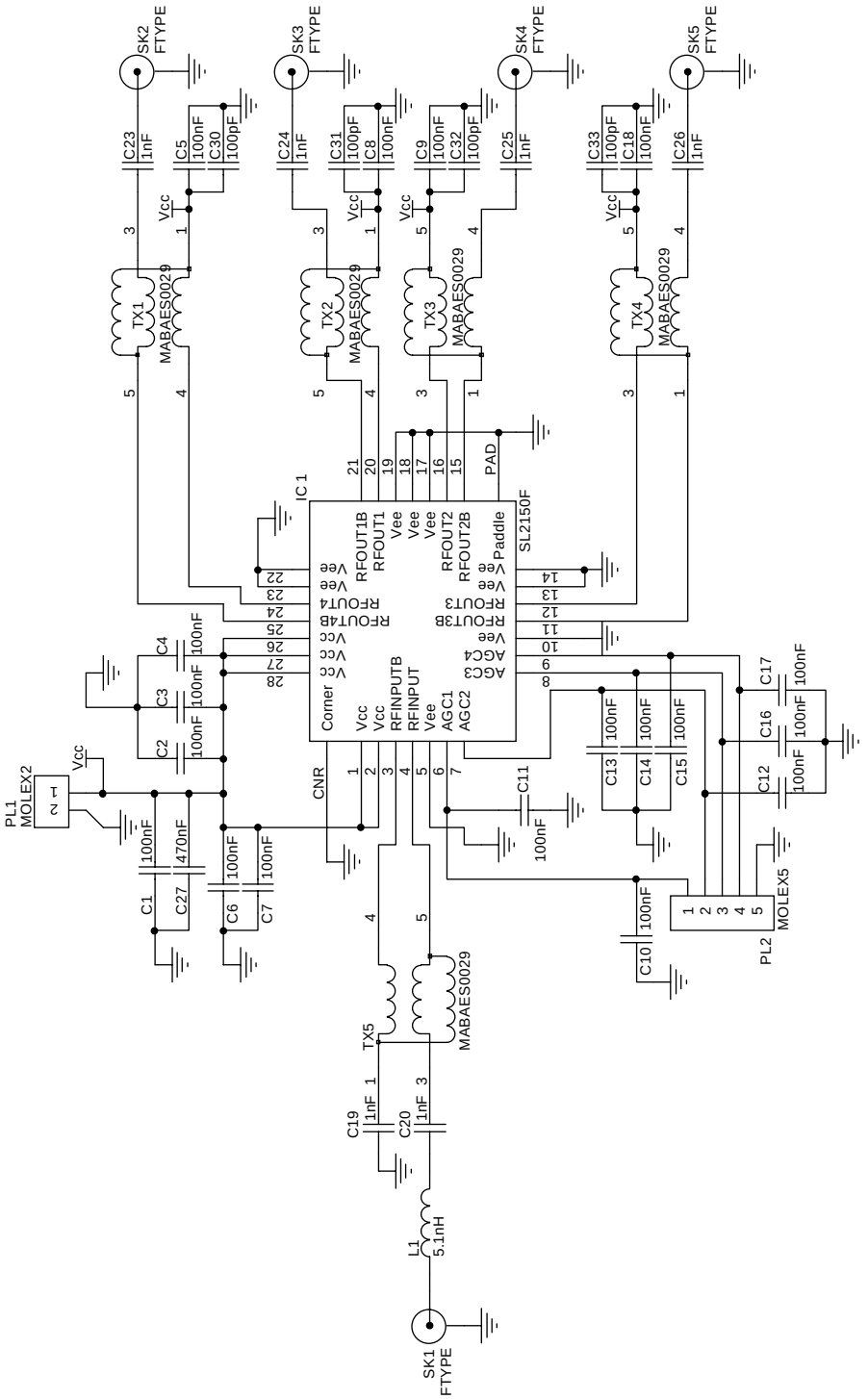
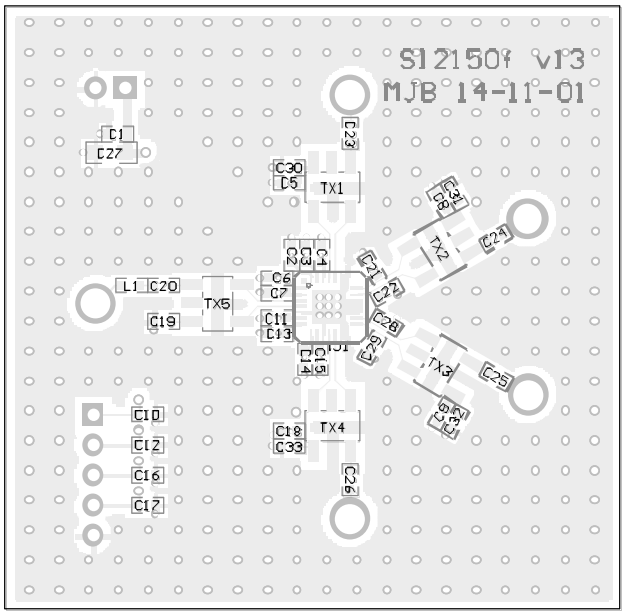
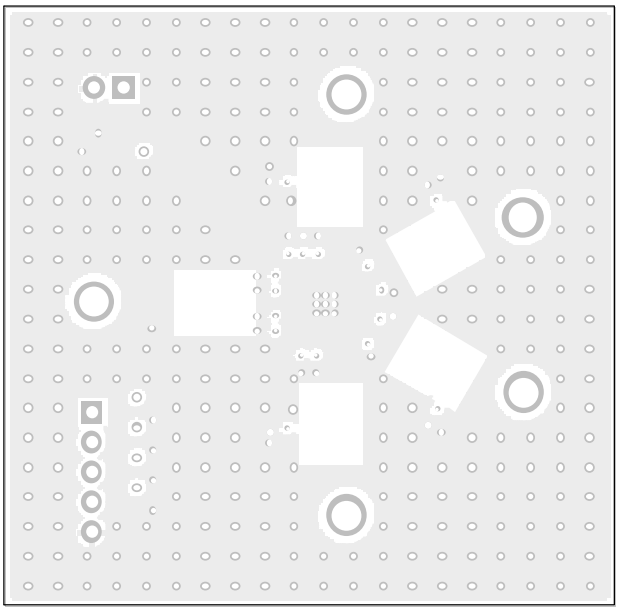


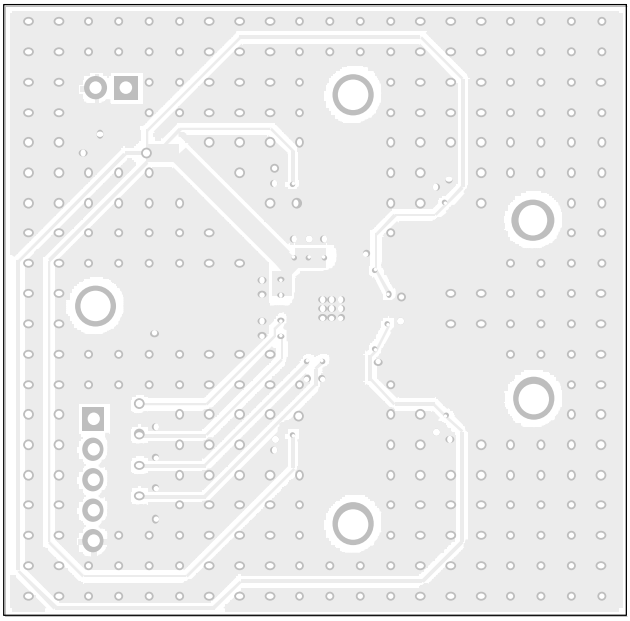
Figure 15 - SL2150F evaluation PCB Schematic



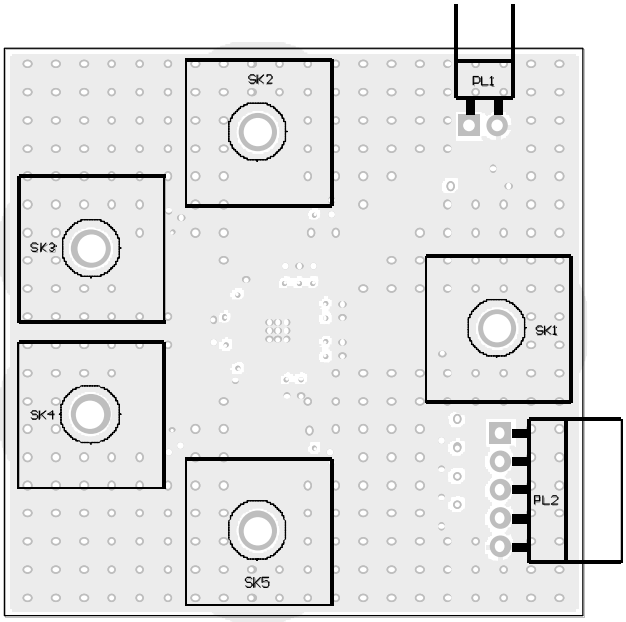
Top view



Layer2 view

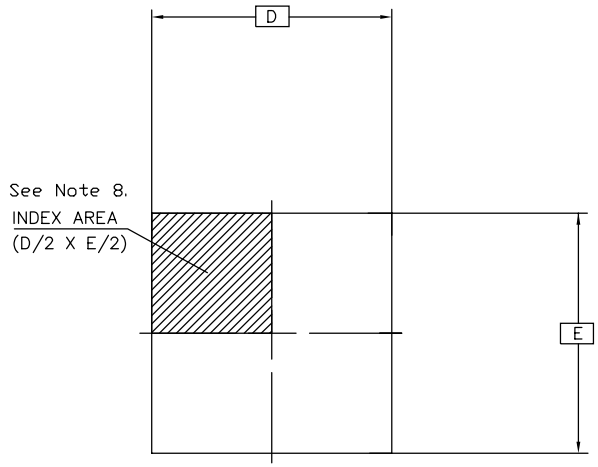


Layer3 view

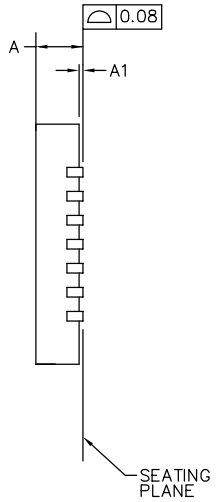


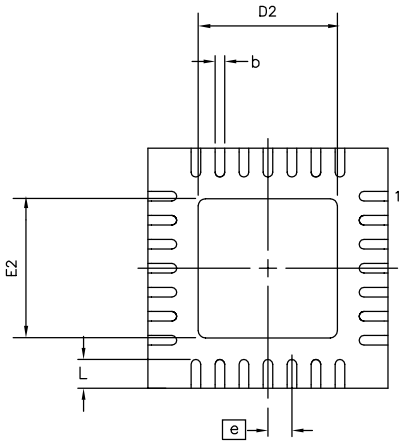
Bottom view mirrored

Figure 16 - SL2150F evaluation PCB layout



TOP VIEW





BOTTOM VIEW

SYMBOL	COMMON DIMENSIONS	
	MIN.	MAX.
A	–	1.00
A1	0.00	0.05
b	0.18	0.30
D	5.00 BSC	
D2	3.00	3.25
E	5.00 BSC	
E2	3.00	3.25
N	28	
Nd	7	
Ne	7	
e	0.50 BSC	
L	0.35	0.75

Conforms to JEDEC MO–220 VHHD–1 iss A

NOTES:
1. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd & Ne ARE THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED
   BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. ALL DIMENSIONS ARE IN MILLIMETERS.
5. LEAD COUNT IS 28 .
6. PACKAGE WARPAGE MAX 0.08mm.
7. NOT TO SCALE.
8. TERMINAL #1 IDENTIFIER MUST BE LOCATED WITHIN THE ZONE INDICATED AND MAY BE EITHER A MOULD OR MARKED FEATURE.

ISSUE	1				
ACN	209757				
DATE	26OCT00				
APPRD.					

ORIGINATING SITE: Swindon

Title: Package Outline For
28 Lead MLP (5 x 5 x 0.9)mm(LH)

Drawing Number
GPD00747

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