TOSHIBA INSULATED GATE BIPOLAR TRANSISTOR SILICON N CHANNEL IGBT

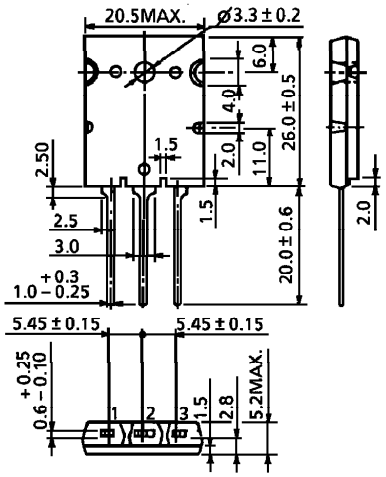
GT50J301

HIGH POWER SWITCHING APPLICATIONS

MOTOR CONTROL APPLICATIONS

- The 3rd Generation
- Enhancement-Mode
- High Speed : $t_f = 0.30\,\mu s$ (Max.)
- Low Saturation Voltage : $V_{CE\,(sat)} = 2.7V$ (Max.)
- FRD Induded Between Emitter and Collector

Unit in mm



1. GATE
2. COLLECTOR (HEAT SINK)
3. EMITTER

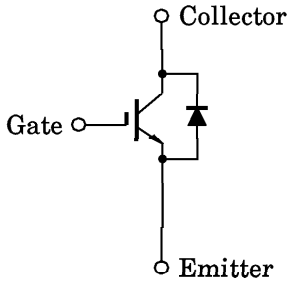
JEDEC	—
EIAJ	—
TOSHIBA	2-21F2C

Weight : 9.75g

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Collector-Emitter Voltage		V_{CES}	600	V
Gate-Emitter Voltage		V_{GES}	±20	V
Collector Current	DC	I_C	50	A
	1ms	I_{CP}	100	
Forward Current	DC	I_F	50	A
	1ms	I_{FM}	100	
Collector Power Dissipation (Tc = 25°C)		P_C	200	W
Junction Temperature		T_j	150	°C
Storage Temperature		T_{stg}	−55~150	°C
Screw Torque		—	0.8	N·m

EQUIVALENT CIRCUIT



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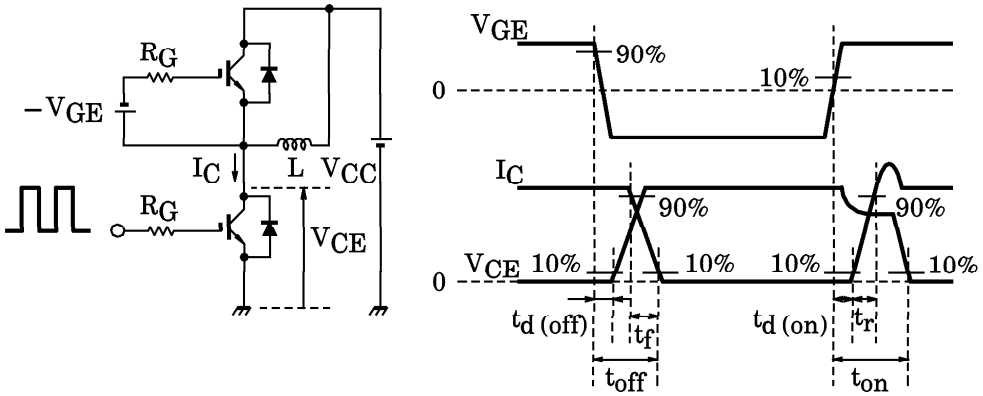
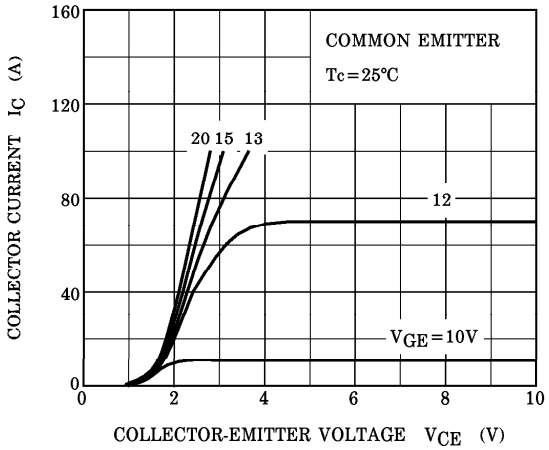
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GES}	$V_{GE} = \pm 20V$, $V_{CE} = 0$	—	—	±500	nA
Collector Cut-off Current		I_{CES}	$V_{CE} = 600V$, $V_{GE} = 0$	—	—	1.0	mA
Gate-Emitter Cut-off Voltage		$V_{GE\ (OFF)}$	$I_C = 5mA$, $V_{CE} = 5V$	5.0	7.0	8.0	V
Collector-Emitter Saturation Voltage		$V_{CE\ (sat)}$	$I_C = 50A$, $V_{GE} = 15V$	—	2.1	2.7	V
Input Capacitance		C_{ies}	$V_{CE} = 10V$, $V_{GE} = 0$ f = 1MHz	—	4500	—	pF
Switching Time	Turn-on delay Time	$t_{d\ (on)}$	Inductive Load $V_{CC} = 300V$ $V_{GE} = \pm 15V$ $I_C = 50A$ $R_G = 24\Omega$ (Note 1)	—	0.08	—	μs
	Rise Time	t_r		—	0.12	—	
	Turn-on Time	t_{on}		—	0.40	—	
	Turn-off delay Time	$t_{d\ (off)}$		—	0.20	—	
	Fall Time	t_f		—	0.15	0.30	
	Turn-off Time	t_{off}		—	0.50	—	
Forward Voltage		V_F	$I_F = 50A$, $V_{GE} = 0$	—	2.4	3.5	V
Reverse Recovery Time		t_{rr}	$I_F = 50A$, $V_{GE} = 10V$ di / dt = 100A / us	—	0.1	0.2	μs
Thermal Resistance		$R_{th\ (j\text{-}c)}$	IGBT	—	—	0.625	°C / W
Thermal Resistance		$R_{th\ (j\text{-}c)}$	DIODE	—	—	2.50	°C / W

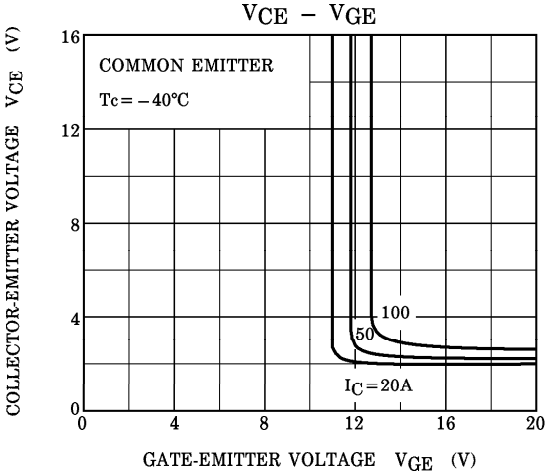
Note 1 Switching time measurement circuit and input / output waveforms



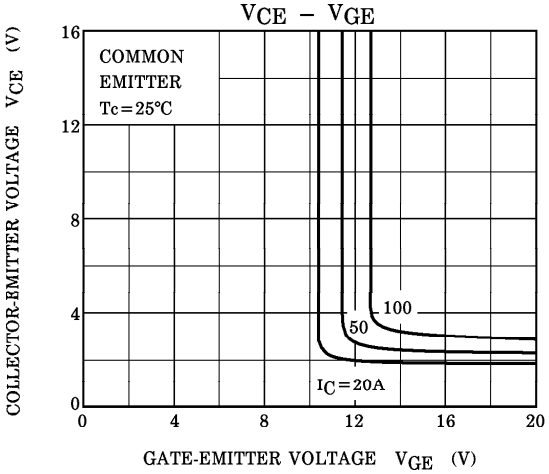
I_C – V_{CE}



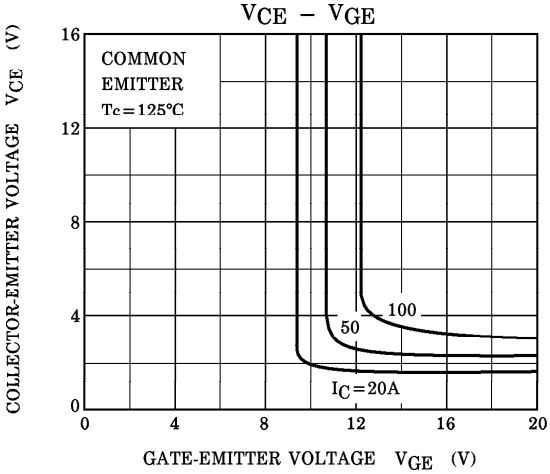
V_{CE} – V_{GE}



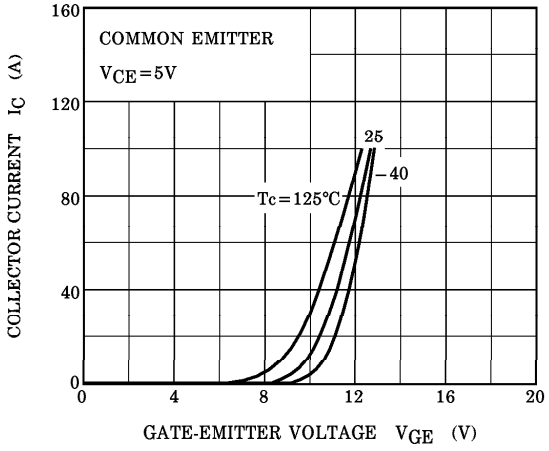
V_{CE} – V_{GE}



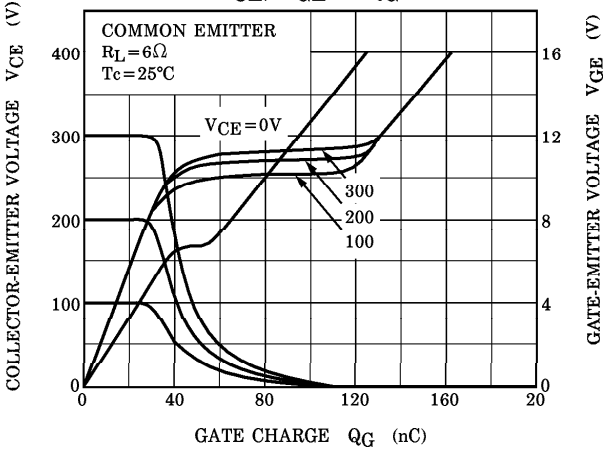
V_{CE} – V_{GE}



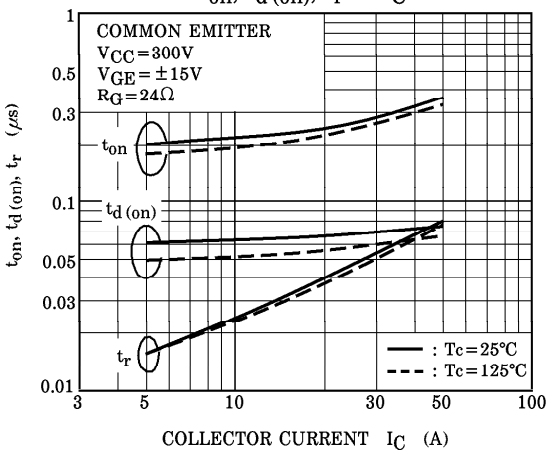
I_C – V_{GE}



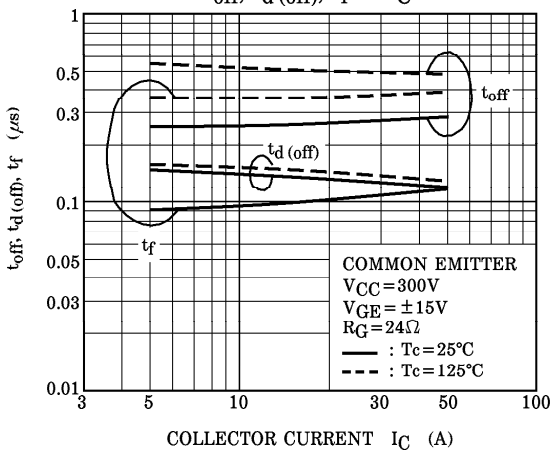
V_{CE}, V_{GE} – Q_G



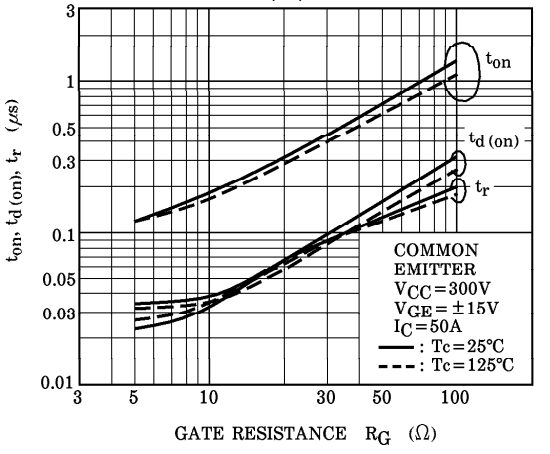
t_{on}, $t_{d\,(on)}$, t_r – I_C



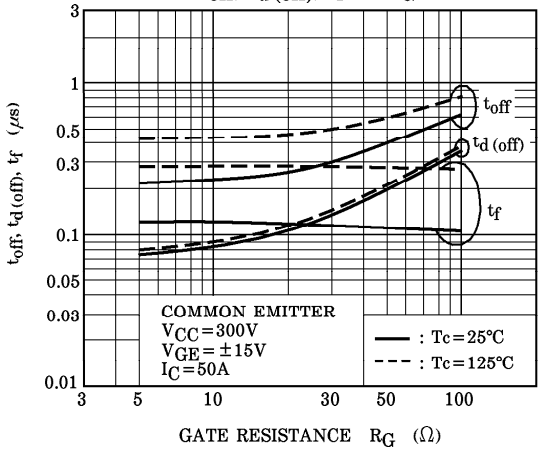
t_{off}, $t_{d\,(off)}$, t_f – I_C



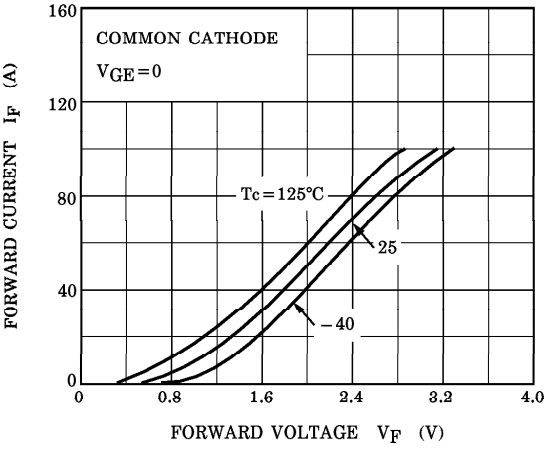
t_{on}, $t_{d\,(on)}$, t_r – R_G



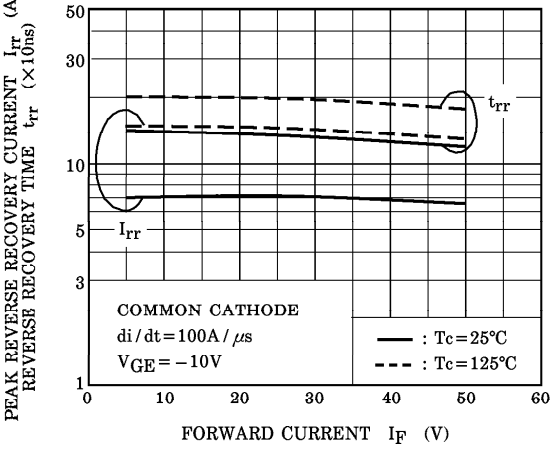
t_{off}, $t_{d\,(off)}$, t_f – R_G



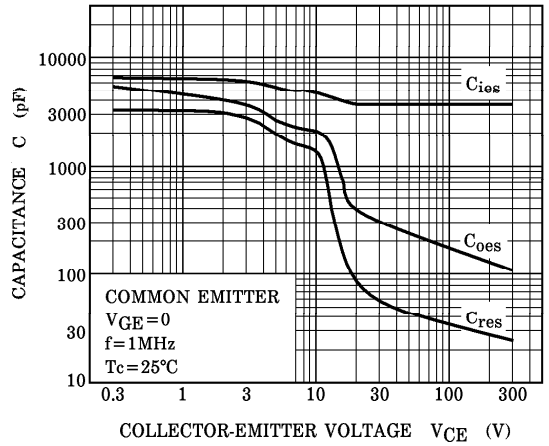
I_F – V_F



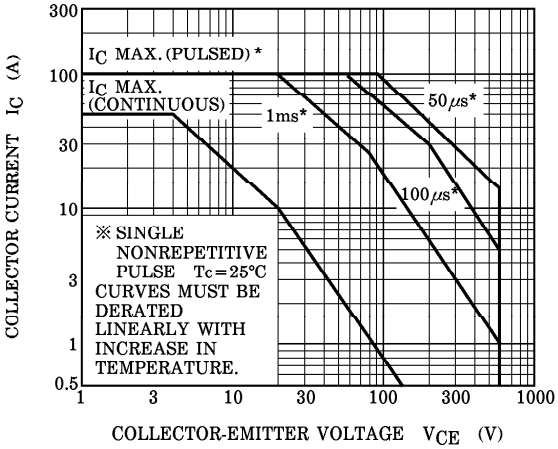
t_{rr}, I_{rr} – I_F



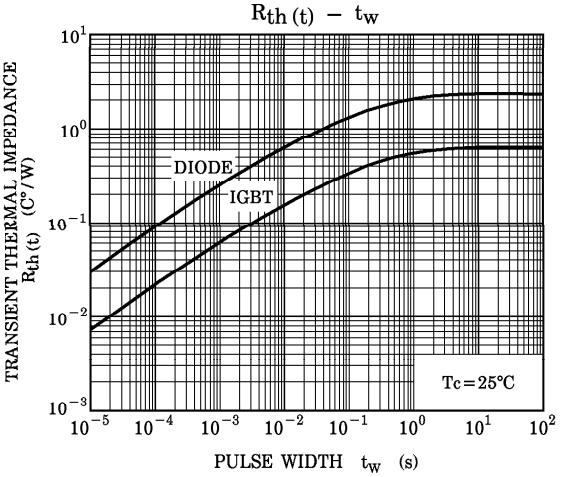
C – V_{CE}



SAFE OPERATING AREA



R_{th} (t) – t_w



REVERSE BIAS SOA