NEC

# BIPOLAR ANALOG INTEGRATED CIRCUIT

# μPC1862

## BURST LOCK CLOCK GENERATOR

The μPC1862 is an LSI incorporating a PLL circuit to generate $nf_{SC}$ clocks ($f_{SC}$: color subcarrier frequency), ideal for the processing of digital video signals as in extended definition television (EDTV) systems.

### FEATURES

- VCO is incorporated.
- Horizontal and vertical sync separation circuits are incorporated (with output pins).
- Horizontal and vertical sync output pulses (TTL level)
- ACC amplifier and killer detector circuits are incorporated.
- 1/4 and 1/8 (1/2 × 1/4) frequency dividers are incorporated.
- $f_{SC}$ phase control circuits is incorporated.
- Applicable to both NTSC and PAL systems.
- Possible to input burst gate pulse from external

### ★ ORDERING INFORMATION

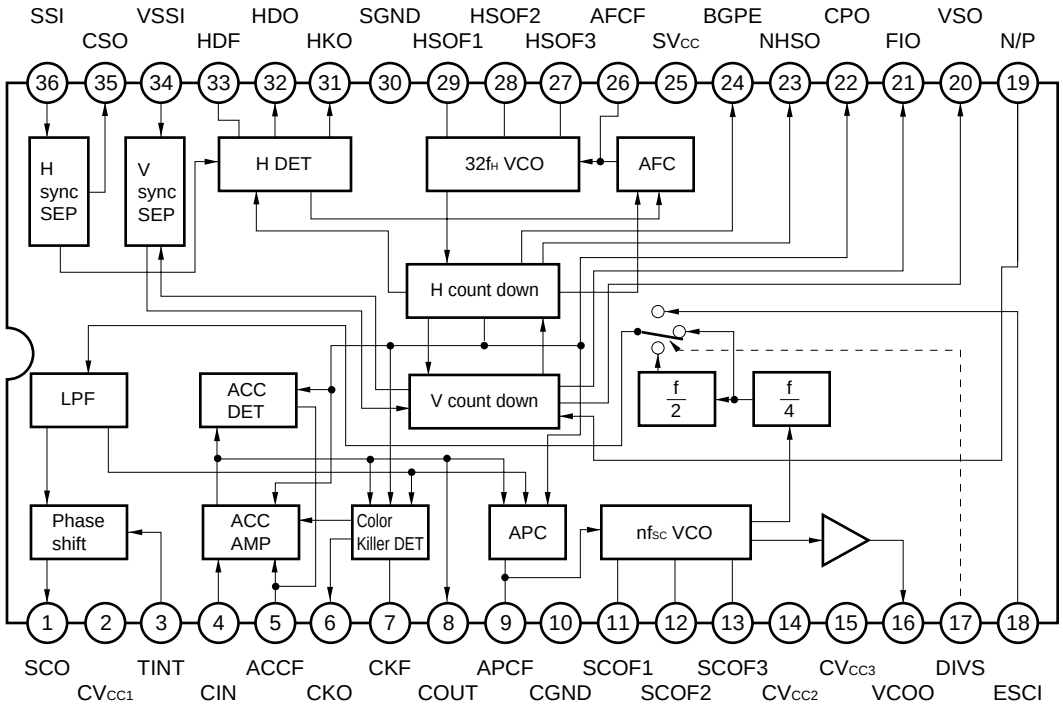
| Part number | Package |
|---|---|
| μPC1862GS | 36-pin plastic shrink SOP (300 mil) |



Document No. S11431EJ3V0DS00 (3rd edition)
Date Published December 1997 N CP(K)
Printed in Japan

**The mark ★ shows major revised points.**

## BLOCK DIAGRAM




**Remark** AFC : Automatic Frequency Control
ACC : Automatic Color saturation level Control
APC : Automatic Phase Control

**Selecting divide ratio by DIVS pin**

| DIVS | Divide ratio |
|---|---|
| H | 1/8 |
| Open | EXT IN with pin 18 |
| L | 1/4 |

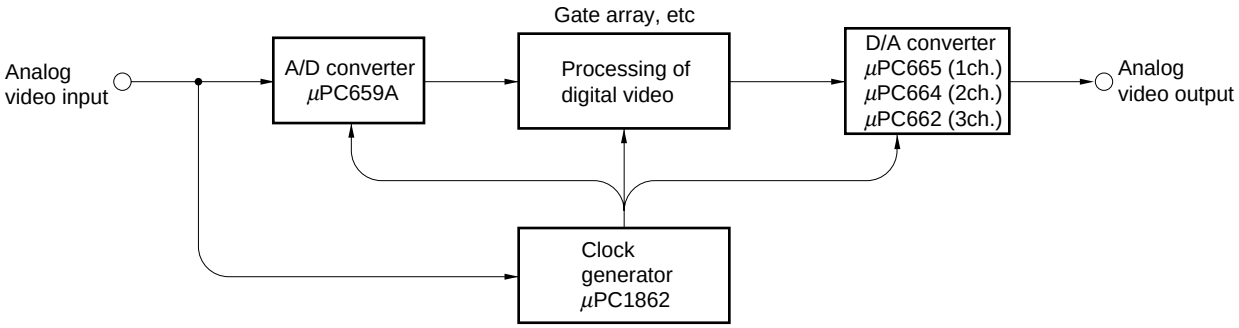
**Selecting TV transmission by N/P pin**

| N/P pin | TV transmission |
|---|---|
| H | PAL |
| L | NTSC |

In PAL, only correspond $4f_{SC}$ (DIVS = L).

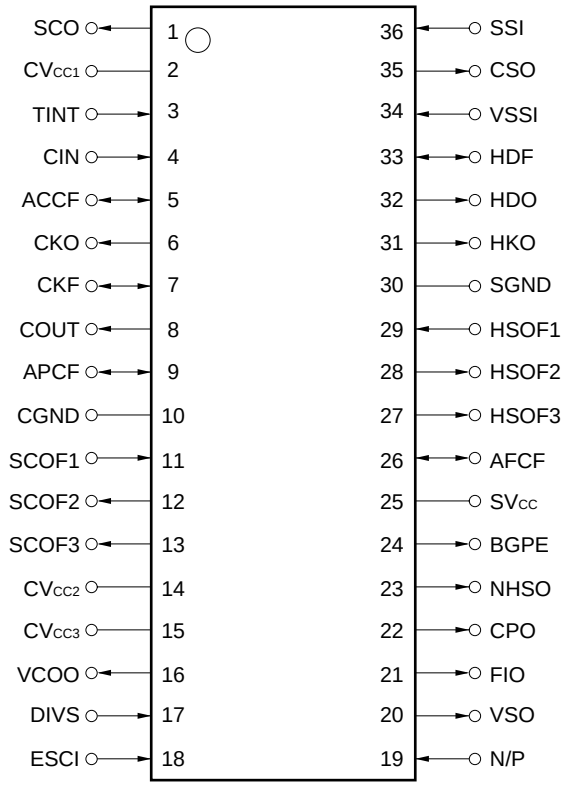
**System Block Diagram**

**Application to Process of Digital Video Signal**



## PIN CONFIGURATION (Top View)

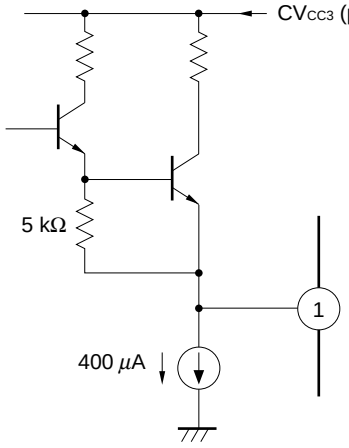
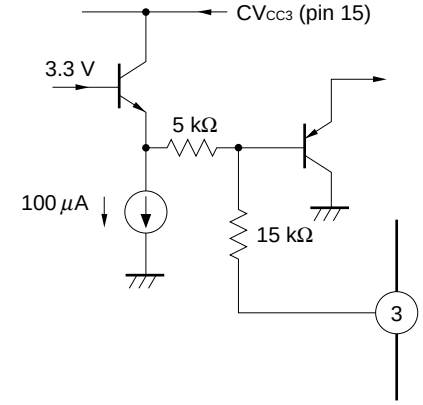
### 36-pin plastic shrink SOP (300 mil)



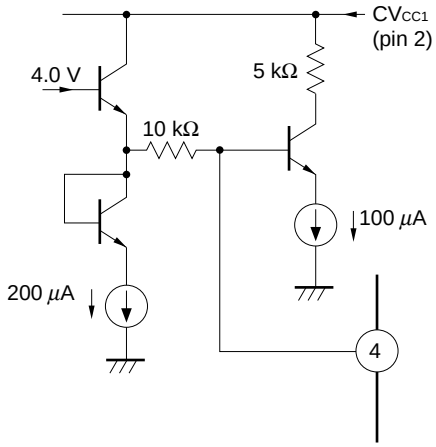
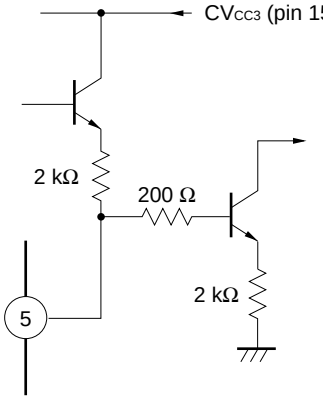
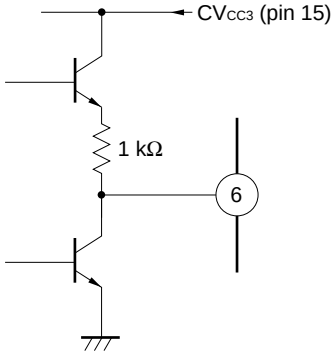
| | | |
|---|---|---|
| ACCF | : | Chroma ACC Filter |
| AFCF | : | Horizontal Sync AFC Filter |
| APCF | : | Chroma APC Filter |
| BGPE | : | Burst Gate Pulse from External |
| CGND | : | Chroma GND |
| CIN | : | Chroma Input |
| CKF | : | Color Killer Filter |
| CKO | : | Color Killer Output |
| COUT | : | Chroma Output |
| CPO | : | Clamp Pulse Output |
| CSO | : | Composite Sync Output |
| $CV_{CC1}$-$CV_{CC3}$ | : | Chroma $V_{CC}$ |
| DIVS | : | Divider Setting Input |
| ESCI | : | External Subcarrier Input |
| FIO | : | Field ID Output |
| HDF | : | Horizontal Sync Detect Filter |
| HDO | : | Horizontal Sync Detect Output |
| HKO | : | Horizontal Sync Killer Output |
| HSOF1-HSOF3 | : | $32f_H$ VCO Filter |
| NHSO | : | Negative Horizontal Sync Output |
| N/P | : | NTSC/PAL Mode Select |
| SCO | : | Subcarrier Output |
| SCOF1-SCOF3 | : | $f_{SC}$ VCO Filter |
| SGND | : | Sync GND |
| SSI | : | Horizontal Sync Separation Input |
| $SV_{CC}$ | : | Sync $V_{CC}$ |
| TINT | : | Tint Control |
| VCOO | : | VCO Output |
| VSO | : | Vertical Sync Output |
| VSSI | : | Vertical Sync Separation Input |

## PIN FUNCTIONS

(1/12)

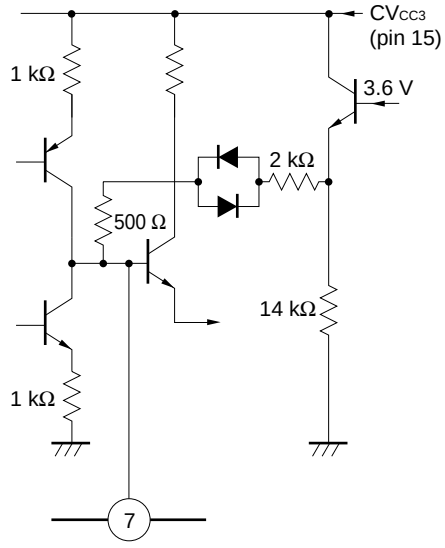
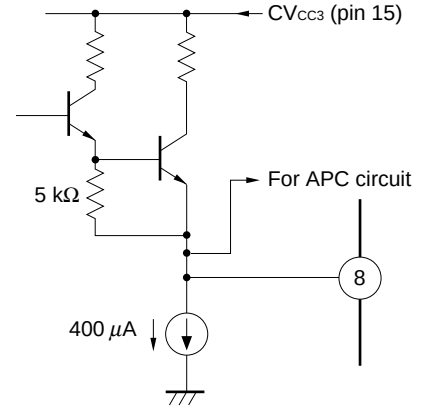
| Pin No. | Symbol | Pin Name | Equivalent Circuit | Function |
|---|---|---|---|---|
| 1 | SCO | Sub Carrier Output |  DC voltage of a standard: 2.9 V | Burst locked sub carrier output |
| 2 | CVCC1 | Chroma VCC1 | | Power supply for chroma signal processing circuit (pin 1 to pin 18) This power supply must be isolated from the power supply for sync processing circuit use. |
| 3 | TINT | Tint Control |  Internal bias voltage of a standard: 2.5 V | Tint control input (DC voltage) This pin adjusts the tint of sub carrier output (SCO pin). |

(2/12)

| Pin No. | Symbol | Pin Name | Equivalent Circuit | Function |
|---|---|---|---|---|
| 4 | CIN | Chroma Signal Input |  | Chroma signal input |
| | | | Internal bias voltage of a standard: 3.2 V | |
| 5 | ACCF | Chroma ACC Filter |  | Pin for connecting filter of ACC (Automatic Color Control) detector |
| | | | DC voltage of a standard[Note]: 1.0 V | |
| 6 | CKO | Color Killer Output |  | Color Killer Detection output<br>When Killer (without burst) signal: Low level output<br>When color signal: High level output |

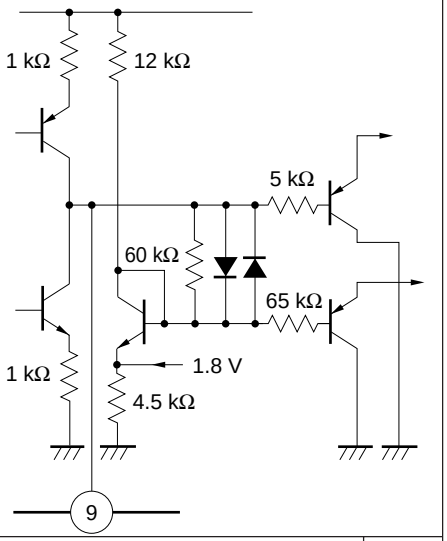
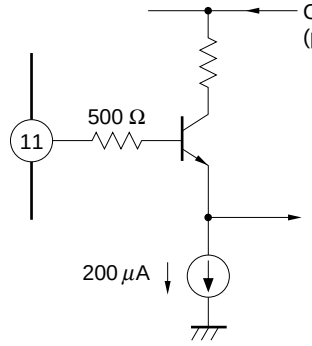
**Note** Chroma burst amplitude from pin 4: 150 $mV_{p-p}$

(3/12)

| Pin No. | Symbol | Pin Name | Equivalent Circuit | Function |
|---|---|---|---|---|
| 7 | CKF | Chroma Killer Filter |  DC voltage of a standard[Note] 2.2 V | Pin for connecting filter of Color killter detector |
| 8 | COUT | Chroma Signal Output |  DC voltage of a standard 2.4 V | Automatic color controlled chroma output |

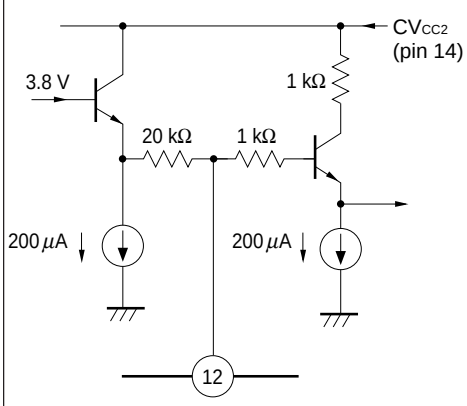
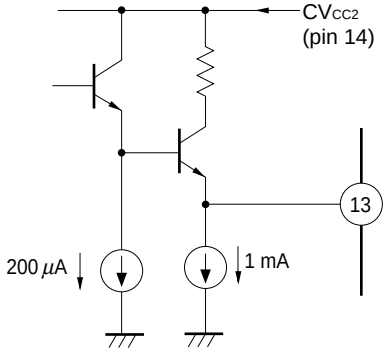
**Note** Chroma burst amplitude from pin 4: 150 $mV_{p-p}$

(4/12)

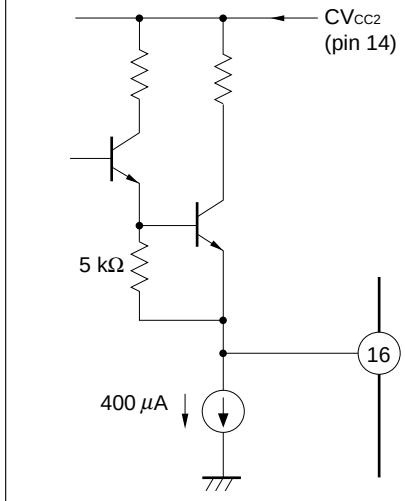
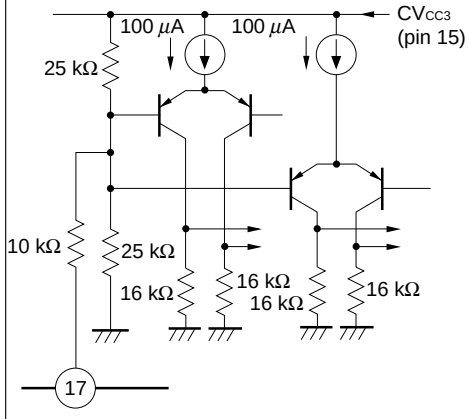
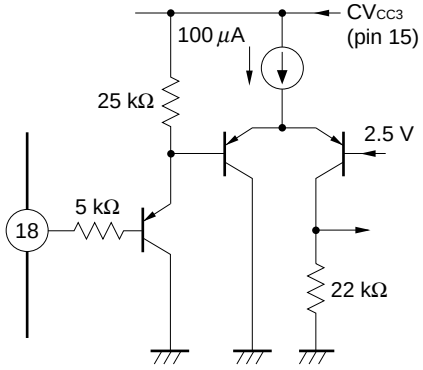
| Pin No. | Symbol | Pin Name | Equivalent Circuit | Function |
|---|---|---|---|---|
| 9 | APCF | APC Filter |  DC voltage of a standard[Note] 2.7 V | Pin for connecting filter of APC (Automatic Phase Control) detector |
| 10 | CGND | Chroma GND | | Ground for chroma signal processing circuit (pin 1 to pin 18) |
| 11 | SCOF1 | $nf_{SC}$ VCO Filter (1) |  Bias voltage of a standard 3.0 V | Pin for connecting filter of $nf_{SC}$ VCO |

**Note** Chroma burst amplitude from pin 4: 150 $mV_{p-p}$

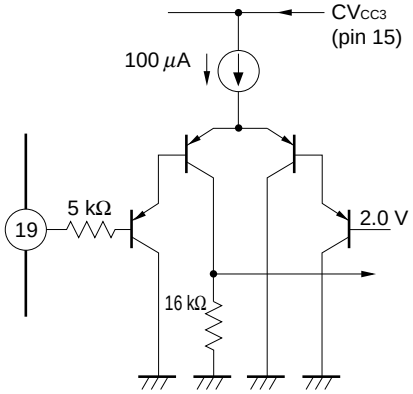
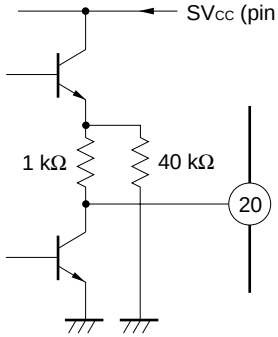
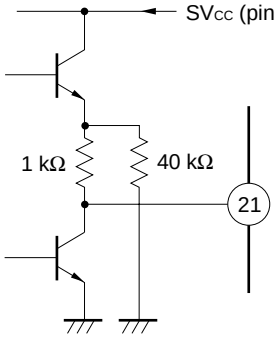
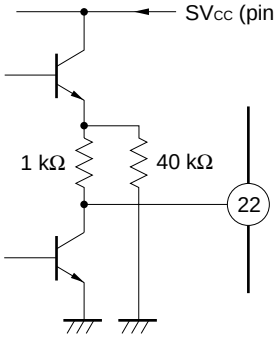
(5/12)

| Pin No. | Symbol | Pin Name | Equivalent Circuit | Function |
|---|---|---|---|---|
| 12 | SCOF2 | $nf_{SC}$ VCO Filter (2) |  Internal bias voltage of a standard: 3.0 V | Pin for connecting filter of $nf_{SC}$ VCO |
| 13 | SCOF3 | $nf_{SC}$ VCO Filter (3) |  DC voltage of a standard: 2.9 V | Pin for connecting filter of $nf_{SC}$ VCO |
| 14 | $CV_{CC2}$ | Chroma $V_{CC}$ 2 | | Power supply for chroma signal processing circuit (pin 1 to pin 18) This power supply must be isolated from the power supply for sync processing circuit use. |
| 15 | $CV_{CC3}$ | Chroma $V_{CC}$ 3 | | Power supply for chroma signal processing circuit (pin 1 to pin 18) This power supply must be isolated from the power supply for sync processing circuit use. |

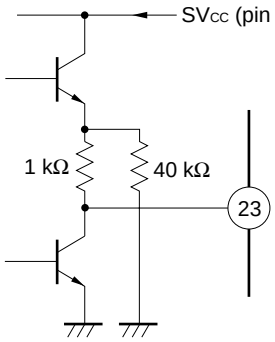
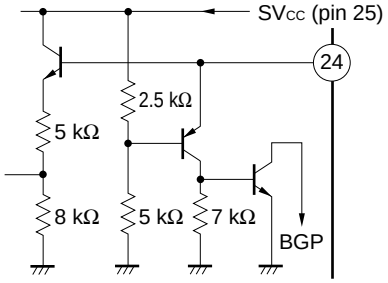
(6/12)

| Pin No. | Symbol | Pin Name | Equivalent Circuit | Function |
|---|---|---|---|---|
| 16 | VCOO | VCO Output |  <br>DC voltage of a standard: 2.8 V | Burst locked VCO output |
| 17 | DIVS | Dividing ratio selection |  | Divider ratio selection input<br>When 1/4: Low level input<br>When 1/8: High level input<br>When external dividing: Middle level input |
| 18 | ESCI | External subcarrier Input<br>(External Divide) |  | External subcarrier input.<br>When no use (pin 17 is not middle level): Low level input |

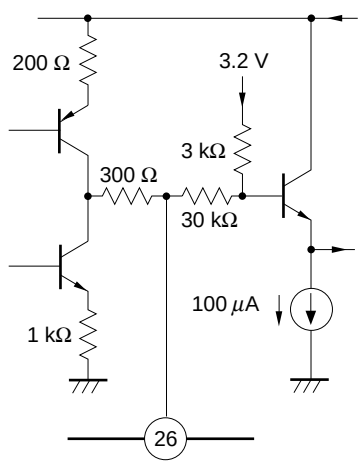
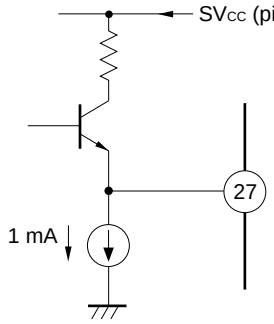
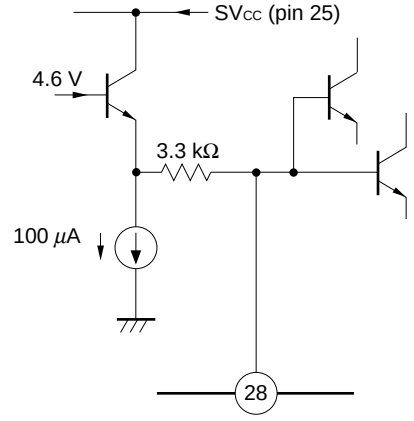
(7/12)

| Pin No. | Symbol | Pin Name | Equivalent Circuit | Function |
|---|---|---|---|---|
| 19 | N/P | NTSC/PAL selection |  | NTSC/PAL system selection input<br>When NTSC system: Low level input<br>When PAL system: High level input |
| 20 | VSO | Vertical Sync Output |  | Negative polarity vertical sync output |
| 21 | FIO | Field ID Output |  | Odd/Even field ID output<br>When Odd ID: Low level output<br>When Even ID: High level output<br>When a input is non-standard signal, this pin outputs an indefiniteness. |
| 22 | CPO | Clamp Pulse Output |  | Pedestal Clamp pulse (burst gate pulse) output |

(8/12)

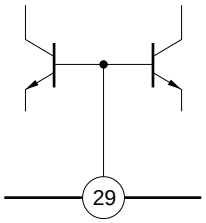
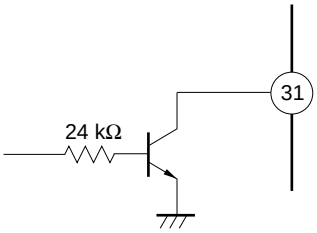
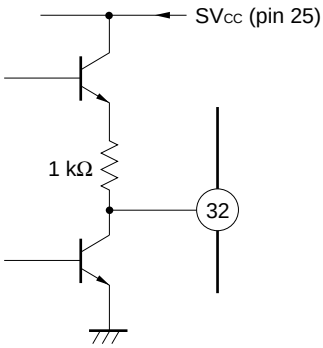
| Pin No. | Symbol | Pin Name | Equivalent Circuit | Function |
|---|---|---|---|---|
| 23 | NHSO | Negative Horizontal Sync Output |  | Negative polarity horizontal sync output |
| 24 | BGPE | Burst Gate Pulse from External |  | Burst gate pulse input<br>In inside burst gate pulse generation mode: Low level fix<br>In external burst gate pulse input mode:<br>When Non-burst period: Middle level input<br>When burst period: High level input |
| 25 | SVCC | Sync VCC | | Power supply for sync signal processing circuit (pin 19 to pin 36)<br>This power supply must be isolated from the power supply for chroma processing circuit use. |

(9/12)

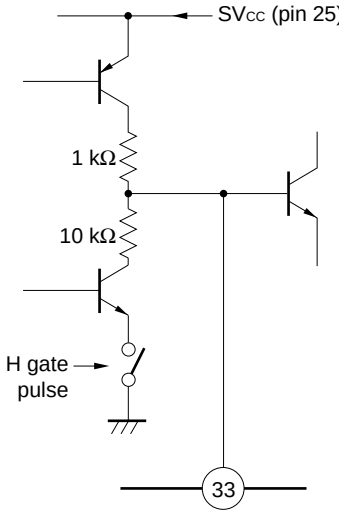
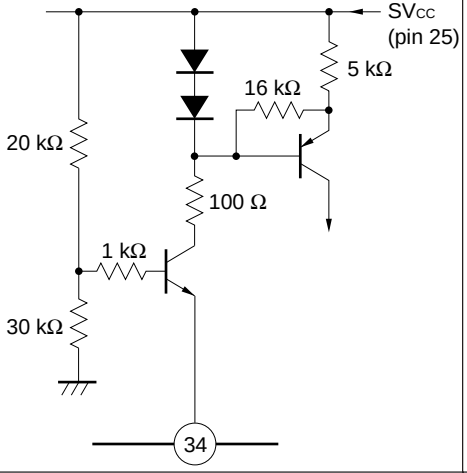
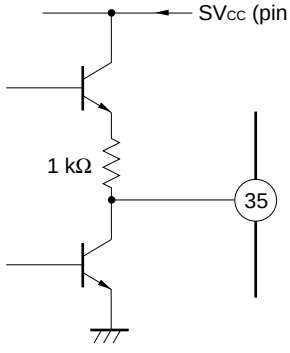
| Pin No. | Symbol | Pin Name | Equivalent Circuit | Function |
|---|---|---|---|---|
| 26 | AFCF | AFC Filter |  DC voltage of a standard[Note] 3.2 V | Pin for connecting filter of horizontal AFC (Automatic Frequency Control) detector |
| 27 | HSOF3 | 32fH VCO Filter (3) |  DC voltage of a standard 2.4V | Pin for connecting filter of 32fH VCO |
| 28 | HSOF2 | 32fH VCO Filter (2) |  Internal bias voltage of a standard 3.8 V | Pin for connecting filter of 32fH VCO |

**Note** When only 0.3 $V_{p\text{-}p}$ sync signal is input to pin 36

(10/12)

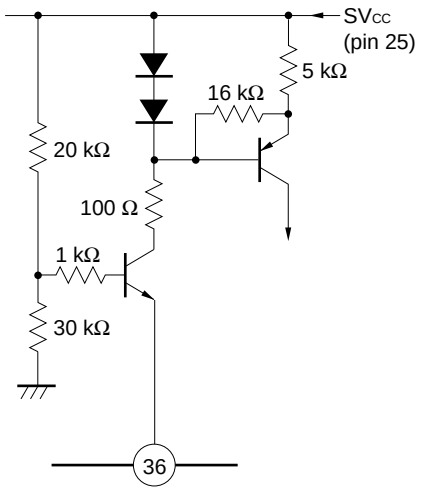
| Pin No. | Symbol | Pin Name | Equivalent Circuit | Function |
|---|---|---|---|---|
| 29 | HSOF1 | 32$f_H$ VCO Filter (1) |  Bias voltage of a standard 3.8 V | Pin for connecting filter of 32$f_H$ VCO |
| 30 | SGND | Sync GND | | Ground for sync processing circuit (pin 19 to pin 36) |
| 31 | HKO | Horizontal Killer Output |  | Horizontal killer output (Open Corrector)<br>When No sync: High impedance output<br>When sync: Low level output |
| 32 | HDO | Horizontal Sync Detection Output |  | Horizontal sync detection signal output<br>When No sync: High level output<br>When sync: Low level output |

(11/12)

| Pin No. | Symbol | Pin Name | Equivalent Circuit | Function |
|---|---|---|---|---|
| 33 | HDF | Horizontal Sync Detection Filter |  Bias voltage of a standard[Note] 4.1 V | Pin for connecting filter of Horizontal sync detector |
| 34 | VSSI | Vertical Sync Separator Input |  | Vertical sync separation input pin |
| 35 | CSO | Composite Sync Separator Output |  | Negative polarity composite sync output |

**Note** When only 0.3 $V_{p\text{-}p}$ sync signal is input to pin 36

(12/12)

| Pin No. | Symbol | Pin Name | Equivalent Circuit | Function |
|---|---|---|---|---|
| 36 | SSI | Horizontal Sync Separator Input |  | Horizontal sync separation input pin |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C, unless otherwise specified)

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7 | V |
| Input signal voltage (Chroma signal) | $e_{i4}$ | 3 | $V_{p-p}$ |
| Input signal voltage (H sync separation) | $e_{i36}$ | 3 | $V_{p-p}$ |
| Input signal voltage (V sync separation) | $e_{i34}$ | 3 | $V_{p-p}$ |
| Input signal voltage (EXT) | $e_{i18}$ | $V_{CC}$ | $V_{p-p}$ |
| Tint control signal voltage | $e_{c3}$ | $V_{CC}$ | V |
| Output current | $I_O$ | –7 | mA |
| Permissible package power dissipation (when mounted on PCB) | $P_D$ | 570 ($T_A$ = 75°C) | mW |
| Operating ambient temperature | $T_A$ | –10 to +75 | °C |
| Storage temperature | $T_{stg}$ | –40 to +125 | °C |

**Caution Expose to Absolute Maximum Rating for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.**

### RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input signal voltage (Chroma signal) | $e_{i4}$ | | 150 | | $mV_{p-p}$ |
| Input signal voltage (H sync separation) | $e_{i36}$ | | 1.0 | | $V_{p-p}$ |
| Input signal voltage (V sync separation) | $e_{i34}$ | | 1.0 | | $V_{p-p}$ |
| Input signal voltage (EXT IN HIGH voltage) | $e_{iH18}$ | 2.0 | | | V |
| Input signal voltage (EXT IN LOW voltage) | $e_{iL18}$ | | | 0.8 | V |
| Divider selector voltage 1 (1/8) | $V_{17\,(8)}$ | 4.8 | | | V |
| Divider selector voltage 2 (1/4) | $V_{17\,(4)}$ | | | 0.2 | V |
| Tint control voltage | $V_3$ | | 2.5 | | V |
| NTSC/PAL select voltage (PAL) | $V_{19P}$ | 4.5 | | | V |
| NTSC/PAL select voltage (NTSC) | $V_{19N}$ | | | 0.5 | V |

## ELECTRICAL CHARACTERISTICS (at $T_A$ = 25±3 °C, RH ≤ 70 %, $V_{CC}$ = 5 V, unless otherwise specified)

### Chroma section

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Supply current of chroma section | $I_{CC\,(C)}$ | $V_{CC\,(C)}$ = 5 V<br>No current on pin 2, 14 and 15 | 17 | 21 | 25 | mA |
| ACC amplitude characteristic 1 | $ACC_1$ | Fluctuation of chroma output level at +6 dB change of chroma input burst signal (0 dB = 150 $mV_{p-p}$) | –2.0 | 0 | +2.0 | dB |
| ACC amplitude characteristic 2 | $ACC_2$ | Fluctuation of chroma output level at –20 dB change of chroma input burst signal (0 dB = 150 $mV_{p-p}$) | –5.0 | –1.0 | +1.0 | dB |
| Color killer set point | $e_{KS}$ | Input level at killer ON with chroma input burst sig. (0 dB = 150 $mV_{p-p}$) being attenuated | –45 | –39 | –33 | dB |
| Color residual of color killer | $e_{KR}$ | Residual level of chroma output in Killer ON state when chroma input burst signal of 150 $mV_{p-p}$ is input | - | - | 15 | $mV_{p-p}$ |
| Chroma output level | $E_{COUT}$ | Chroma output level when chroma input burst signal of 150 $mV_{p-p}$ is input | 1.1 | 1.3 | 1.5 | $V_{p-p}$ |
| Color killer output High level (1) | $E_{CKOH\,(1)}$ | High level of color killer output at color killer OFF<br>$I_{OH}$ = –400 μA | 2.7 | 3.5 | - | V |
| Color killer output High level (2) | $E_{CKOH\,(2)}$ | High level of color killer output at color killer OFF<br>$I_{OH}$ = –20 μA | 3.5 | 4.0 | - | V |
| Color killer output Low level | $E_{CKOL}$ | Low level of color killer output at color killer ON<br>$I_{OL}$ = +2 mA | - | 0.2 | 0.4 | V |
| APC lock-in range | $f_P$ | Frequency pulled by APC with chroma input burst frequency changed ($f_{SC}$ conversion) | ±400 | ±600 | - | Hz |
| VCO control sensitivity | $\beta_P$ | Rate of variation of frequency when APC filter pin is changed from –0.025 V to +0.025 V ($f_{SC}$ conversion) | 8.0 | 10.0 | 12.0 | Hz/mV |
| Phase variable range | $\theta_{CONT}$ | Amount of phase shift when voltage of phase control pin is set at 2.5 V + 1 V | ±40 | ±55 | - | deg |
| VCO output level | $e_{VCOO}$ | VCO output level when chroma input burst signal of 150 $mV_{p-p}$ is input | 1.0 | 1.3 | 1.6 | $V_{p-p}$ |
| $f_{SC}$ output level | $e_{SCO}$ | $f_{SCO}$ output level when chroma input burst signal of 150 $mV_{p-p}$ is input | 210 | 300 | 390 | $mV_{p-p}$ |
| Divider select voltage | $V_{DIVSL}$ | 1/4 freq. division if $V_{DIVS}$ < $V_{DIVSL}$<br>EXT IN with $V_{DIVS}$ : OPEN<br>1/8 freq. division if $V_{DIVSH}$ < $V_{DIVS}$ | - | - | 0.5 | V |
| | $V_{DIVSH}$ | | 4.5 | - | - | V |
| NTSC/PAL select voltage | $V_{N/PT}$ | $f_V$ = 60 Hz if $V_{N/P}$ < $V_{N/PT}$<br>$f_V$ = 50 Hz if $V_{N/PT}$ < $V_{N/P}$ | 1.7 | 2.0 | 2.3 | V |

**Sync section**

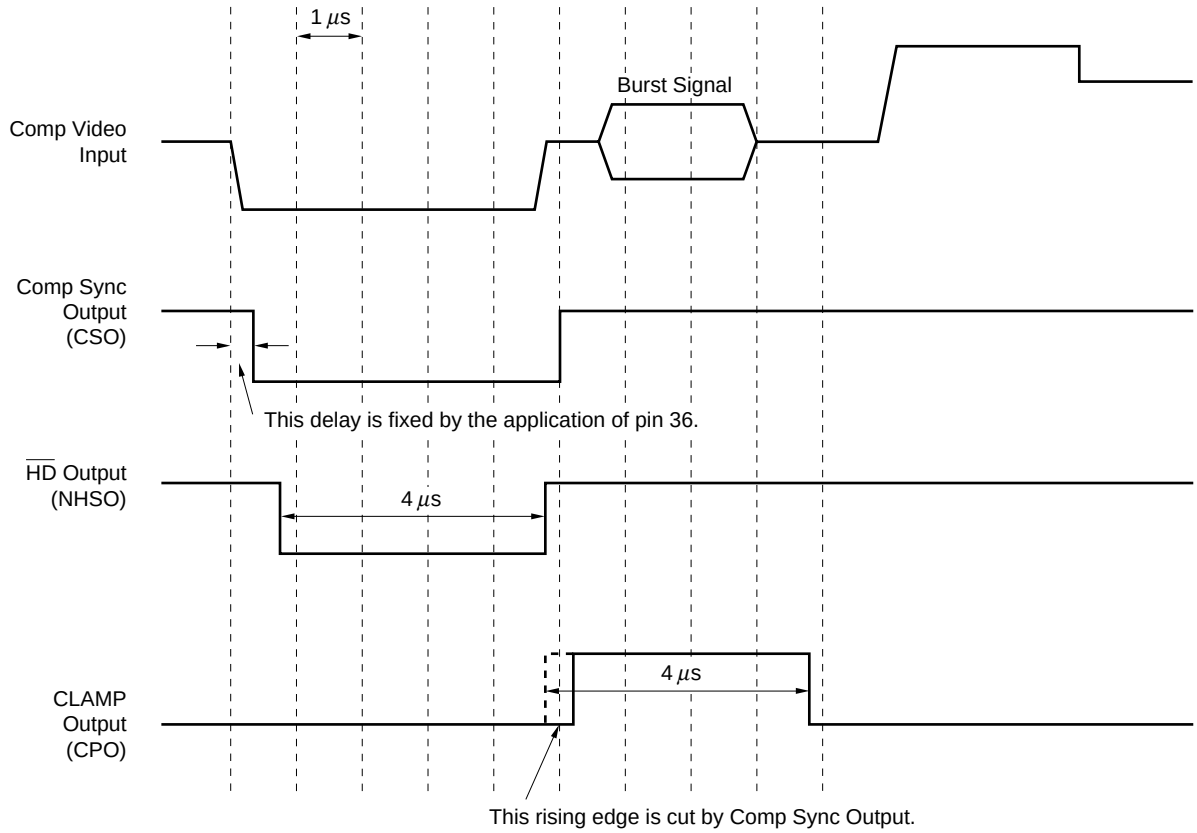
| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Supply current of Sync section | $I_{CC(1)}$ | $V_{CC(1)}$ = 5 V<br>No current on pin 25 | 12 | 15 | 18 | mA |
| DC level of H sync separation input | $V_{SSI}$ | Voltage of pin 36 when connected to GND via 10 kΩ resistor | 1.9 | 2.2 | 2.5 | V |
| DC level of V sync separation input | $V_{VSSI}$ | Voltage of pin 34 when connected to GND via 10 kΩ resistor | 1.9 | 2.2 | 2.5 | V |
| Sync separation output High level (1) | $E_{CSOH1}$ | High level of sync separation output when only 0.3 $V_{p-p}$ sync signal is input to pin 36<br>$I_{OH}$ = –400 μA | 2.7 | 3.8 | - | V |
| Sync separation output High level (2) | $E_{CSOH2}$ | High level of sync separation output when only 0.3 $V_{p-p}$ sync signal is input to pin 36<br>$I_{OH}$ = –20 μA | 3.5 | 4.3 | - | V |
| Sync separation output Low level | $E_{CSOL}$ | Low level of sync separation output when only 0.3 $V_{p-p}$ sync signal is input to pin 36<br>$I_{OL}$ = +2 mA | - | 0.1 | 0.4 | V |
| $\overline{HD}$ output High level (1) | $E_{NHSOH1}$ | High level of synchronized $\overline{HD}$ output when only 0.3 $V_{p-p}$ sync signal is input to pin 36<br>$I_{OH}$ = –400 μA | 2.7 | 3.8 | - | V |
| $\overline{HD}$ output High level (2) | $E_{NHSOH2}$ | High level of synchronized $\overline{HD}$ output when only 0.3 $V_{p-p}$ sync signal is input to pin 36<br>$I_{OH}$ = –20 μA | 3.5 | 4.3 | - | V |
| $\overline{HD}$ output Low level | $E_{NHSOL}$ | High level of synchronized $\overline{HD}$ output when only 0.3 $V_{p-p}$ sync signal is input to pin 36<br>$I_{OL}$ = +2 mA | - | 0.1 | 0.4 | V |
| VD output High level (1) | $E_{VSOH1}$ | High level of synchronized VD output when only 0.3 $V_{p-p}$ sync signal is input to pin 36<br>$I_{OH}$ = –400 μA | 2.7 | 3.8 | - | V |
| VD output High level (2) | $E_{VSOH2}$ | High level of synchronized VD output when only 0.3 $V_{p-p}$ sync signal is input to pin 36<br>$I_{OH}$ = –20μA | 3.5 | 4.3 | - | V |
| VD output Low level | $E_{VSOL}$ | High level of synchronized VD output when only 0.3 $V_{p-p}$ sync signal is input to pin 36<br>$I_{OL}$ = +2 mA | - | 0.1 | 0.4 | V |
| Clamp output High level (1) | $E_{CPOH1}$ | High level of synchronized Clamp output when only 0.3 $V_{p-p}$ sync signal is input to pin 36<br>$I_{OH}$ = –400 μA | 2.7 | 3.8 | - | V |
| Clamp output High level (2) | $E_{CPOH2}$ | High level of synchronized Clamp output when only 0.3 $V_{p-p}$ sync signal is input to pin 36<br>$I_{OH}$ = –20 μA | 3.5 | 4.3 | - | V |
| Clamp output Low level | $E_{CPOL}$ | High level of synchronized Clamp output when only 0.3 $V_{p-p}$ sync signal is input to pin 36<br>$I_{OL}$= +2 mA | - | 0.1 | 0.4 | V |

| Parameter | Symbol | Condition | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Field ident. output High level (1) | $E_{FIOH1}$ | High level of synchronized Field ident. output when only 0.3 $V_{p-p}$ sync signal is input to pin 36 $I_{OH}$ = –400 μA | | 2.7 | 3.8 | - | V |
| Field ident. output High level (2) | $E_{FIOH2}$ | High level of synchronized Field ident. output when only 0.3 $V_{p-p}$ sync signal is input to pin 36 $I_{OH}$ = –20 μA | | 3.5 | 4.3 | - | V |
| Field idnet. output Low level | $E_{FIOL}$ | High level of synchronized Field ident. output when only 0.3 $V_{p-p}$ sync signal is input to pin 36 $I_{OL}$ = +2 mA | | - | 0.1 | 0.4 | V |
| H detection output High level (1) | $E_{FIOH1}$ | High level of asynchronized H detect output without H sync input $I_{OH}$ = –400 μA | | 2.7 | 3.8 | - | V |
| H detection output High level (2) | $E_{FIOH2}$ | High level of asynchronized H detect output without H sync input $I_{OH}$ = –20 μA | | 3.5 | 4.3 | - | V |
| H detection output Low level | $E_{FIOL}$ | High level of synchronized H detect output when only 0.3 $V_{p-p}$ sync signal is input to pin 36 $I_{OL}$= +2 mA | | - | 0.1 | 0.4 | V |
| H sync lock-in range | $f_{HP}$ | Frequency range that can be pulled when only 0.3 $V_{p-p}$ sync signal is input to pin 36 and H sync frequency is varied ($f_{SC}$ conversion) | | ±400 | ±500 | - | Hz |
| Horizontal VCO control sensitivity | $\beta_H$ | Rate of variation of frequency when APC filter pin is changed form 3.0 V to 3.4 V without H sync input ($f_{SC}$ conversion) | | –1.6 | –1.3 | –0.9 | Hz/mV |
| Horizontal VCO free-run frequency | $f_{HO}$ | Frequency difference of HD output from $f_H$ when H sync input is not applied | | –100 | –25 | +50 | Hz |
| Pulse width of $\overline{HD}$ output | $P_{WNHSO}$ | Pulse width of synchronized $\overline{HD}$ output when only 0.3 $V_{p-p}$ sync signal is input to pin 36 | | 3.8 | 4.0 | 4.2 | μs |
| Pulse width of VD output | $P_{WVSO1}$ | Pulse width of synchronized VD output when only 0.3 $V_{p-p}$ sync signal is input to pin 36 | ODD | - | 6.0 | - | H[Note] |
| | $P_{WVSO2}$ | | EVEN | - | 5.5 | - | H[Note] |
| Pulse width of Clamp output | $P_{WCPO}$ | Pulse width of synchronized Clamp output when only 0.3 $V_{p-p}$ sync signal is input to pin 36 | | 3.4 | 3.6 | 3.8 | μs |
| Oscillation start voltage of horizontal VCO | $V_{ST}$ | Output voltage at $\overline{HD}$ when $V_{CC}$ is gradually increased from 0 V without H sync input | | - | - | 4.2 | V |
| H killer output Low level | $E_{HKOL}$ | Low level of synchronized H killer output when only 0.3 $V_{p-p}$ sync signal is input to pin 36 Change value of Chroma output | | - | - | 0.4 | V |
| Burst gate input Threshold level 1 | $V_{BGPE1}$ | Burst gate pulse input voltage when Clamp voltage begins Low level is gradually increased from 0 V without signal input | | 1.6 | 1.9 | 2.0 | V |

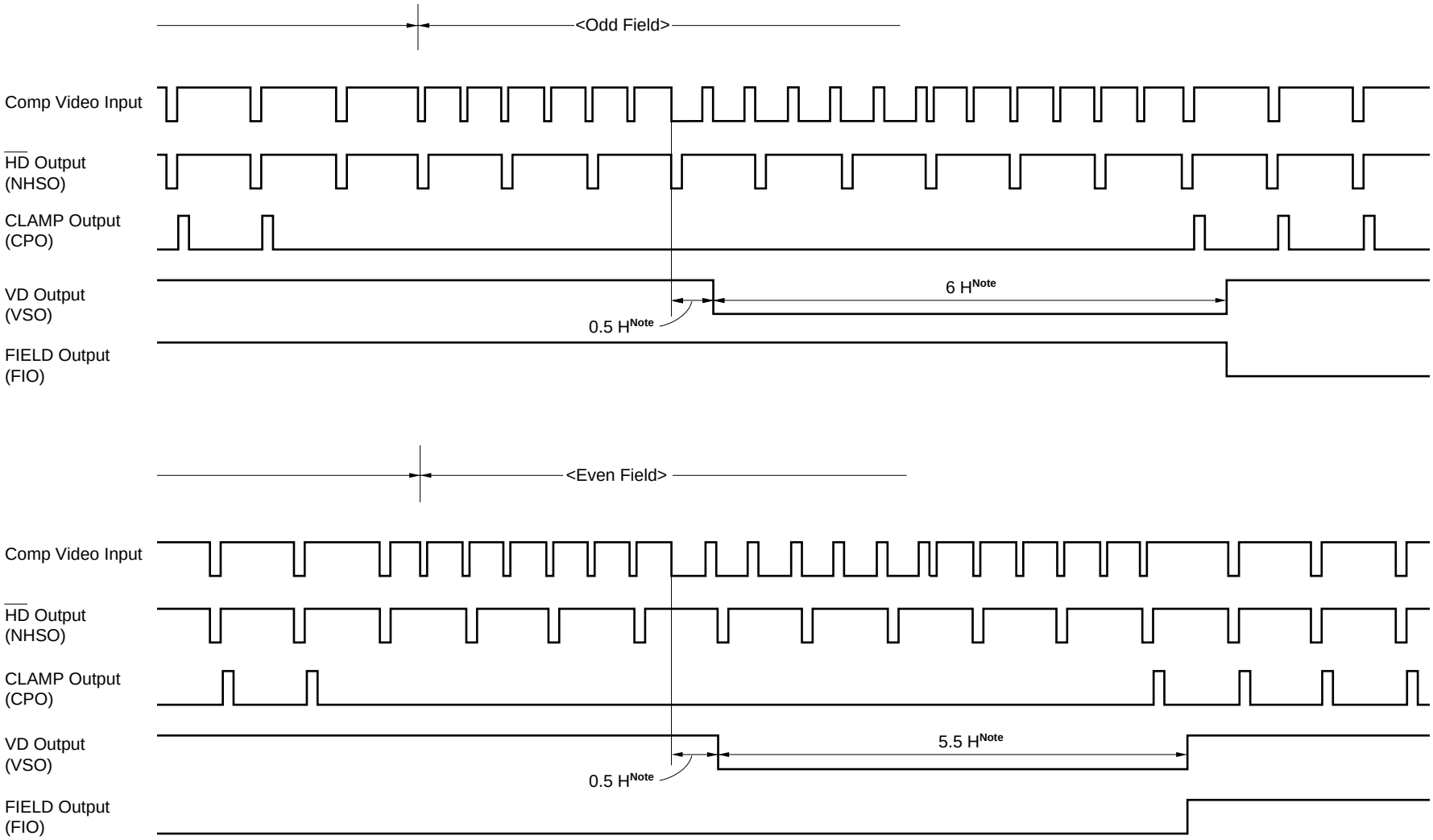
**Note** H: Horizontal scanning period

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Burst gate input Threshold level 2 | $V_{BGPE2}$ | Burst gate pulse input voltage when Clamp voltage begins High level is gradually increased from $V_{BGPE1}$ without signal input | 3.8 | 4.0 | 4.2 | V |
| Vertical free-running frequency 1 | $f_{V1\ (50)}$ | Frequency ratio of HD output to VD output<br>H sync input: No signal<br>Pin 33 input: $V_{CC}$<br>V sync input: $V_{CC}$ | - | $f_H/352$ | - | Hz |
| | $f_{V1\ (60)}$ | | - | $f_H/288$ | - | Hz |
| Vertical free-running frequency 2 | $f_{V2\ (50)}$ | Same as $f_{V1}$ with the following exception<br>V sync input: GND | - | $f_H/288$ | - | Hz |
| | $f_{V2\ (60)}$ | | - | $f_H/240$ | - | Hz |
| Vertical free-running frequency 3 | $f_{V3\ (50)}$ | Same as $f_{V1}$ with the following exception<br>Pin 33 input: GND | - | $f_H/368$ | - | Hz |
| | $f_{V3\ (60)}$ | | - | $f_H/296$ | - | Hz |
| Vertical free-running frequency 4 | $f_{V4\ (50)}$ | Same as $f_{V1}$ with the following exception<br>Pin 33 input: GND<br>V sync input: GND | - | $f_H/272$ | - | Hz |
| | $f_{V4\ (60)}$ | | - | $f_H/232$ | - | Hz |

**TIMING CHARTS (Horizontal Period)**



## TIMING CHARTS (Vertical Period)




**Note** H: Horizontal scanning period

## CAUTION AT DESIGNING

### Resonators

NEC evaluates μPC1862 using resonators which are shown below in design and development process.

If the different product is used as a resonator, electrical specification value described in this document is not assured.

And when connecting resonator to external circuit, there is need to consider temperature specification, voltage fluctuation and product variation. In this case, normal operation is not assured in the application circuit including the different product.

Use the resonators which are shown below when you design circuit.

32 $f_H$ VCO resonator $X_1$ : in application example circuit
$X_1$ (PAL) : CSB500F2 (MURATA)
(NTSC) : CSB503F2 (MURATA)
n$f_{SC}$ VCO resonator $X_2$
$X_2$ : HC-49/U (KINSEKI, μPC1860 adoption)

**Reference data of 4$f_{SC}$, 8$f_{SC}$ VCO resonator (KINSEKI)**

| Item | NTSC for 4$f_{SC}$ | NTSC for 8$f_{SC}$ | PAL for 4$f_{SC}$ |
|---|---|---|---|
| Name | HC-49/U | | |
| Frequency | 14.31818 MHz | 28.63636 MHz | 17.34475 MHz |
| Overtone Order | Fundamental (AT cut) | Fundamental (BT cut) | Fundamental (AT cut) |
| Operating Temperature | –10 to +70°C | | |
| Frequency Permitted Tolerance (25±5°C) | $\pm 30 \times 10^{-6}$ | $\pm 50 \times 10^{-6}$ | $\pm 30 \times 10^{-6}$ |
| Frequency Temperature Specification (to 25°C) | $\pm 30 \times 10^{-6}$ | $\pm 100 \times 10^{-6}$ | $\pm 30 \times 10^{-6}$ |
| Equivalent Serial Resistance | 50 Ω or less | | |
| Parallel Capacitance | 7.0 pF or less | | |
| 3rd harmonic standard | 3rd harmonic frequency is over 3$f_O$ (42.95454 MHz) + 7.5 kHz | – | 3rd harmonic frequency is over 3$f_O$ (53.203425 MHz) + 7.5 kHz |

**Recommended pattern**

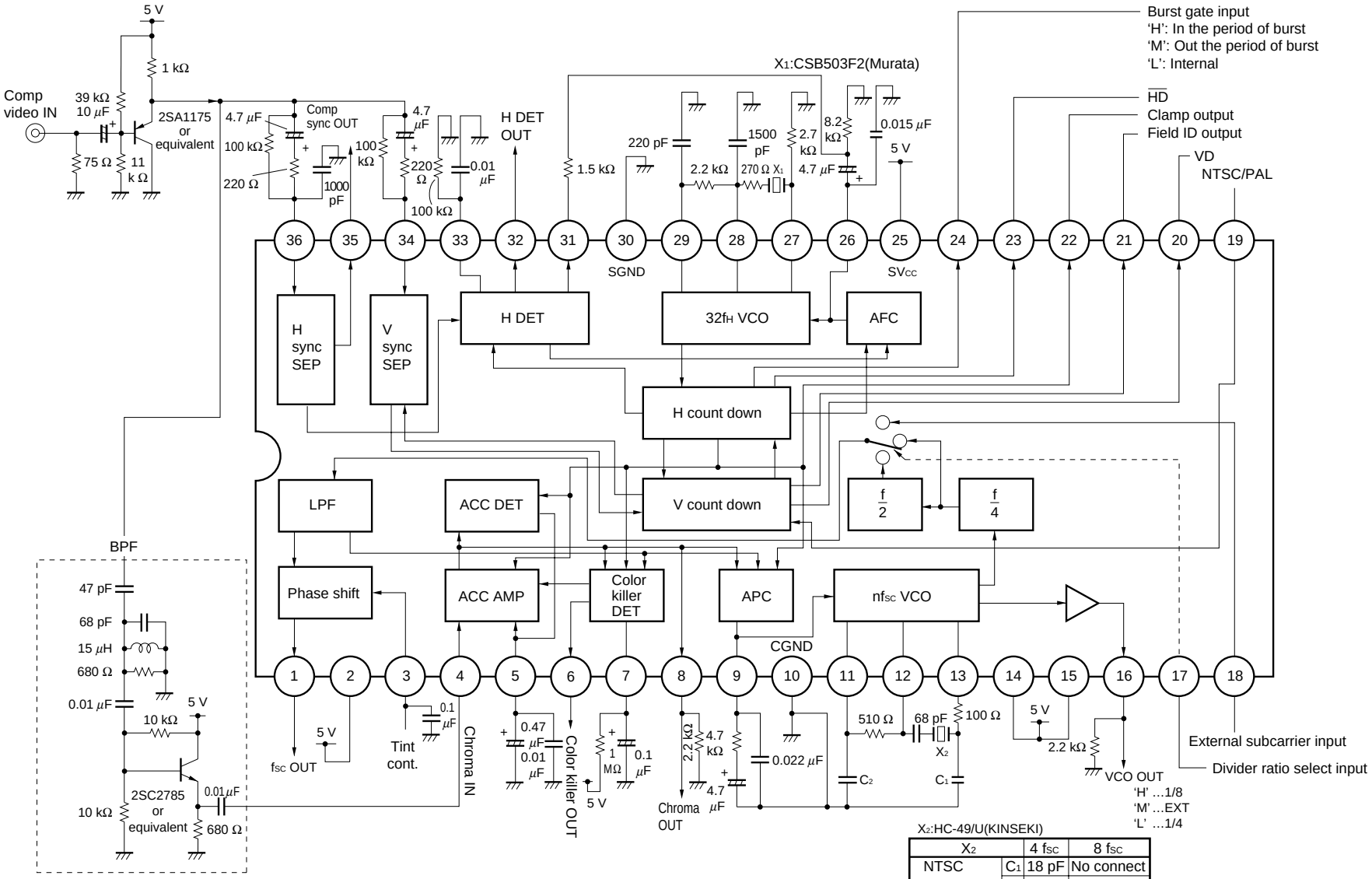
The μPC1862 generates system clock for synchronous signal processing and clock generate processing.

If the supply voltage, line placement and routing are not set appropriately that the μPC1862 cannot generate correct system clock.

Though the recommended pattern is not shows in this document, note points shown below at designing.

1. For synchronous section and chroma section, each power supply must be isolated.
2. Lines to pin 9 to pin 13 should be as thick and short as possible.
3. Connect resonator as near IC as possible. Don't put GND line between resonator pins for parasitism capacitance.

## APPLICATION CIRCUIT




X2:HC-49/U(KINSEKI)

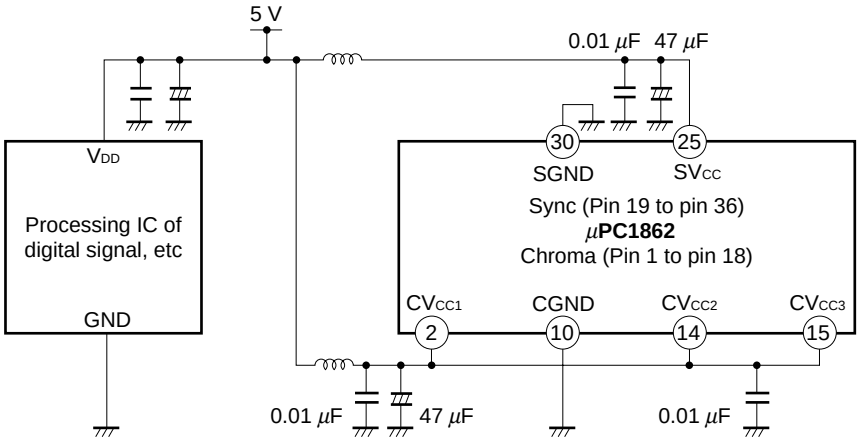
| X2 | | 4 fSC | 8 fSC |
|---|---|---|---|
| NTSC (N/P ='L') | C1 | 18 pF | No connect |
| | C2 | 22 pF | 10 pF |
| PAL (N/P ='H') | C1 | 12 pF | – |
| | C2 | 18 pF | – |

Cannot correspond 8fSC of PAL.

**Care Point for Planning of Application Circuit**

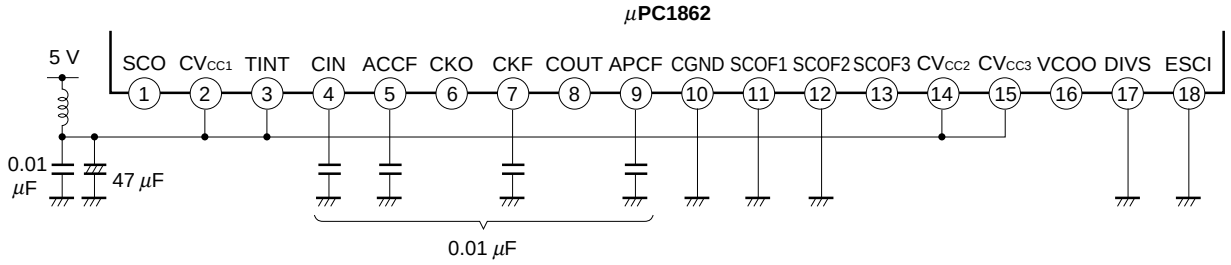
**1. Processing of $V_{CC}$ pin**

Please isolate Chroma. $V_{CC}$ from Sync. $V_{CC}$ as follows. If you have external processing block of digital signal, don't directly supply of the block's $V_{DD}$.




**2. Application of no using Chroma pin**

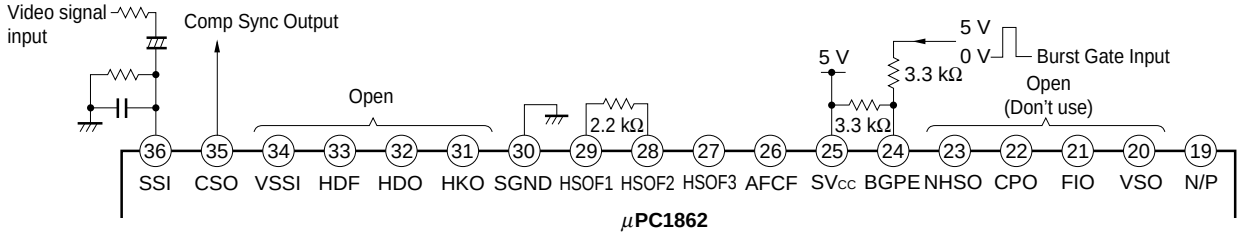
If you don't use Chroma pin but use Sync pin on μPC1862, you process pin 1 to pin 18 as follows.




**3. Application of no using Sync pin**

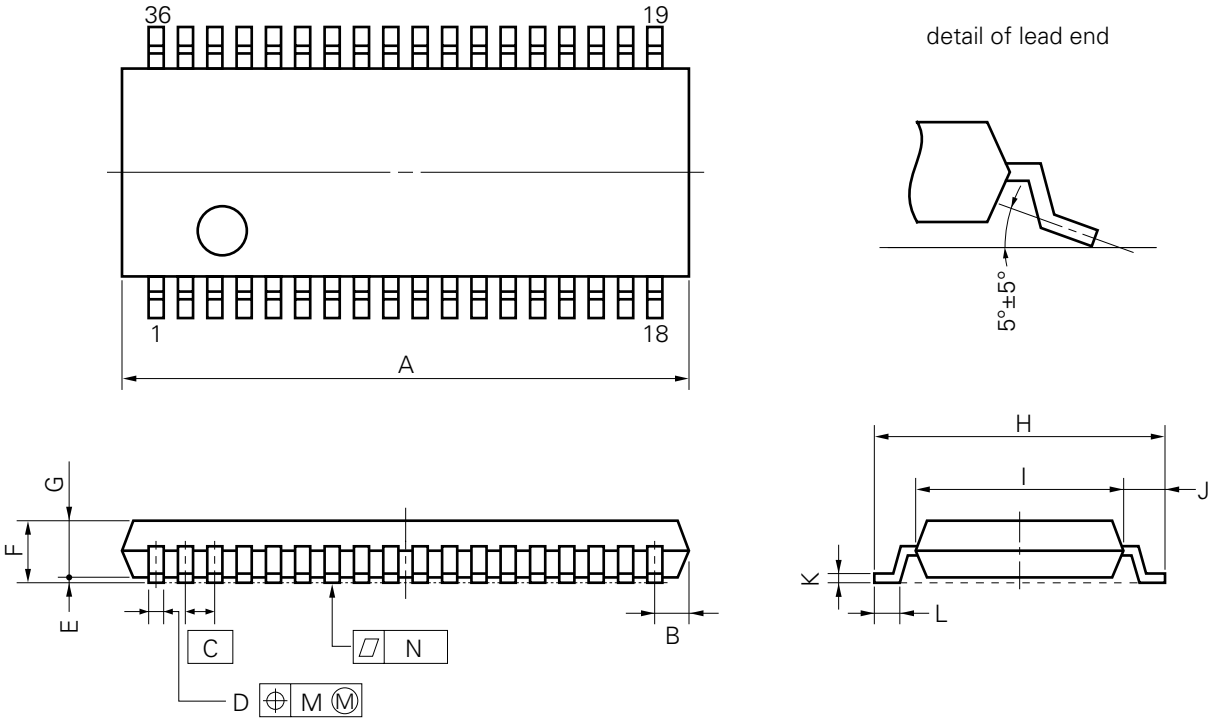
If you don't use Sync pin but use Chroma pin on μPC1862, you process pin 19 to pin 36 as follows. In this case, you need to input a pin 24 with burst gate pulse from external.

In this application, you can't use output of pin 20 to pin 23.



## PACKAGE DRAWING

### 36 PIN PLASTIC SHRINK SOP (300 mil)




P36GM-80-300B-3

**NOTE**

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 15.54 MAX. | 0.612 MAX. |
| B | 0.97 MAX. | 0.039 MAX. |
| C | 0.8 (T.P.) | 0.031 (T.P.) |
| D | $0.35^{+0.10}_{-0.05}$ | $0.014^{+0.004}_{-0.003}$ |
| E | 0.125±0.075 | 0.005±0.003 |
| F | 1.8 MAX. | 0.071 MAX. |
| G | 1.55 | 0.061 |
| H | 7.7±0.3 | 0.303±0.012 |
| I | 5.6 | 0.220 |
| J | 1.1 | 0.043 |
| K | $0.20^{+0.10}_{-0.05}$ | $0.008^{+0.004}_{-0.002}$ |
| L | 0.6±0.2 | $0.024^{+0.008}_{-0.009}$ |
| M | 0.10 | 0.004 |
| N | 0.10 | 0.004 |

## RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E)**.

### Surface Mount Device

**μPC1862GS: 36-pin plastic shrink SOP (300 mil)**

| Process | Conditions | Symbol |
|---|---|---|
| Infrared ray reflow | Peak temperature: 235 °C or below (Package surface temperature),<br>Reflow time: 30 seconds or less (at 210 °C or higher),<br>Maximum number of reflow processes: 2 times. | IR35-00-2 |
| VPS | Peak temperature: 215 °C or below (Package surface temperature),<br>Reflow time: 40 seconds or less (at 200 °C or higher),<br>Maximum number of reflow processes: 2 times. | VP15-00-2 |
| Wave Soldering | Solder temperature: 260 °C or below, Flow time: 10 seconds or less,<br>Maximum number of flow process: 1 time,<br>Pre-heating temperature: 120 °C or below (Package surface temperature). | WS60-00-1 |
| Partial heating method | Pin temperature: 300 °C or below,<br>Heat time: 3 seconds or less (Per each side of the device). | – |

**Caution Apply only one kind of soldering condition to a device, except for "Partial heating method", or the device will be damaged by heat stress.**

[MEMO]

**[MEMO]**

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.



M4 96.5