The RF MOSFET Line

RF Power Field Effect Transistors

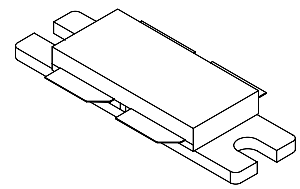
N-Channel Enhancement-Mode Lateral MOSFETs

MRF9120R3
MRF9120LR3

Designed for broadband commercial and industrial applications with frequencies from 865 to 895 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common source amplifier applications in 26 volt base station equipment.

- Typical CDMA Performance @ 880 MHz, 26 Volts, I_{DQ} = 2 x 500 mA
  IS-97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
  Output Power — 26 Watts
  Power Gain — 16 dB
  Efficiency — 26%
  Adjacent Channel Power —
  750 kHz: -45 dBc @ 30 kHz BW
  1.98 MHz: -60 dBc @ 30 kHz BW
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 880 MHz, 120 Watts (CW) Output Power
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Excellent Thermal Stability
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ″ Nominal.
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

**880 MHz, 120 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs**



**CASE 375B-04, STYLE 1
NI-860**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	- 0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	- 0.5, +15	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	W W/°C
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.45	°C/W

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

(1) MTTF calculator available at http://www.motorola.com/semiconductors/rf. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.

NOTE - **CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μAdc)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 450 mAdc)	$V_{GS(Q)}$	—	3.8	—	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.3 Adc)	$V_{DS(on)}$	—	0.17	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 4 Adc)	g_{fs}	—	5.3	—	S
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	50	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2	—	pF

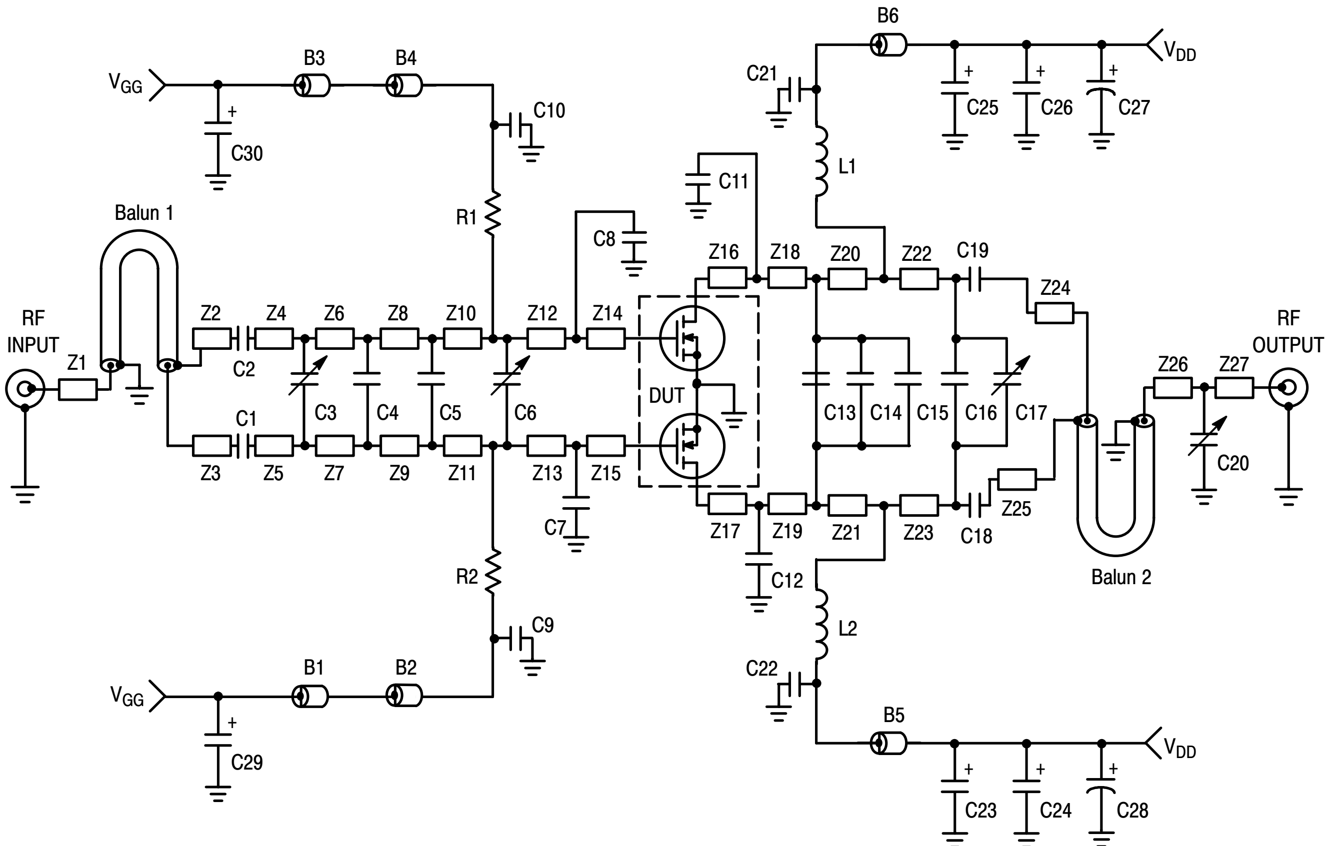
(1) Each side of device measured separately.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2)					
Two-Tone Common-Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 500 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	G_{ps}	15	16.5	—	dB
Two-Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 500 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	η	36	39	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 500 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	IMD	—	-31	-28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 500 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	IRL	—	-16	-9	dB
Two-Tone Common-Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 500 mA, f1 = 895.0 MHz, f2 = 895.1 MHz)	G_{ps}	—	16.5	—	dB
Two-Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 500 mA, f1 = 895.0 MHz, f2 = 895.1 MHz)	η	—	40.5	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 500 mA, f1 = 895.0 MHz, f2 = 895.1 MHz)	IMD	—	-30	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 500 mA, f1 = 895.0 MHz, f2 = 895.1 MHz)	IRL	—	-13	—	dB
Power Output, 1 dB Compression Point (V_{DD} = 26 Vdc, P_{out} = 120 W CW, I_{DQ} = 2 x 500 mA, f1 = 880.0 MHz)	P_{1dB}	—	120	—	W
Common-Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 120 W CW, I_{DQ} = 2 x 500 mA, f1 = 880.0 MHz)	G_{ps}	—	16	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 120 W CW, I_{DQ} = 2 x 500 mA, f1 = 880.0 MHz)	η	—	51	—	%
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 120 W CW, I_{DQ} = 2 x 500 mA, f = 880.0 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power			

(2) Device measured in push-pull configuration.



Z1	0.420″ x 0.080″ Microstrip
Z2, Z3	0.090″ x 0.420″ Microstrip
Z4, Z5	0.125″ x 0.220″ Microstrip
Z6, Z7	0.095″ x 0.220″ Microstrip
Z8, Z9	0.600″ x 0.220″ Microstrip
Z10, Z11	0.200″ x 0.630″ Microstrip
Z12, Z13	0.500″ x 0.630″ Microstrip
Z14, Z15	0.040″ x 0.630″ Microstrip
Z16, Z17	0.040″ x 0.630″ Microstrip
Z18, Z19	0.330″ x 0.630″ Microstrip
Z20, Z21	0.450″ x 0.630″ Microstrip
Z22, Z23	0.750″ x 0.220″ Microstrip
Z24, Z25	0.115″ x 0.420″ Microstrip
Z26	0.130″ x 0.080″ Microstrip
Z27	0.350″ x 0.080″ Microstrip

Figure 1. 880 MHz Broadband Test Circuit Schematic

Table 1. 880 MHz Broadband Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
B1, B3, B5, B6	Long Ferrite Beads, Surface Mount	95F787	Newark
B2, B4	Short Ferrite Beads, Surface Mount	95F786	Newark
C1, C2	68 pF Chip Capacitors, B Case	100B680JP500X	ATC
C3, C6	0.8 - 8.0 pF Variable Capacitors	44F3360	Newark
C4	7.5 pF Chip Capacitor, B Case	100B7R5JP150X	ATC
C5	3.3 pF Chip Capacitor, B Case	100B3R3CP150X	ATC
C7, C8	11 pF Chip Capacitors, B Case	100B110BCA500X	ATC
C9, C10, C21, C22	51 pF Chip Capacitors, B Case	100B510JP500X	ATC
C11, C12	6.2 pF Chip Capacitors, B Case	100B6R2BCA150X	ATC
C13	4.7 pF Chip Capacitor, B Case	100B4R7BCA150X	ATC
C14	5.1 pF Chip Capacitor, B Case	100B5R1BCA150X	ATC
C15	3.0 pF Chip Capacitor, B Case	100B2R7BCA150X	ATC
C16	2.7 pF Chip Capacitor, B Case	100B3R0BCA150X	ATC
C17	0.6 - 4.5 pF Variable Capacitor	44F3358	Newark
C18, C19	47 pF Chip Capacitors, B Case	100B470JP500X	ATC
C20	0.4 - 2.5 pF Variable Capacitor	44F3367	Newark
C29, C30	10 μF, 35 V Tantalum Chip Capacitors	93F2975	Newark
C23, C24, C25, C26	22 μF, 35 V Tantalum Chip Capacitors	92F1853	Newark
C27, C28	220 μF, 50 V Electrolytic Capacitors	14F185	Newark
Balun 1, Balun 2	Xinger Surface Mount Balun Transformers	3A412	Anaren
L1, L2	12.5 nH Mini Spring Inductors	A04T-5	Coilcraft
R1, R2	510 Ω, 1/4 W Chip Resistors		Garret
WB1, WB2, WB3, WB4	10 mil Brass Wear Blocks		
Board Material	30 mil Glass Teflon®, ε_r = 2.55 Copper Clad, 2 oz Cu	900 MHz Push-Pull Rev 01B	CMR
PCB	Etched Circuit Board	900 MHz Push-Pull Rev 01B	CMR

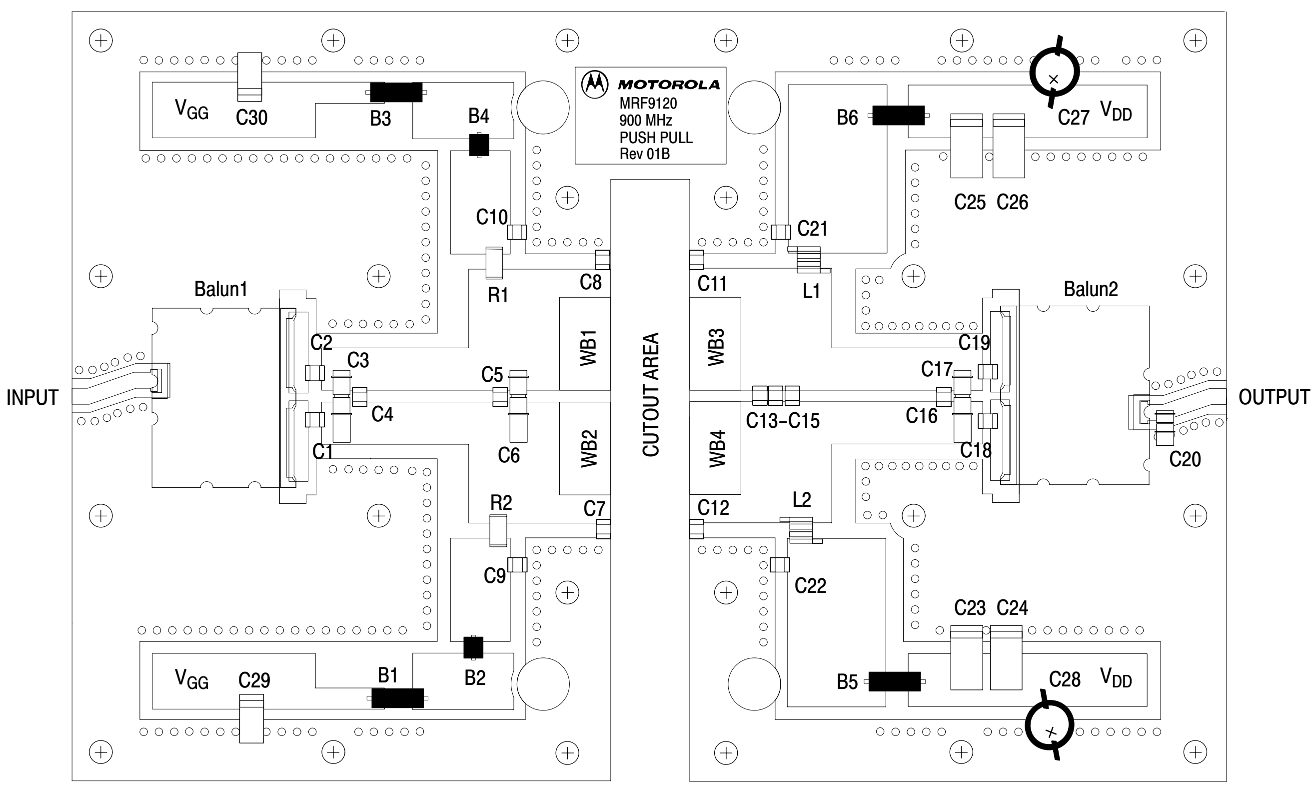


Figure 2. 865-895 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

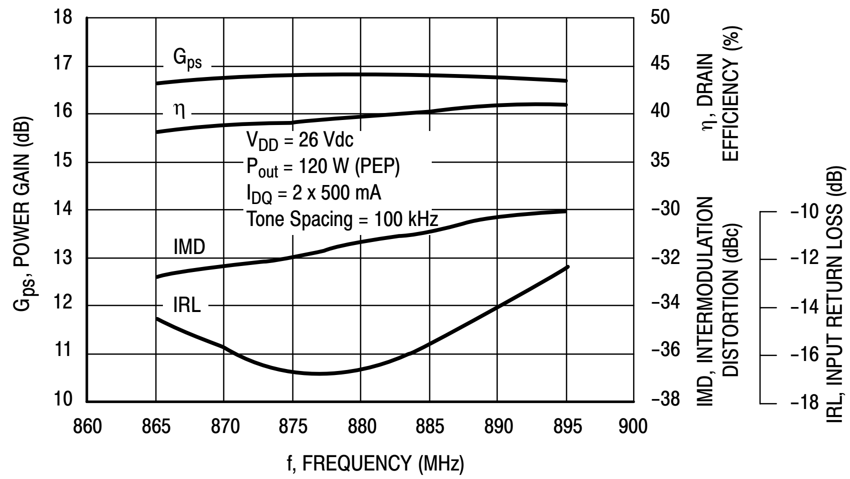


Figure 3. Class AB Broadband Circuit Performance

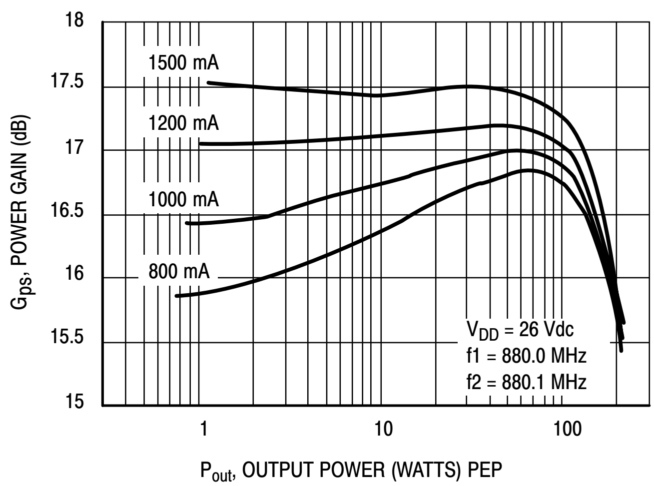


Figure 4. Power Gain versus Output Power

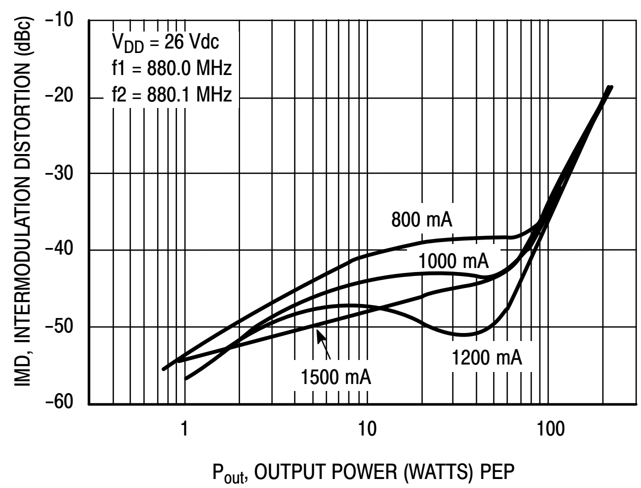


Figure 5. Intermodulation Distortion versus Output Power

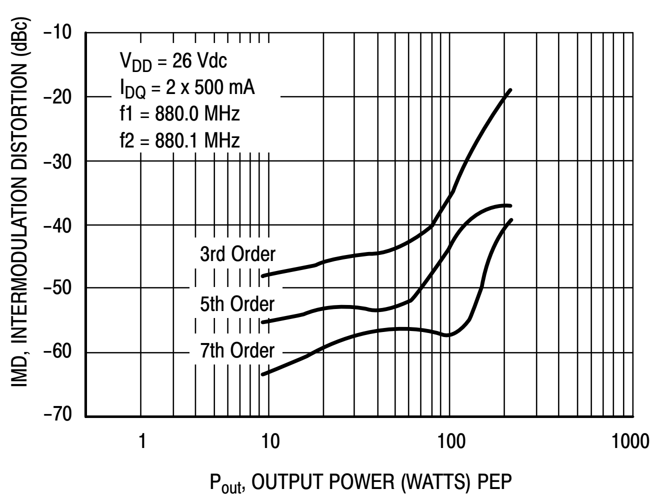


Figure 6. Intermodulation Distortion Products versus Output Power

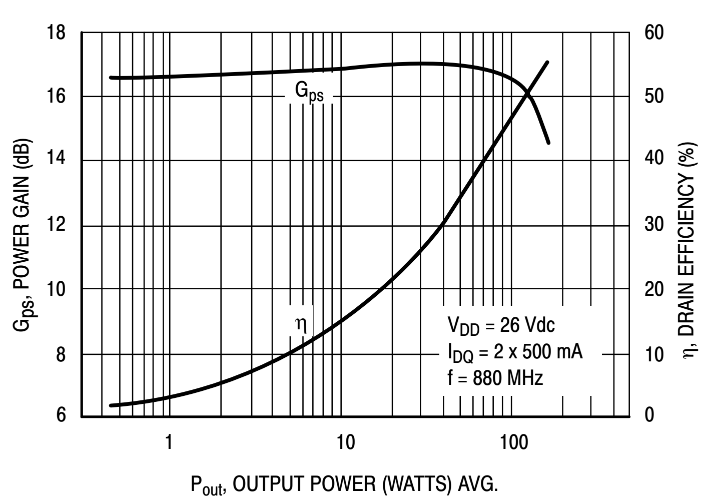


Figure 7. Power Gain and Efficiency versus Output Power

TYPICAL CHARACTERISTICS

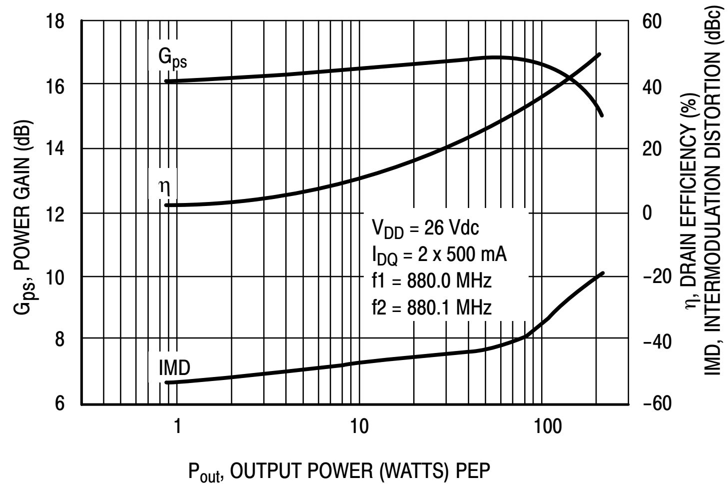


Figure 8. Power Gain, Efficiency and IMD versus Output Power

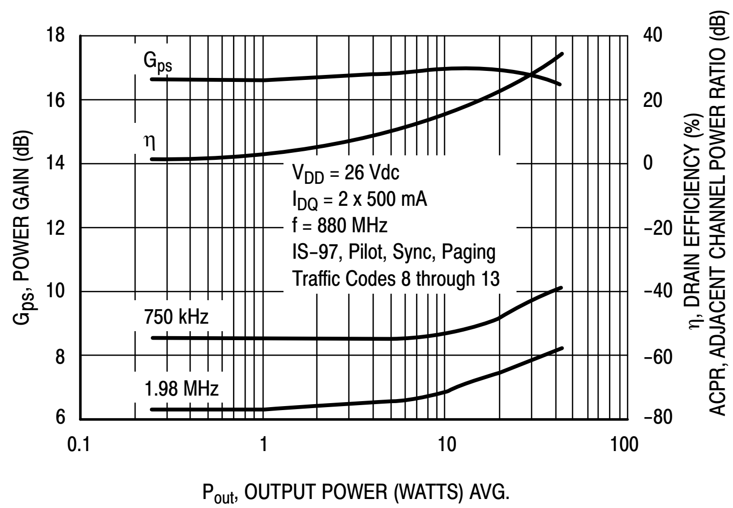
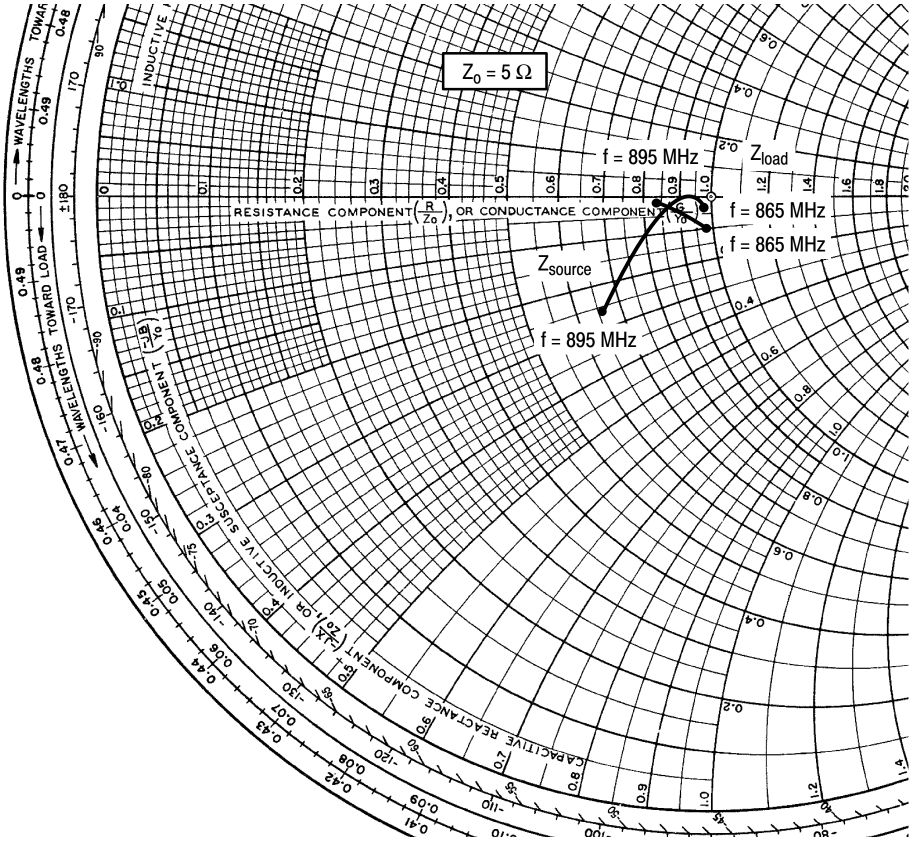


Figure 9. Power Gain, Efficiency and ACPR versus Output Power



V_{DD} = 26 V, I_{DQ} = 2 × 500 mA, P_{out} = 120 W PEP

f MHz	Z_{source} Ω	Z_{load} Ω
865	4.89 - j0.2	4.9 - j0.5
880	4.54 + j0.07	4.6 - j0.32
895	3.29 - j1.3	4.2 - j0.04

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

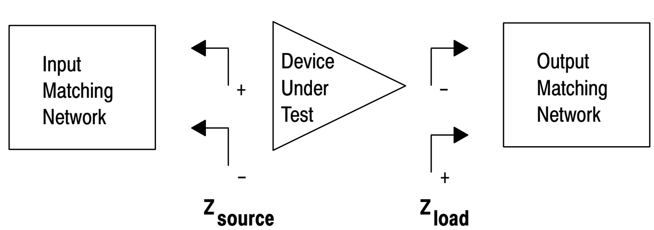


Figure 10. Series Equivalent Input and Output Impedance

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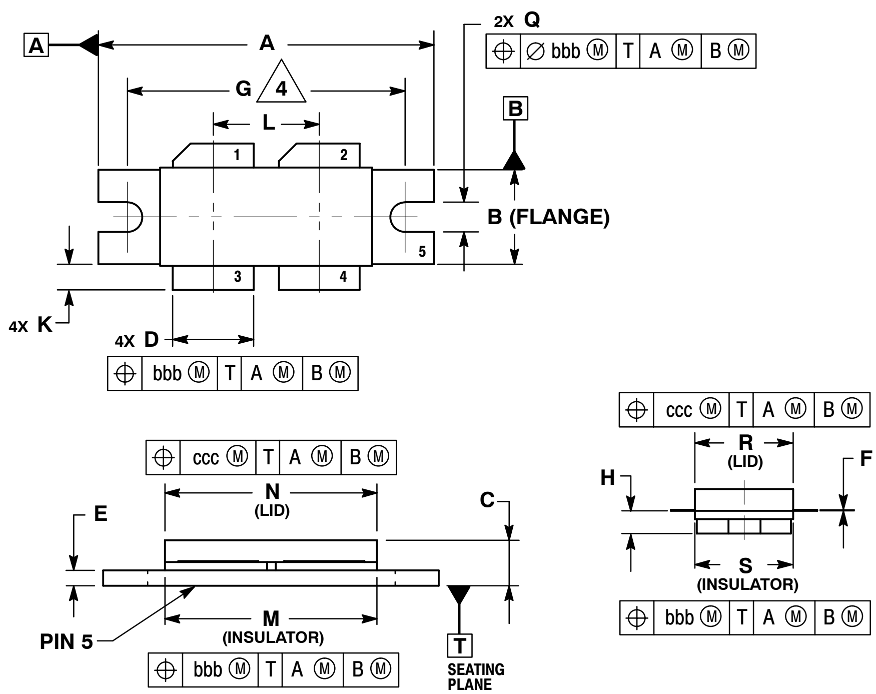
PACKAGE DIMENSIONS



NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
4. (△) RECOMMENDED BOLT CENTER DIMENSION OF 1.140 (28.96) BASED ON M3 SCREW.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.180	0.224	4.57	5.69
D	0.325	0.335	8.26	8.51
E	0.060	0.070	1.52	1.78
F	0.004	0.006	0.10	0.15
G	1.100 BSC		27.94 BSC	
H	0.097	0.107	2.46	2.72
K	0.085	0.115	2.16	2.92
L	0.425 BSC		10.80 BSC	
M	0.852	0.868	21.64	22.05
N	0.851	0.869	21.62	22.07
Q	0.118	0.138	3.00	3.51
R	0.395	0.405	10.03	10.29
S	0.394	0.406	10.01	10.31
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375B-04
ISSUE E
NI-860

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