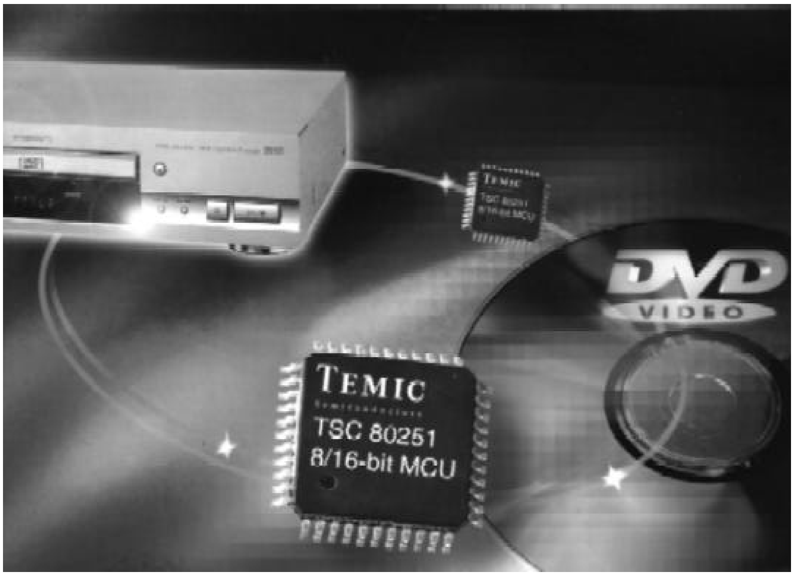
Qualification Package

TSC87251G2D / TSC83251G2D

0.5 µm SCMOS3 Technology



TSC87251G2D
0.5 µm SCMOS3
1999 October

TEMIC SEMICONDUCTORS IS AN ATMEL COMPANY

1. General Information

1.1 Product Description

Product Name:	TSC87251G2D / TSC83251G2D
Function:	8/16-bit Microcontrollers 32K EPROM / 32K ROM
Wafer process:	Z94 (SCMOS 3 NV) / Z92 (SCMOS 3)
Available plastic package types:	Wide range of packages including PLCC44, PDIP40, PQFP44, TQFP44, VQFP44
Other forms	Multiple Hermetic Packages, Die, Wafer

Locations:

Process, product development	TEMIC Semiconductors Nantes, France
Wafer plant	TEMIC Semiconductors Nantes, France
QC responsibility	TEMIC Semiconductors Nantes, France
Assembly	GATEWAY, Philippines - ASE, Taiwan CHINTEIK, Thailand - ANAM, Korea and Philippines CHIPPAC, China
Probe test	TEMIC Semiconductors Nantes, France
Final test	GATEWAY, Philippines - ASE, Taiwan ANAM, Korea and Philippines
Shipment control	GLOBAL LOGISTICS CENTER, Philippines
Quality Assurance	TEMIC Semiconductors Nantes, France
Reliability testing	TEMIC Semiconductors Nantes, France
Failure analysis	TEMIC Semiconductors Nantes, France

Product Quality Management Nantes
Signed :

Pascal LECUYER

2. Technology Information

2.1 Wafer Process Technology

2.1.1 SCMOS3 0.5um ROM Process

Process type (Name):	CMOS (SCMOS3 - Z92)
Base material:	Bulk
Wafer Thickness (final)	475 µm
Wafer diameter	150 mm
Number of masks	16
Gate oxide	
Material	Silicon dioxide
Thickness	110 A (optical - 120A electrical)
Polysilicon	
Number of layers	1
Thickness	3000 A
Metal	
Number of layers	3
Material	Ti + TiN + AlCu
Layer 1 thickness	300A + 600A + 5000A + 250A TiN
Layer 2 thickness	300A + 600A + 5000A + 250A TiN
Layer 3 thickness	300A + 600A + 6500A + 250A TiN
Passivation	
Material	SiO_2 / Si_3N_4
Thickness	3000A / 7000 A

2.1.2 SCMOS3 NV 0.5um EPROM Process

Process type (Name):	CMOS (SCMOS3 NV - Z94)
Base material:	Bulk
Wafer Thickness (final)	475 µm
Wafer diameter	150 mm
Number of masks	22
Gate oxide	
Material	Silicon dioxide
Thickness	110 A (optical - 120A electrical)
Polysilicon	
Number of layers	2
Thickness Poly1	2000 A (amorphous)
Thickness Poly2	3000 A (polysilicon)
Metal	
Number of layers	3
Material	Ti + TiN + AlCu + TiN
Layer 1 thickness	300A Ti + 600A TiN + 5000A AlCu+ 250A TiN
Layer 2 thickness	300A Ti + 600A TiN + 5000A AlCu+ 250A TiN
Layer 3 thickness	300A Ti + 600A TiN + 6500A AlCu+ 250A TiN
Passivation	
Material	SiO_2 / Nitride Oxide
Thickness	3000A /15000 A

2.2 Product Design

Die size	For TSC87251G2D: 17.84 mm^2 (4250 µm * 4400 µm)
	For TSC83251G2D: 17.84 mm^2 (4250 µm * 4400 µm)
Pad size	84 µm * 84 µm
Logic Effective channel length	0.42 µm
Gate poly width	0.5 µm
Gate poly spacing	0.6 µm
Metal 1 width	0.6 µm
Metal 1 spacing	0.7 µm
Metal 2 width	0.8 µm
Metal 2 spacing	0.7 µm
Metal 3 width	0.8 µm
Metal 3 spacing	0.7 µm
Contact size	0.6 µm
Via 1 size	0.6 µm
Via 2 size	0.7 µm

2.3 Package Technology

2.3.1 Package description

Depending on the customer’s need. For information, the following data concern the PLCC 44.

Package weight	2.34g
Chip separation method	Sawing
Lead frame	
Material	Cu
Thickness	10 mils
Size	270*270 mils^2
Lead plating	Electroplated Sn/Pb 85/15
Die attach	
Material	Silver epoxy
Type	Ablestick 84-1 LMIS
Wire bonding	
Material	Gold
Diameter	33um

Method	Thermosonic
Molding	
Material	Sumitomo EME 6300HS
Flammability rating	UL94V-0
Marking	
Method	Printed ink
Coding example	T *optional special customer marking* TSC83C51RB2-MCA © INTEL 80,82 Date-code Lot nbr
Dry packing	No
Tube packed	
Primary	Tube
Material	Antistatic PVC
Number per unit	27
Secondary	Box
Material	Cardboard
Number per unit	972
Labeling (minimum)	Device type, Quantity, Date Code, Production code
Bar coding	Code 39 to EIA-556-A

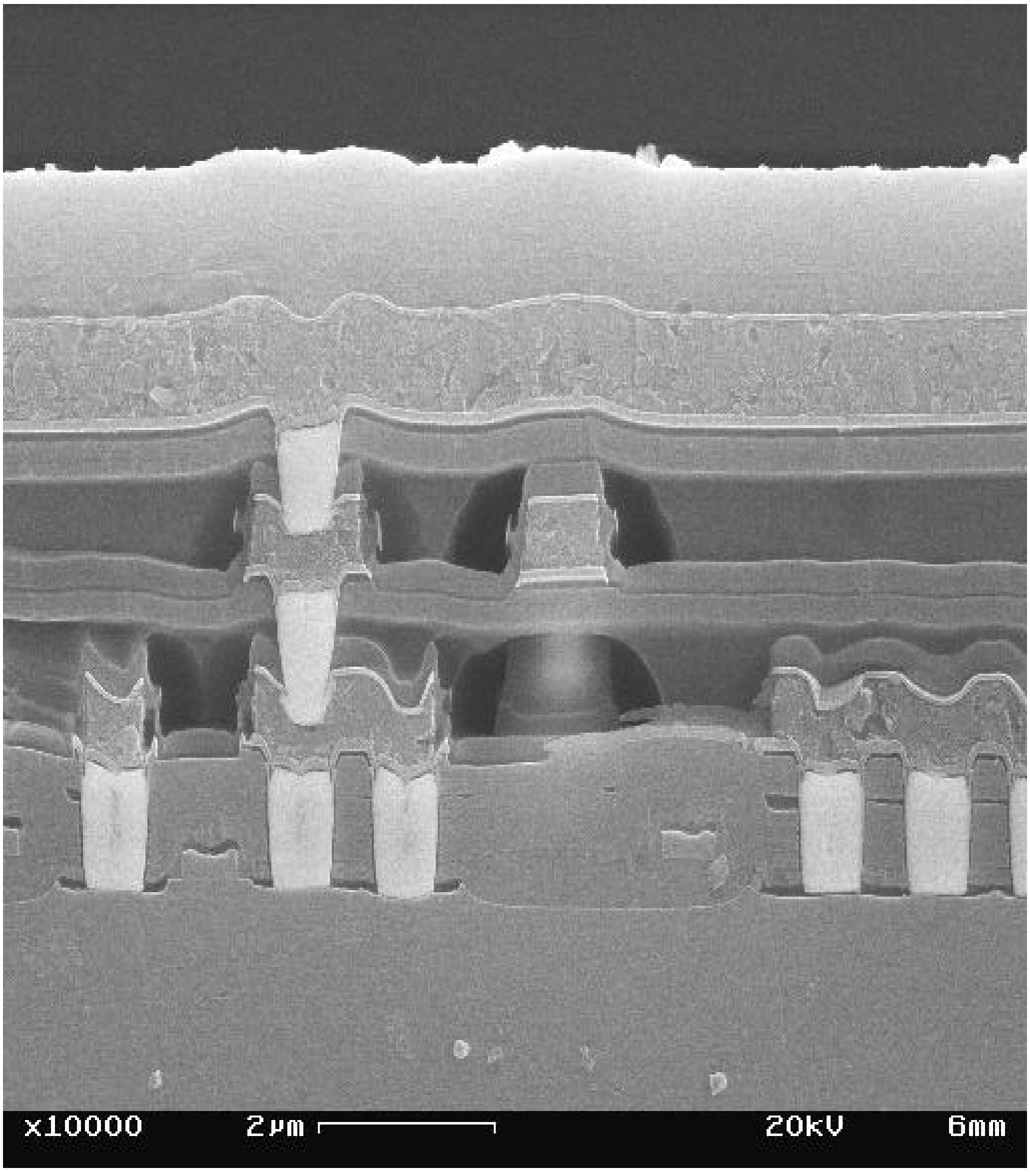
2.3.2 Other available packages

PQFP, PDIP, CQFP, CERDIP	No dry pack required
TQFP, VQFP	Dry pack required

2.4 Test

Probe equipment	SCHLUMBERGER ITS9000 / S15
Probe temperature	85°C
Test equipment	SENTRY 15
Test temperature	
Commercial range	25°C
Industrial range	25°C and optional 85°C
Automotive range	25°C, 125°c and optional -40°c

2.5 Device Cross Section



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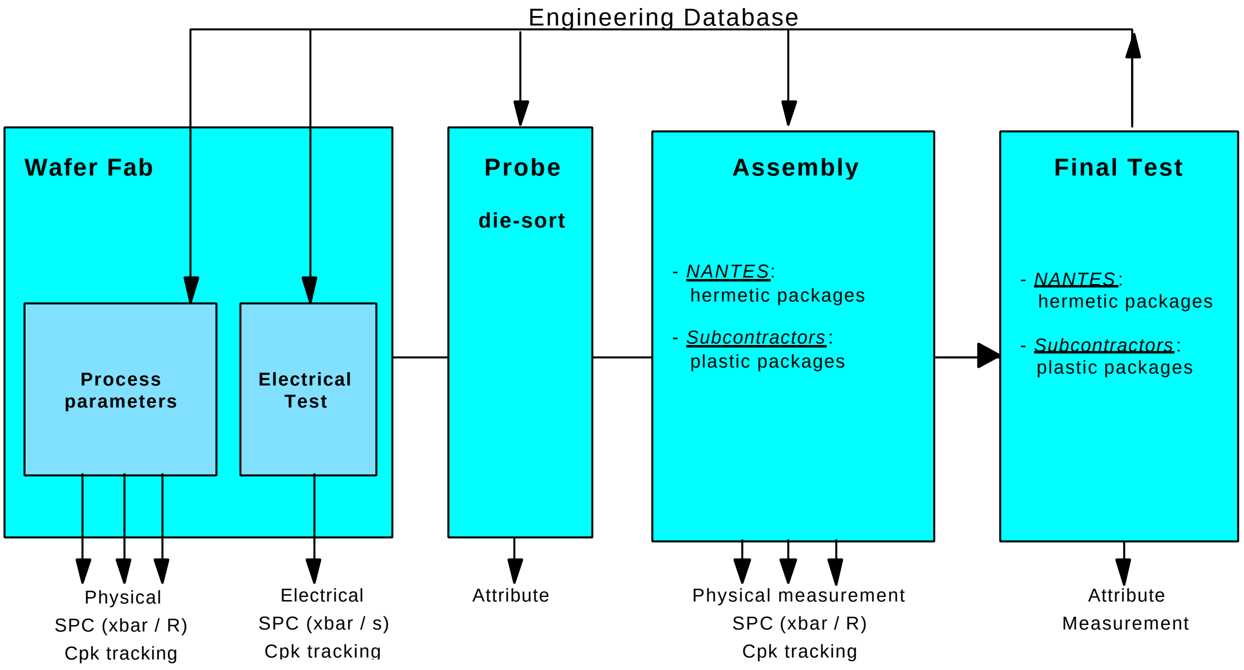
Final Z92 Cross Section

2.6 Wafer Process Control

All the inspections and controls are defined as a process step in the production management software, and are led by using a centralized SPC software. PC system could be summarized as follows:

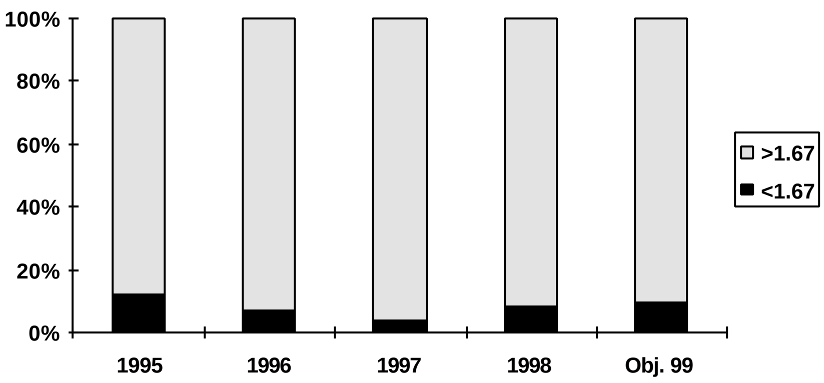


Critical process parameters are identified by using F.M.E.A. and other advanced tools.

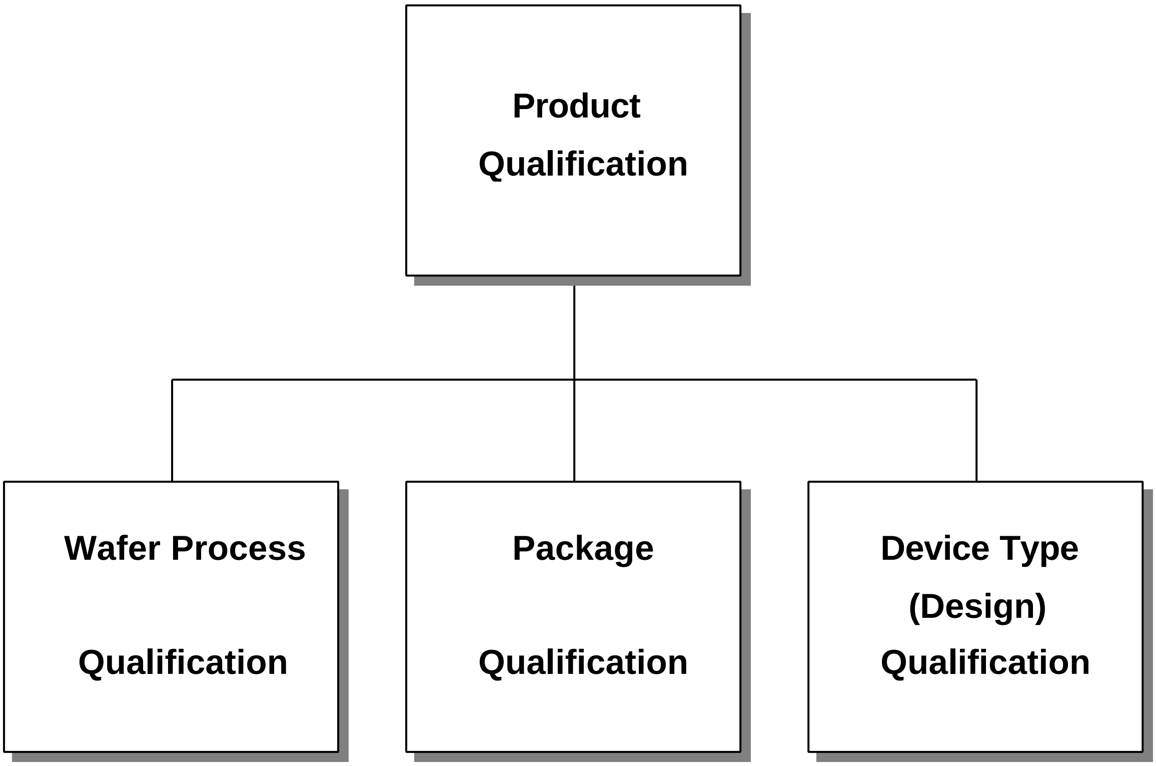
Those parameters are followed in real time with the SPC methodology and their capability is measured and monthly reported in the Operation Review.

For end 1999, the Cpk target is the following:

% of all parameters per Cpk categories



3. Qualification



All product qualifications are split into three distinct steps as shown above. This same procedure is also used to qualify a change. Before a product is released for use, it must have been manufactured using a qualified wafer and package process. Before a device is released for production processing, it must also have successfully completed its required specific qualification.

The standard tests which are used for this procedure are shown in the section **"Qualification Flow"** .

3.1 Change Procedure

All changes are controlled by PCN (Product Change Notice). All major changes are notified to the customers affected by the change.

A major change is defined as a change that requires evidence of no electrical, mechanical impact on the product, or a change in the specification or marking of the product or packing. The list of changes usually considered as major is detailed hereafter:

1	**General Major Changes**
1-1	Manufacturing line
1-2	Sequence of fabrication process cycle
1-3	Material type
1-4	Electrical parameter
1-5	External physical dimension
1-6	Die size

2	**Changes specific to wafer fabrication area**
2-1	Doping method
2-2	Gate oxide formation method
2-3	Equipment change
2-4	Layer Thickness
2-5	Module dimensions

3	**Changes specific to to assembly process area**
3-1	Sawing method
3-2	Die attach
3-3	Wire interconnect tools
3-4	Molding process
3-5	Tinning method

4	**Changes specific to test area**
4-1	Specification limit
4-2	Test coverage reduction
4-2	Product identification
4-3	Final conditioning

3.2 Qualification Flow

General Requirements for Plastic packaged CMOS IC

Standard	Test Description	Qualification type (acceptance)
MIL-STD 883D Method 1005	**Electrical Life Test (Early Failure Rate)** 12 hours 150°C (Tj) 5.75V	Device (1/2000 12h)
MIL-STD 883D Method 1005	**Electrical Life Test (Latent Failure Rate)** 1000 hours 150°C 5.75V Dynamic or Static	Device (0/100 500h)
MIL-STD 883D Method 3015.7	**Electrostatic Discharge HBM** +/-2000v 1.5kOhm/100pF/3 pulses	Device (0/3 per level)
JEDEC 78	**Latch up** 50mW power injection 125°C	Device (0/10)
MHS PAQA0046	**NV Memory Dataretention** High Temperature Storage 165°C	Device (0/50 500c)
MIL-STD 883D Method 1010	**Temperature Cycling** 1000 cycles -65°C/150°C air/air	Die and Package (0/50 500c)
MHS PAQA0184	**Pressure Pot after Mounting Stress** 168 hours 130°C/85%RH	Die and Package (0/50 168h)
EIA JESD22-A101	**85/85 Humidity Test** 1000 hours 85°C/85%RH	Die and Package (0/50 500h)
EIA JESD22-A110	**HAST** 336 hours 130°C/85%RH/5.5V	Die and Package (0/50 168h)
EIA JEDEC J-20-STD	**Moisture Sensitivity Ranking** Infra Red Stress 220°C/235°c/3 times	Package (0/10 per class)
MIL-STD 883D Method 2003	**Solderability**	Package (0/3)
MIL-STD 883D Method 2015	**Marking Permanency**	Package (0/5)

3.3 Wafer Process Qualification

3.3.1 Process Module Reliability

This chapter contains all the information relative to the reliability of the SCMOS3 technology. Results presented in the following sections concern the reliability of the basic process steps that build up the technology.

3.3.1.1 Hot carrier qualification

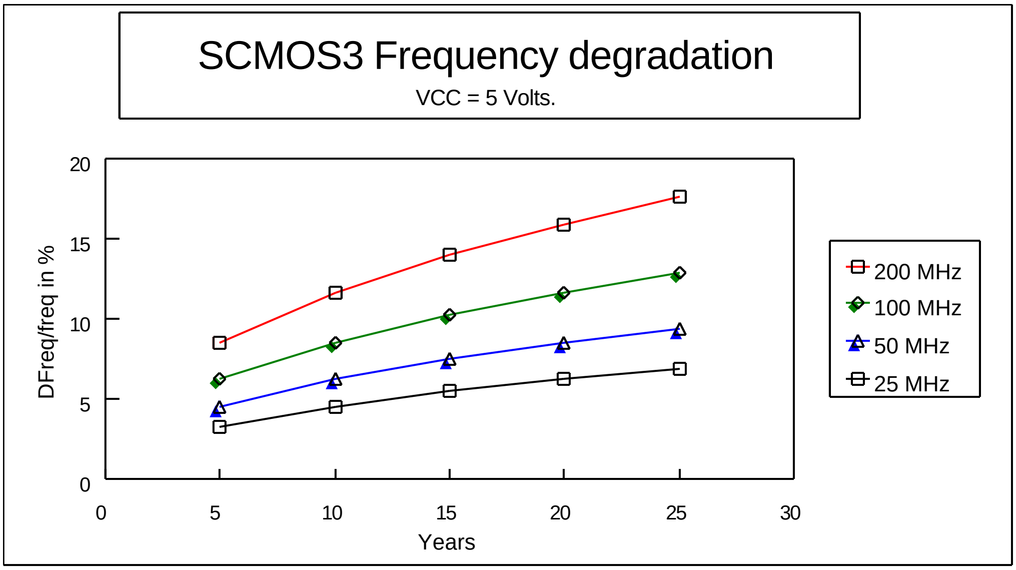
STATIC NMOS DEGRADATION

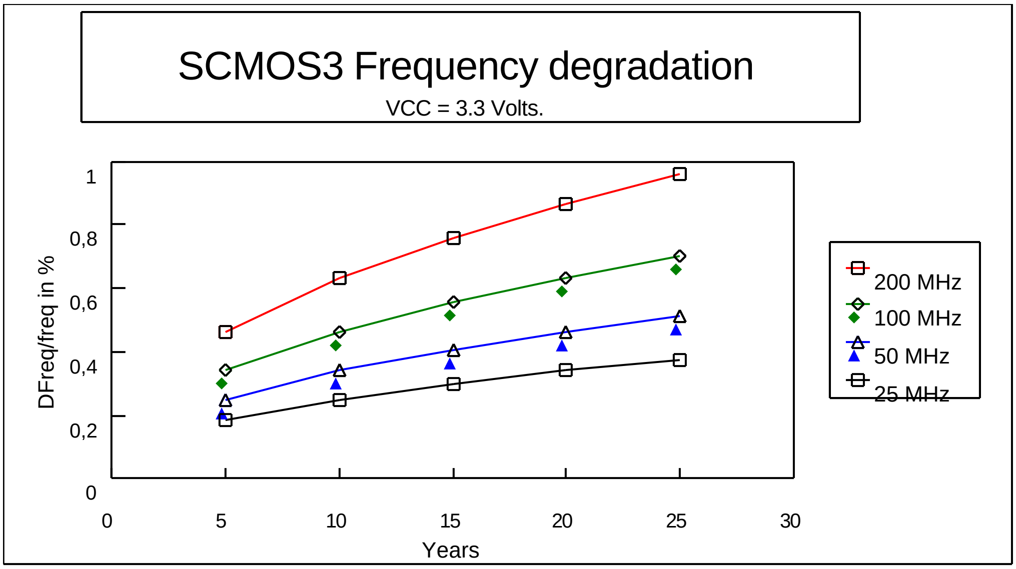
Channel length in µm	**0.5**	**0.55**	**0.6**	**0.65**	**0.7**	**0.5**
Process corner	Fast	Fast	Fast	Fast	Fast	Typical
Substrate current in µA/µm VD=5.5v, VG=2.25v	17	15	13.4	12.1	11.1	14.7
Substrate current in µA/µm VD=3.6v, VG=1.6v	0.35	0.3	0.25	0.22	0.2	0.3
Lifetime in seconds for 10% shift of Gm at VD=5.5v	3.2e3	3.7e3	4.2e3	4.7e3	5.2e3	3.8e3
Lifetime in seconds for 10% shift of Gm at VD=3.6v	8e7	10e7	12e7	14e7	16e7	10e7

STATIC PMOS DEGRADATION

Channel length in µm	**0.5**	**0.55**	**0.6**	**0.65**	**0.7**	**0.5**
Process corner	Fast	Fast	Fast	Fast	Fast	Typical
Substrate current in µA/µm VD=5.5v, VG=2.25v	0.31	0.28	0.25	0.22	0.21	0.24
Substrate current in µA/µm VD=3.6v, VG=1.25v	2.3e-3	1.9e-3	1.6e-3	1.4e-3	1.1e-3	1.6e-3
Lifetime in seconds for 10% shift of Gm at VD=5.5v	2.7e4	3.1e4	3.5e4	3.9e4	4.3e4	3.5e4
Lifetime in seconds for 10% shift of Gm at VD=3.6v	2e7	2.5e7	3e7	3.8e7	4.6e7	3.2e7

EXPERIMENTAL RESULTS IN DYNAMIC MODE: hot carrier degradation effects on inverter propagation time have been measured on oscillators running at 75 MHz at 7v and 6.5v. Accelerator factor in voltage is then carried out and expected degradation laws at 5v and 3.3v derived. The following graphs show the frequency degradation of oscillators running at 5v and 3.3v.


SCMOS3 Frequency degradation
VCC = 5 Volts.
DFreq/freq in %
0
5
10
15
20
0
5
10
15
20
25
30
Years
200 MHz
100 MHz
50 MHz
25 MHz


SCMOS3 Frequency degradation
VCC = 3.3 Volts.
DFreq/freq in %
0
0,2
0,4
0,6
0,8
1
0
5
10
15
20
25
30
Years
200 MHz
100 MHz
50 MHz
25 MHz

3.3.1.2 Electromigration

Characterization

Stresses of electromigration are achieved for 1000 hours on 32 packaged metal line running on flat with a current density of $2x10^6$ A/cm2 at a temperature of 200°C. Lines are declared to be failed for a shift of the initial resistance by 20%. Results are summarized in the table below.

Level	W/L/T(1)	Structure	Failures
Metal1	**2/2000/0.50**	**Ti/TiN/AlCu/TiN**	**No**
Metal2	**2/2000/0.50**	**Ti/TiN/AlCu/TiN**	**No**
Metal3	**2/2000/0.70**	**Ti/TiN/AlCu/TiN**	**No**

(1)W/L/T=Width/Length/Thickness of the metal line in microns

Lifetime projection

The objective of reliability is to reach less than 10FIT on metal line within 10 years at a temperature of 150°C. As no failures have been found at 1000 hours in the above stress conditions a lifetime projection in FIT is meaningless.
However, assuming for AlCu metalization an activation energy in temperature Ea of 0.60eV and an activation in current with a power-law coefficient n of 2, the current density which guarantees no failures within 10 years at 150°C can be extrapolated.
With these assumptions the projected current density for no failures at 150°C within 10 years is calculated as $5x10^5$A/cm2 which is much higher than the current density of $2x10^5$A/cm2 specified in the design rules.

3.3.1.3 Time Dependent Dielectric Breackdown

QBD MEASUREMENT:

The critical charge, supported by the thin oxide and related to the extrinsic and intrinsic defects, is measured on TOX/P- and TOX/N- capacitors. The tested capacitor areas are varying from 4e-4 to 5e-2 cm2. Two types of capacitors with poly overlaping the field oxide (DEC) and poly non overlaping the field oxide (INC) are measured. The distributions have been obtained from 750 measurements for each area and type of capacitors on 10 different lots.

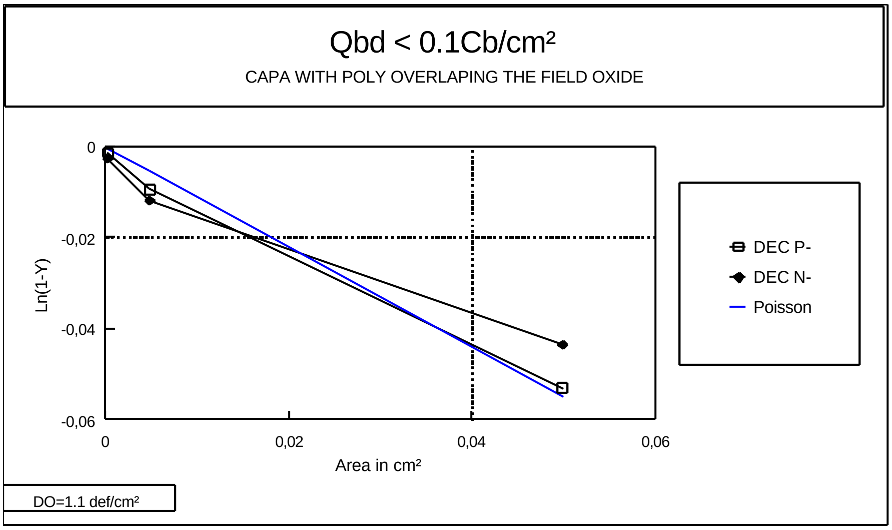
Extrinsic defects:

The two graphs here after represent the % of failures vs area for Qbd below or equal to 0.1 Cb/cm2. The law of Poisson is used to determine the D0 defect density of the extrinsic defects:

Y=1-exp(-Area * DO)

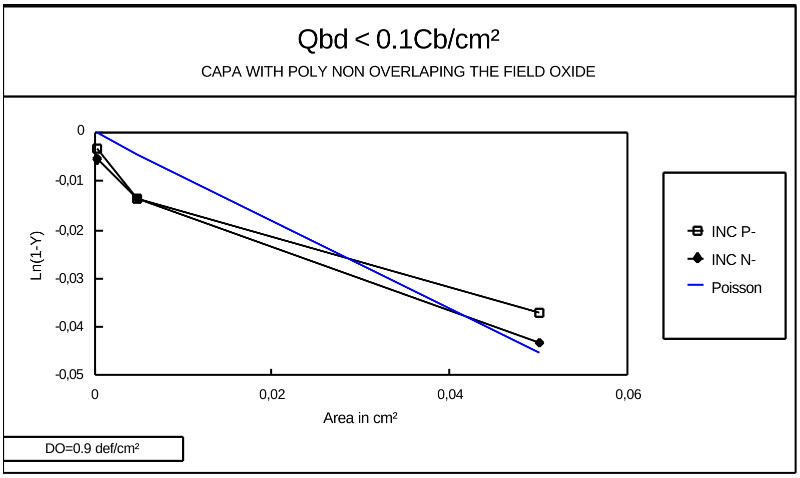
Poly overlaping the Field oxide on Tox/P- and Tox/N-:

The DO is found to be 1.1 def/cm2. This result is in agreement with the goal for D0 of 1 def/cm2.



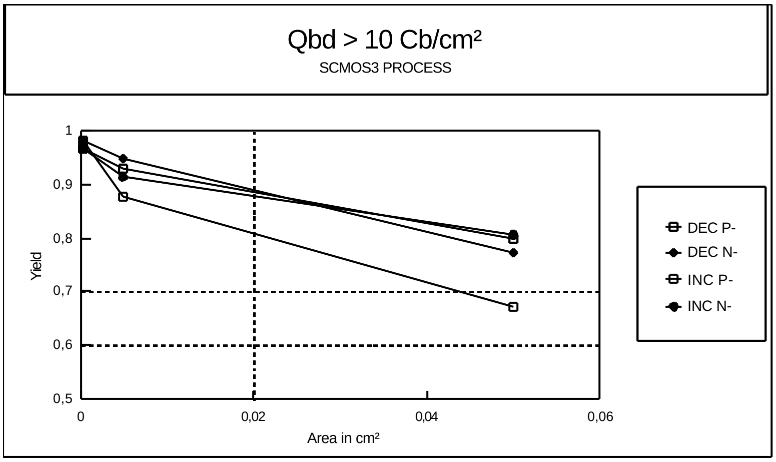
Poly non overlaping the Field oxide on Tox/P- and Tox/N-:

The DO is found to be 0.9def/cm2. This result is in agreement with the goal for D0 of 1 def/cm2.



Intrinsic defects:

The graph here after represents the percentage of failure for a Qbd > 10 Cb/cm² vs the area. The worst case given by the bigest capacitors shows that 67% of the total distribution has a Qbd > 10 Cb/cm². This result guarantees a good reliability behaviour. The critical charge, supported by thin oxide and related to the extrinsic defects, is measured on TOX/P- capacitors of 42570um2 and TOX/N- capacitors of 85140um2. Following are the average results obtained on recent lots from a distribution of about 60 sites per wafer. The minimum specification limit is 10C/cm2.



Conclusion:

The QBD results demonstrate high reliability level of SCMOS3 thin oxide.

3.3.2 Z92 Wafer Process Qualification Results

This section summarizes the cumulated reliability data of 0.5um microcontrollers ROM technology.

Lots	Device Type	Test Description	Step	Result	Comment
Z27746A	TSC251G2D	EFR Dynamic Life Test	12h	3/2661	Poly particle Metal3 defect
		LFR Life Test	500h	0/100	
			1000h	0/100	
Z27735A	TS80C32X2	EFR Dynamic Life Test	12h	11/11712	Contacts alignment
Z29249					
Z29683C		LFR Life Test	500h	0/699	
Z29936			1000h	0/699	
Z27300A	TS83C51RC2	EFR Dynamic Life Test	12h	5/7318	Passivation scratch
Z27880A					Poly particle
Z28109A		LFR Life Test	500h	0/200	Silicon breakdown
			1000h	0/200	
Z26274A	TS83C51RX2	EFR Dynamic Life Test	12h	3/2238	
Z26407					
Z27291A		LFR Life Test	500h	0/173	
			1000h	0/173	
Global	All products	EFR Dynamic Life Test			
		Commercial / Industrial	12h	22/23929	919 ppm (828 ppm / 10 mm2)
		Automotive (1)	24h	0/3564	0ppm
			168h	0/1172	
		LFR Life Test	500h	0/1172	4.7 fit
			1000h	0/1172	(3.0 fit / 10mm2)

Note (1): The additional operations included in the automotive backend flow allow to reduce significantly the Early Life Failure Rate. As long as needed to achieve the Automotive Quality Assurance requirements, these operations may be any of those described hereafter:

- Statistical wafer sort
- Accelerated Dynamic Burn-in at probe
- Probe critical parameters 3 sigma sort
- Part Average Testing
- Dynamic Burn-in of products
- Other equivalent methods

3.3.3 Z94 Wafer Process Qualification Results

This section summarizes the cumulated reliability data of 0.5um microcontrollers EPROM technology.

Lots	Device Type	Test Description	Step	Result	Comment
Z27314A Z27748	TSC87251G2D	EFR Dynamic Life Test	12h 24h	4/3772 0/360	Poly bridging, Interlayer oxide defect, functional not identified, metal 2 photo etch bridging
		LFR Life Test	500h	1/150	
Z28233C	TSC87C51RB2	EFR Dynamic Life Test	12h 24h	1/1663 0/323	Functional not identified
		LFR Life Test	500h 1000h	0/100 0/97	
Z28090B Z28987 Z29142 Z29311D Z29568B	TSC87C51RC2	EFR Dynamic Life Test	12h 24h	8/11533 0/1284	Poly particle Contact misalignment Capacitor oxide defects
		LFR Life Test	500h 1000h	0/500 0/500	
Z28303C	TSC87C51RD2	EFR Dynamic Life Test	12h 24h	2/953 0/324	Poly particle
		LFR Life Test	500h 1000h	0/100 0/100	
Z28430A	TSC87C52X2	EFR Dynamic Life Test	12h 24h	2/2333 0/297	Functional not identified
		LFR Life Test	500h 1000h	0/100 0/100	

Global	All products	EFR Dynamic Life Test Commercial / Industrial	12h	17/20254	839 ppm (705 ppm / 10mm2)
		Automotive (1)	24h 168h	0/2588 0/950	0ppm
		LFR Life Test	500h 1000h	1/950 0/797	14.2 fit (11.6 fit / 10mm2)

3.4 Package Qualification

This section summarizes the initial package qualification data of TSC87251G2D and TSC87251G2D products in PLCC44.

Lots	Device Type	Test Description	Step	Result	Comment
Z27314A	TSC87251G2D PLCC44	85/85 Humidity	500h 1000h	0/50 0/50	
		Moisture Sensitivity Ranking	L1	0/10	Pass level 1 of J-20-STD
		HAST after Soldering Stress	15c 168h	0/50 0/50	
Z27746A	TSC83251G2D PLCC44	Thermal Cycles	500c 1000c	0/50 0/50	
		HAST after Soldering Stress	15c 168h	0/50 0/50	

3.5 Device Qualification

This section presents the qualification results of TSC87251G2D/TSC83251G2D devices.

Lots	Device Type	Test Description	Step	Result	Comment
Z27314A	TSC87251G2D PLCC44	EFR Dynamic Life Test	12h 24h 168h	2/1978 0/360 0/150	Interlayer oxide defect Polysilicide particle
		LFR Life Test	500h 1000h	1/150	Metal 2 photo etch bridging
		High Temp. Retention	500h 1000h	0/50 0/50	
Z27746A	TSC83251G2D PLCC44	EFR Dynamic Life Test	12h 24h 168h	3/2661 0/211 0/100	Polysilicide particle Metal 3 defect
		LFR Life Test	500h 1000h	0/100 0/100	

Lots	Device Type	Test Description	Step	Result	Comment
Z26629	TSC87251G2D	ESD HBM	2000V	3/3	Class 1 of MIL883
		Latch up Overvoltage Power injection	 10V 50mW	 0/5 0/5	 Latch-up free
Z27746	TSC83251G2D	ESD HBM	2000V 3000V	0/3 0/3	Class 2 of MIL883
		Latch up Overvoltage Power injection	 10V 50mW	 0/5 0/5	 Latch-up free

Comments:

No reject observed during package qualification tests.

One reject in LFR, but physical analysis demonstrated the failure was wafer process dependant and not related to the device itself. As a consequence it was not charged for device qualification.

3.5.1 Failure Mechanisms and Corrective Actions

As part of TEMIC continuous improvement policy, all defects are analysed. For all failure mechanisms identified, root causes ranked regards number of occurencies and criticity are investigated and addressed by corrective actions.

Failure Mechanism	**Root Cause**	**Corrective Action**	**Date**	**Effect**	**Check of Efficiency**
56% Contacts misalignment	RTA drift	Upgrade of RTA equipment	06/99	reduce alignment scattering	Visual inspection, yield - 07/99
26% Poly defects	Defect density at Poly level	# Hard mask : replacement of PR Titane mask by masking buffers during Ti deposition for	10/98	Reduction of defect density at Poly level	Yield EFR - 12/98
		# polysilicideBARC (Bottom Anti-Reflective Coating)		Improve Poly dimension control	Yield EFR - 12/98
		# PR strip optimization	03/99	Defect density reduction	EFR - 05/99
6% Metal particles	PR strip process	# PR strip method optimized # Equipment upgrade (Semitool)	03/99 07/99	Reduction of the defect density	Yield – EFR 05/99
6% Passivation	Marginal				
6% Silicon breakdown	Marginal				

3.5.2 Qualification status

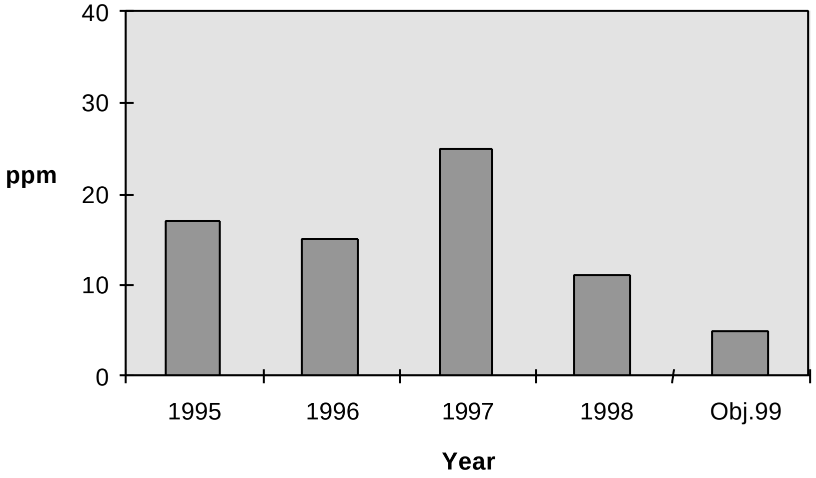
The 0.5um logic wafer process was qualified on 1997 September. The qualification was extended to OTP microcontrollers (SCMOS3 NV) process on 1999 April.

The TSC83251G2D was qualified on 1999 January, and OTP version TSC87251G2D was full qualified on 1999 April.

3.6 Outgoing Quality and Reliability

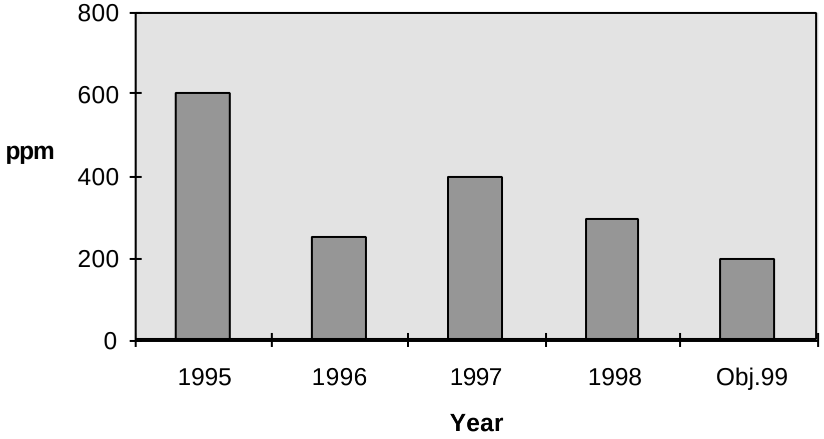
3.6.1 AOQ (Average Outgoing Quality)

The AOQ is measured following 100% test by sampling outgoing product. The results of this inspection are recorded in ppm (parts per million) using the method defined in JEDEC 16. The figures below cover the last years for both the subject and structurally similar products.



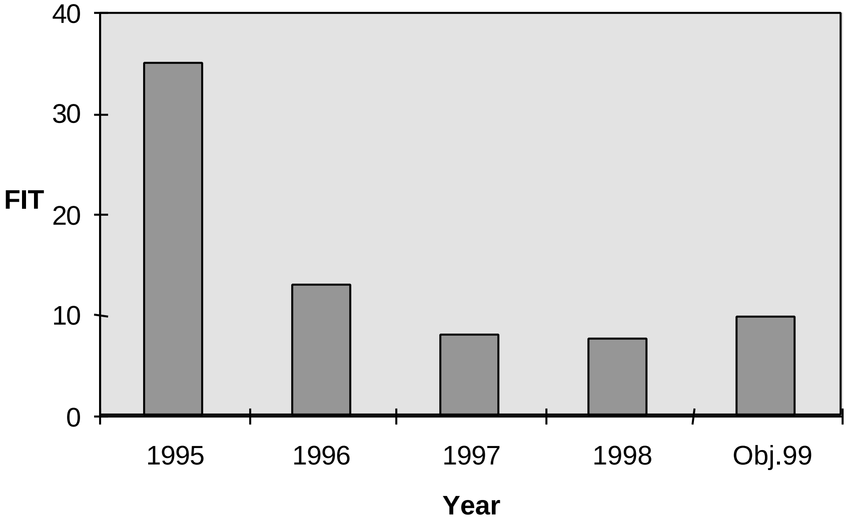
3.6.2 EFR (Early Failure Rate)

The EFR is measured on a sample of devices by operating them at an elevated temperature and measuring the number which fails to meet specification after 12 hours at 150°C. The figure is expressed in terms of ppm.



3.6.3 LFR (Latent Failure Rate)

The LFR is measured by operating devices at elevated temperatures for 1000 hours and measuring the failure rate. Using the Arrhenius law, the expected failure rate at a operating temperature of 55°C is calculated using an activation Energy of 0.6 eV with a confidence level of 60%. This is expressed in units per billion hours (FIT). The figures given are for the subject and structurally similar products.



4. User Information

4.1 Soldering Recommendations

For DRY PACKED products, TEMIC recommends to strictly follow the procedure described hereunder:

- Dry packed products must not be stored more than 1 year at 40°c - 90%rh (worst storage conditions assumed)

- A longer storage period is allowed taking into account the following conditions: 5 years max at 25°c (+/-5°c) - 50%rh

- From opening of the packs, the product must be assembled within 48 hours. (worst in-process storage condition assumed: 30°c - 60%rh)

- If they cannot be soldered within this time period, then the pieces must be dryed at 125°c for 24 hours. Only one drying is allowed.

- Max relative humidity allowed in the bag is 20% (readable on the indicator inside the bag). If this value is reached, then the parts must be dryed at 125°C for 24 hours before mounting.

- For high sensitive products, the delay between pack openning and assembly is reduced to 6 hours (Level 6 of JEDEC 22-A112). In this case, a warning printed on each pack advises the user of this restriction.

4.2 DRY PACK Ordering rules

TEMIC qualification procedure allows to classify products according to JEDEC 22-A112 and to determine the convenient conditioning for safe customer use.

Nevertheless, even if the product is not classified as moisture sensitive, it is possible (for example if storage conditions are not properly controlled) to order product with a Dry Pack.

4.3 ESD caution

The user must protect components against EOS and ESD damages by grounding personal and workstations.

5. Environmental Information

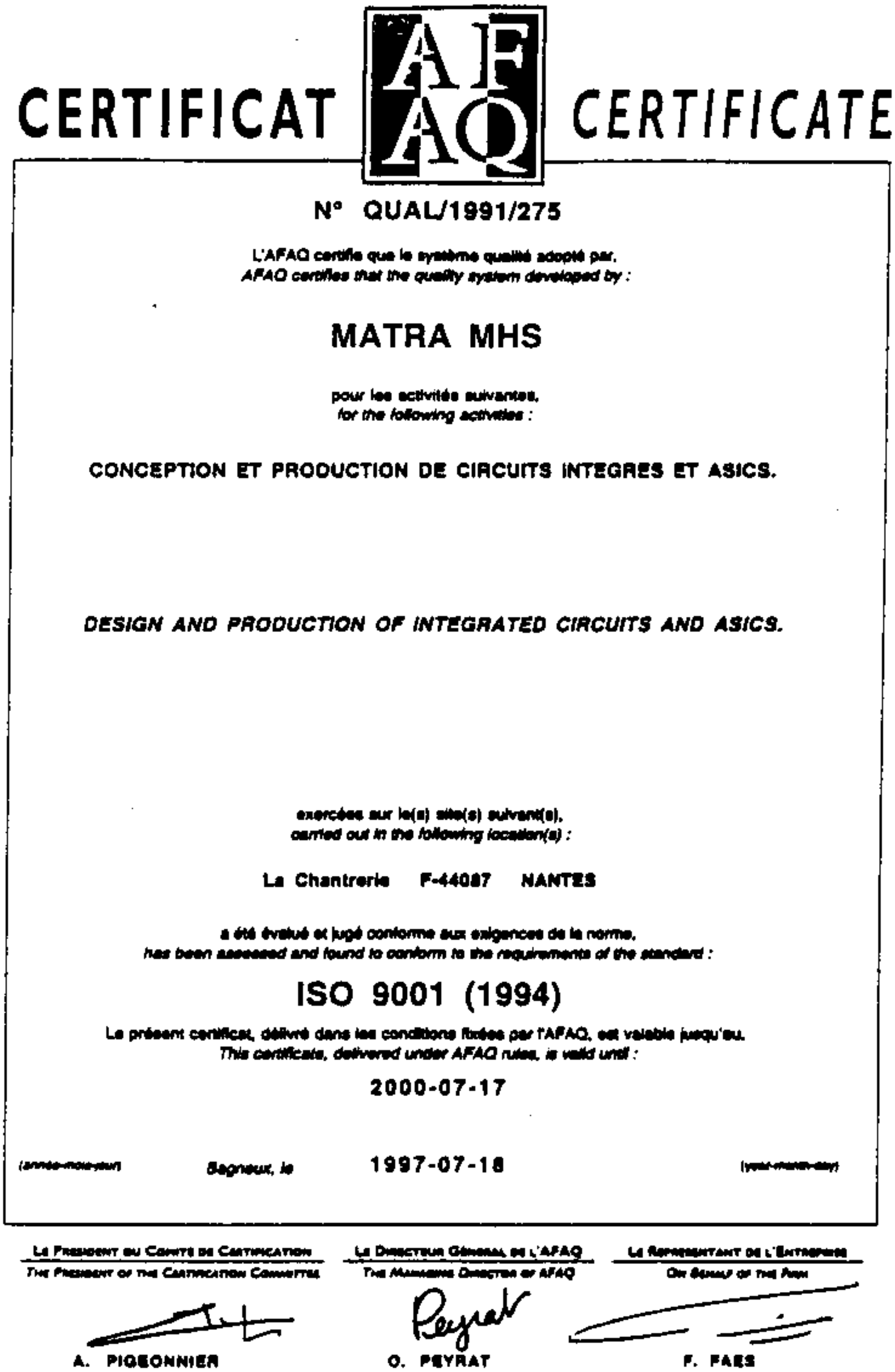
The TEMIC Environmental Policy aims are :

- Reducing the use of harmful chemicals in its processes
- Reducing the content of harmful materials in its products
- Using re-cyclable materials wherever possible
- Reducing the energy content of its products

As part of that plan, Ozone Depleting Chemicals are being replaced either by TEMIC MHS or its sub-contractors' process.

6. Other Data

6.1 ISO9001 Approval Certificate



CERTIFICAT AF AQ **CERTIFICATE**

N° QUAL/1991/275

L'AFAQ certifie que le système qualité adopté par,
AFAQ certifies that the quality system developed by :

MATRA MHS

pour les activités suivantes,
for the following activities :

CONCEPTION ET PRODUCTION DE CIRCUITS INTEGRES ET ASICS.

DESIGN AND PRODUCTION OF INTEGRATED CIRCUITS AND ASICS.

exercées sur le(s) site(s) suivant(s),
carried out in the following location(s) :

La Chantrerie F-44087 NANTES

a été évalué et jugé conforme aux exigences de la norme,
has been assessed and found to conform to the requirements of the standard :

ISO 9001 (1994)

Le présent certificat, délivré dans les conditions fixées par l'AFAQ, est valable jusqu'au,
This certificate, delivered under AFAQ rules, is valid until :

2000-07-17

(année-mois-jour) *Bagneux, le* **1997-07-18** *(year-month-day)*

Le Président du Comité de Certification *The President of the Certification Committee*	Le Directeur Général de l'AFAQ *The Managing Director of AFAQ*	Le Représentant de l'Entreprise *On Behalf of the Firm*
	Peyrat	
A. PIGEONNIER	**O. PEYRAT**	**F. FAES**

6.2 Databook Reference

The datasheet is available upon request to sales representative, or on TEMIC Semiconductors web site: http://www.temic-semi.com

6.3 Address Reference

All inquiries relating to this document should be addressed to the following:

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Or Direct contact
Pascal LECUYER
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7. Revision History

Issue	Modification Notice	Application Date
0	Initial Product Qualification Report	1999 October

Remarks:

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