

# JLC1562B

## I<sup>2</sup>C Bus I/O Expander

The JLC1562B facilitates easy I<sup>2</sup>C Bus expandability. Multiple devices (up to 8 on the same I<sup>2</sup>C Bus) are easily added as each device has its own selectable 3-bit address. The JLC1562B provides an 8-bit bidirectional input/output port and 6-bit resolution Digital to Analog Converter. The voltage on pins P0–P4 is compared with a controllable threshold voltage and the results are readable through the I<sup>2</sup>C Bus.

I<sup>2</sup>C Bus interface pins SDA, SCL and A0–A2 are; Serial Data, Serial Clock and Device Address respectively. External interface pins are P0–P7 and VDAC; I/O Port and D/A output.

### Features

- Pb-Free Packages are Available\*
- Low Power Dissipation
- I<sup>2</sup>C-Bus Format (2-Wire Type; SDA, SCL) Data Transfer
- 6-bit DAC
- Bus Address Selectable (3-bit)
- Address Input Pins are Pulled Up to V<sub>DD</sub> with Internal Resistor
- I/O Pins are Open Drain Outputs
- 5 Comparators at Inputs
- Inputs Protected from External Bus Currents in Power Down Mode

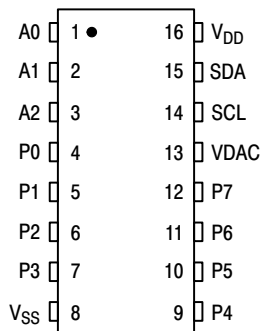


Figure 1. Pin Assignment

PIN LIST	
A0–A2	Chip Address Input
P0–P4	Comparator Input / Open Drain Output
P5–P7	Comparator Input / Open Drain Output
SCL	Serial Clock Input
SDA	I <sup>2</sup> C Data Output
VDAC	DAC Output

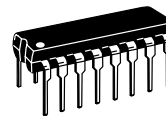
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



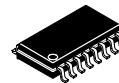
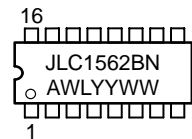
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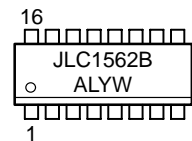
### MARKING DIAGRAMS



PDIP-16  
N SUFFIX  
CASE 648



EIAJ-16  
F SUFFIX  
CASE 966



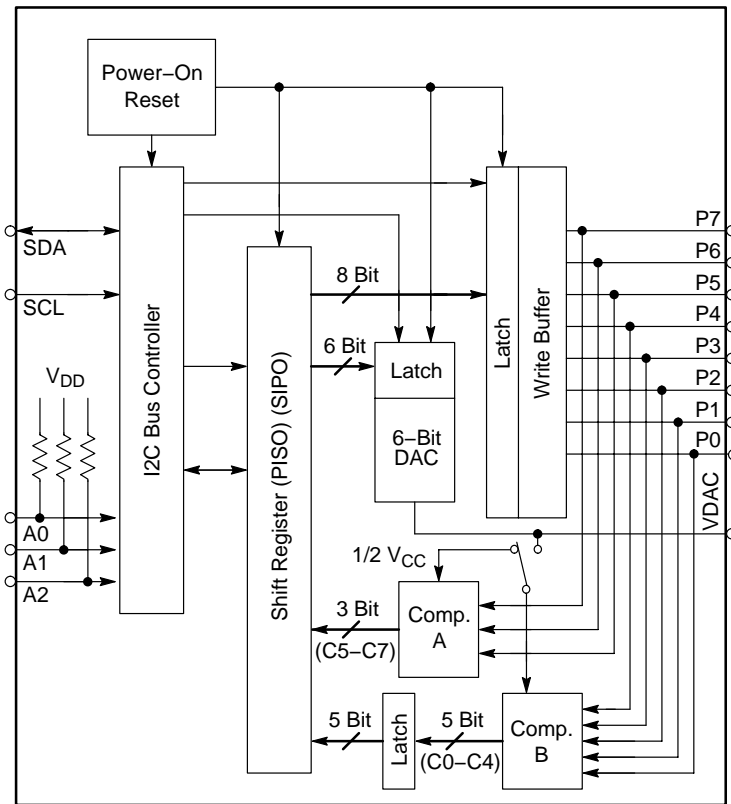
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping†
JLC1562BN	PDIP-16	500 / Unit PAK
JLC1562BNG	PDIP-16 (Pb-Free)	500 / Unit PAK
JLC1562BF	EIAJ-16 (Pb-Free)	50 Units / Rail
JLC1562BFEL	EIAJ-16 (Pb-Free)	2000 Units / Reel

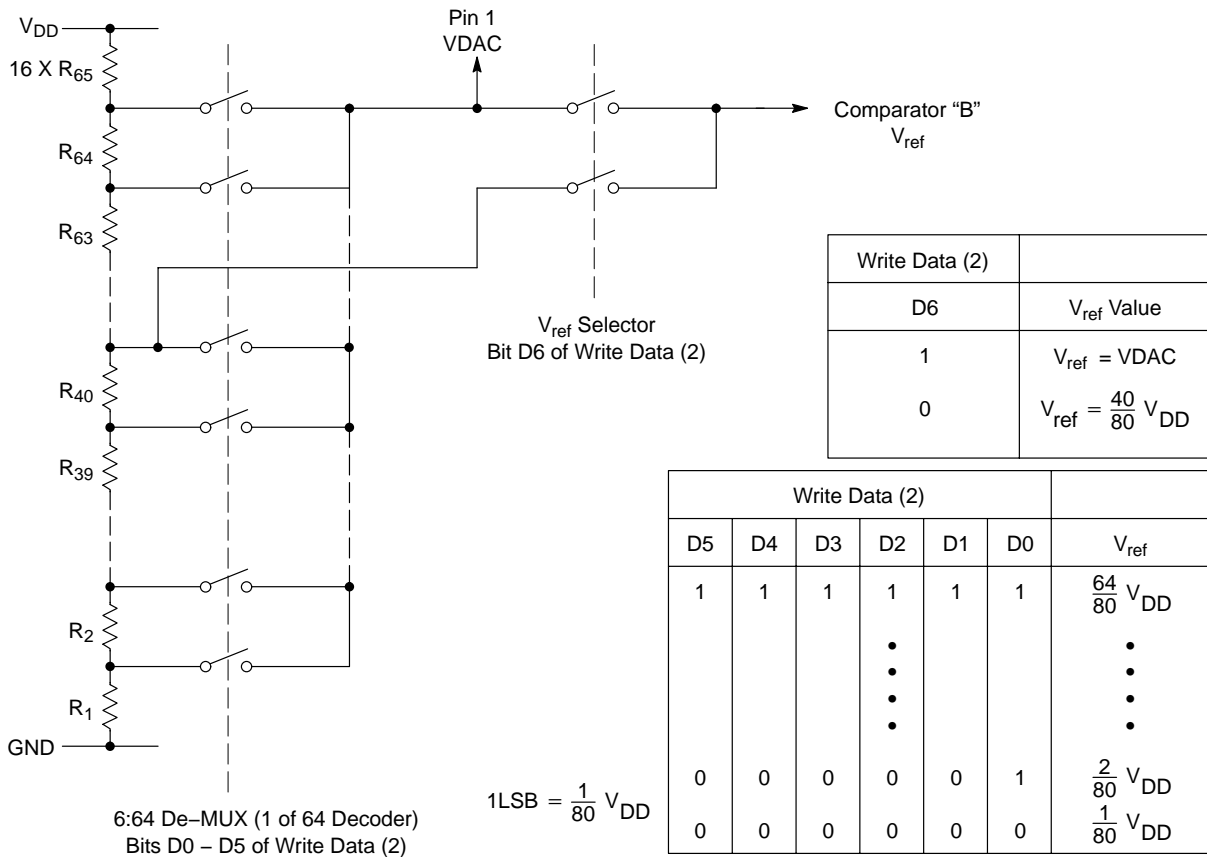
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# JLC1562B



NOTE: Internal Power On Reset sets P0 ~ P7 low, sets VDAC to 1/80 V<sub>DD</sub> and selects 1/2 V<sub>DD</sub> for Comparator "B" threshold.

Figure 2. Block Diagram



# JLC1562B

## MAXIMUM RATINGS (Referenced to GND)

Symbol	Parameter	Value	Unit
$V_{dd}$	DC Supply Voltage	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage	-0.5 to $V_{dd} + 0.5$	V
$V_{out}$	DC Output Voltage	-0.5 to $V_{dd} + 0.5$	V
I	DC Input/Output Current (per Pin)	25	mA
$I_{DD}$	DC Supply Current ( $V_{DD}$ and GND Pins)	75	mA
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds	300	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{dd}$	DC Supply Voltage	4.2	6.0	V
$V_{in}, V_{out}$	DC Input Voltage	0.0	$V_{dd}$	V
$T_A$	Operating Temperature	-40	+85	°C

## DC CHARACTERISTICS (Referenced to $V_{SS}$ )

Symbol	Parameter	Guaranteed Limit		Unit
		Min	Max	
$V_{IH}$	Maximum Input Voltage, "H"	0.7 $V_{dd}$	-	V
$V_{IL}$	Maximum Input Voltage, "L"	-	0.3 $V_{dd}$	V
$V_{OL}$	Maximum Output Voltage, "L" ( $I_{out} = 4mA$ )	-	0.3	V
$I_{in}$	Maximum Input Leakage Current ( $V_{in} = V_{dd}$ or $V_{SS}$ , SCL pin only)	-	$\pm 1.0$	$\mu A$
$I_{oz}$	Maximum Output Hi-Z Leakage Current (Output = High Impedance; $V_{out} = V_{dd}$ )	-	$\pm 5.0$	$\mu A$
$C_{in}$	Maximum Input Capacitance (Input Pin)	-	10	pF
$C_{out}$	Maximum Output Capacitance (Output Pin)	-	15	pF
$C_{i/o}$	Maximum I/O Capacitance (I/O Pin)	-	15	pF
$V_{ICR}$	Comparator Common Mode Input Voltage Range	0	$V_{dd} - 1.5$	V
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	-	5.0	mA

## COMPARATOR AC CHARACTERISTICS

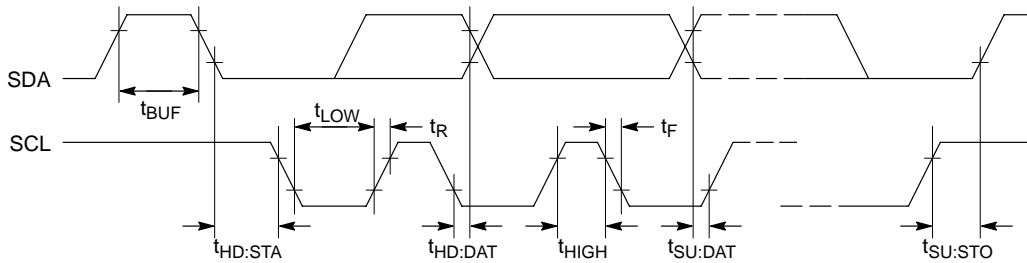
Symbol	Parameter	Test Conditions	Guaranteed Limit			Unit
			Min	Typ	Max	
$t_{PD}$	Maximum Propagation Delay	$V_{ref} = 1.5 V, 10mV$ overdrive	-	1.0	-	$\mu S$
		$V_{ref} = 1.5 V, 100mV$ overdrive	-	0.2	-	$\mu S$

DA COMPARATOR CHARACTERISTICS

Symbol	Parameter	Guaranteed Limit			Unit
		Min	Typ	Max	
DNL	DAC Referential NON-Linearity		±1/4 LSB		
e <sub>FS</sub>	DAC Full Scale Error			±1 LSB	
e <sub>ZC</sub>	DAC Zero Scale Error			±1 LSB	

TIMING CHARACTERISTICS

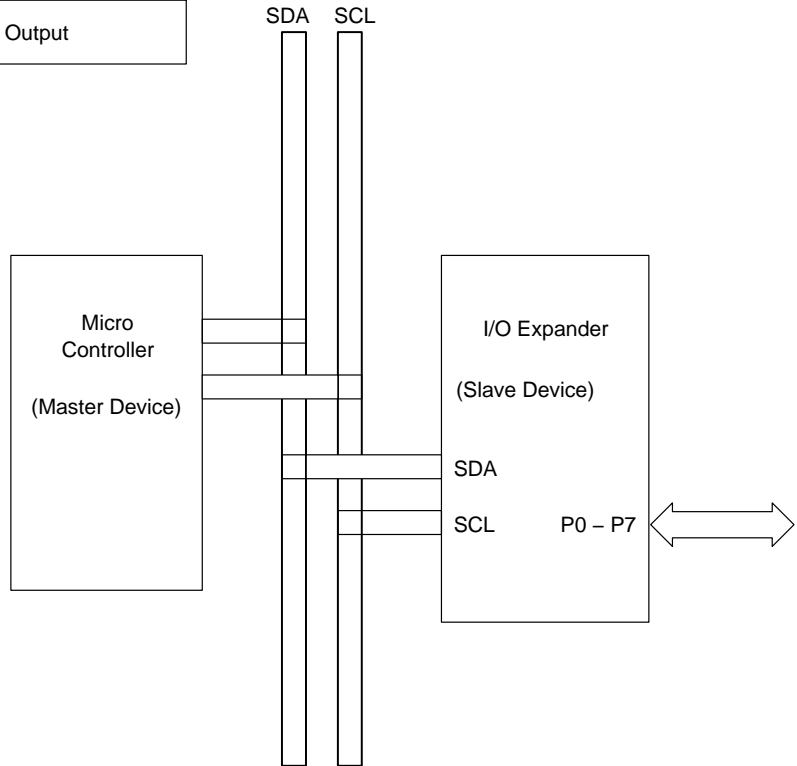
Symbol	Parameter	Guaranteed Limit		Unit
		Min	Max	
f <sub>CL</sub>	SCL CLOCK Frequency	0	100	kHz
t <sub>BUF</sub>	BUS Free Time (Between "STOP" and "START")	4.7	–	µs
t <sub>HD:STA</sub>	HOLD Time for "START"	4.0	–	µs
t <sub>LOW</sub>	HOLD Time at SCL CLOCK LOW	4.7	–	µs
t <sub>HIGH</sub>	HOLD Time at SCL CLOCK HI	4.0	–	µs
t <sub>HD:DAT</sub>	DATA HOLD Time	0	–	µs
t <sub>SU:DAT</sub>	DATA SETUP Time	250	–	ns
t <sub>R</sub>	Rise Time (SDA and SCL)	–	1000	ns
t <sub>F</sub>	Fall Time (SDA and SCL)	–	300	ns
t <sub>SU:STO</sub>	SETUP Time for "STOP"	4.0	–	µs



# JLC1562B

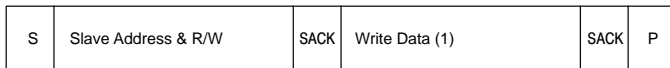
## READ / WRITE MODES

MODE	SDA		I/O Expander
	Master Device	Slave Device	I/O Port
READ	Receiver	Transmitter	Input
WRITE	Transmitter	Receiver	Output

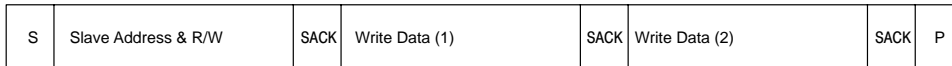


### The JLC1562B Supports the following types of Bus Cycles

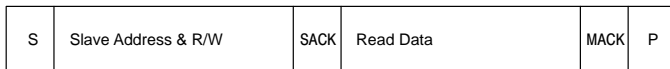
#### 1.) WRITE MODE (A)



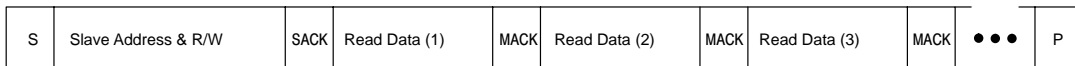
#### 2.) WRITE MODE (B)



#### 3.) READ MODE (A)



#### 4.) READ MODE (B)

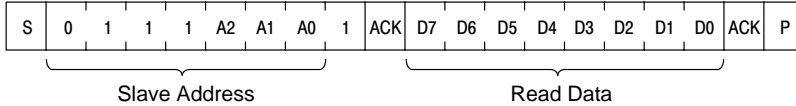


S = START Condition  
 SACK = Slave Acknowledgement  
 MACK = Master Acknowledgement  
 P = STOP Condition

# JLC1562B

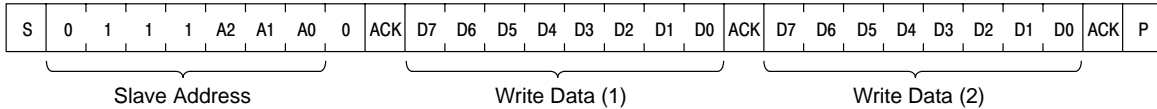
## READ WRITE DATA FORMAT

### <<READ MODE>>



Slave Address	A0 – A2  A3 – A6  R/W	I/O Expander Device Address (Pins A0 – A2)  <table border="1" style="display: inline-table; border-collapse: collapse; text-align: center; margin: 5px;"> <tr> <td style="width: 20px;">A6</td> <td style="width: 20px;">A5</td> <td style="width: 20px;">A4</td> <td style="width: 20px;">A3</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> </tr> </table> is hard wired as <table border="1" style="display: inline-table; border-collapse: collapse; text-align: center; margin: 5px;"> <tr> <td style="width: 20px;">0</td> <td style="width: 20px;">1</td> <td style="width: 20px;">1</td> <td style="width: 20px;">1</td> </tr> </table> 1 : READ ADDRESS	A6	A5	A4	A3	0	1	1	1	0	1	1	1
A6	A5	A4	A3											
0	1	1	1											
0	1	1	1											
Read Data	D5 – D7  D0 – D4	Output of Comparator “A”. ( $V_{th} = 1/2 V_{DD}$ )  Output of Comparator “B”. ( $V_{th} = 1/2 V_{DD}$ OR $V_{DAC}$ ) READ LATCH Bit Controls when Data Will Be Latched.												

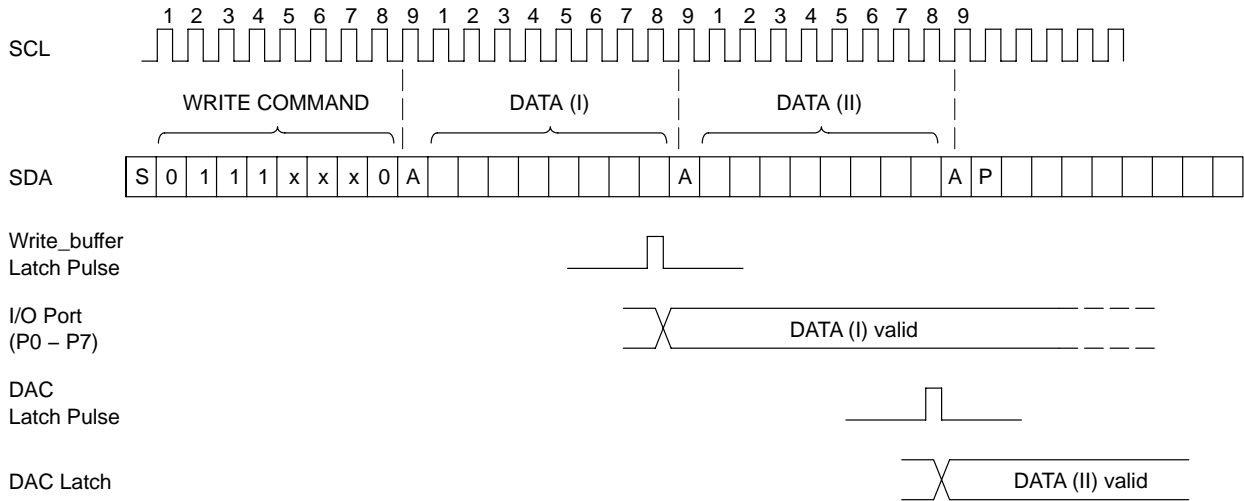
### <<WRITE MODE>>



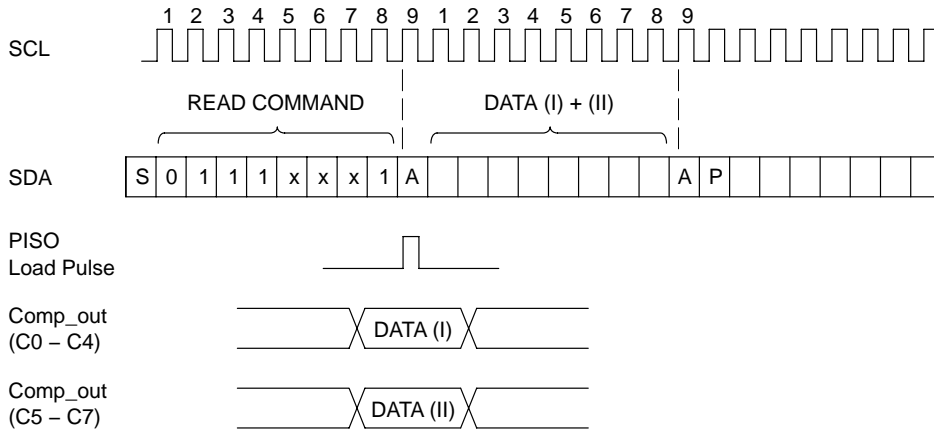
Slave Address	A0 – A2  A3 – A6  R/W	I/O Expander Device Address (Pins A0 – A2)  <table border="1" style="display: inline-table; border-collapse: collapse; text-align: center; margin: 5px;"> <tr> <td style="width: 20px;">A6</td> <td style="width: 20px;">A5</td> <td style="width: 20px;">A4</td> <td style="width: 20px;">A3</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> </tr> </table> is hard wired as <table border="1" style="display: inline-table; border-collapse: collapse; text-align: center; margin: 5px;"> <tr> <td style="width: 20px;">0</td> <td style="width: 20px;">1</td> <td style="width: 20px;">1</td> <td style="width: 20px;">1</td> </tr> </table> 0 : WRITE ADDRESS	A6	A5	A4	A3	0	1	1	1	0	1	1	1
A6	A5	A4	A3											
0	1	1	1											
0	1	1	1											
Write Data (1)	D0 – D7	Device Pins P0 to P7 Output Bits.												
Write Data (2)	D7          D6          D0 – D5	READ LATCH CONTROL    Latch Control of Signals C0 – C4 in the Device BLOCK DIAGRAM  0 : Data is latched at the ACK after a READ COMMAND. 1 : Data is latched when Comparator “B” switches from 0 to 1. (switch point is controlled by $V_{th}$ .) Data is reset at the ACK after a READ COMMAND.  COMPARATOR “B” $V_{ref}$ Control Bit  $0 : V_{ref} = \frac{40}{80} V_{DD}$ $1 : V_{ref} = V_{DAC}$  DAC Input Bits												

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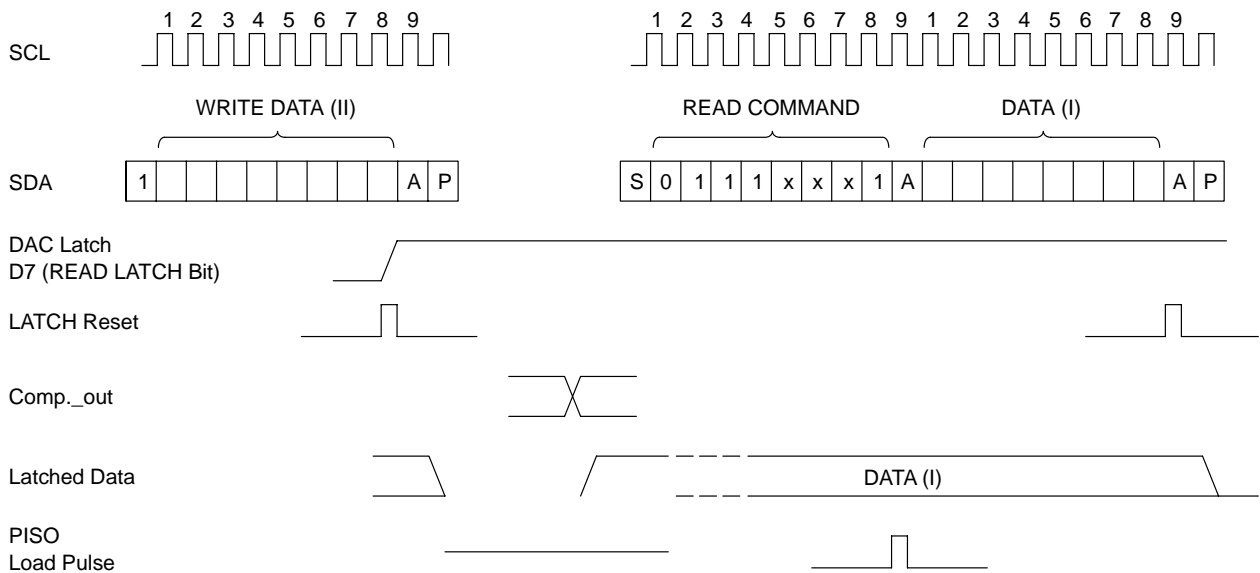
## <<WRITE MODE>>



## <<READ MODE>> (READ LATCH = 0)



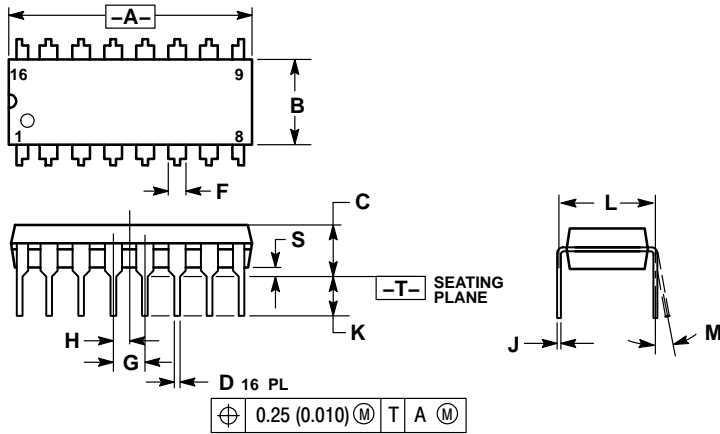
## <<READ MODE>> (READ LATCH = 1)



# JLC1562B

## PACKAGE DIMENSIONS

PDIP-16  
N SUFFIX  
CASE 648-08  
ISSUE T



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

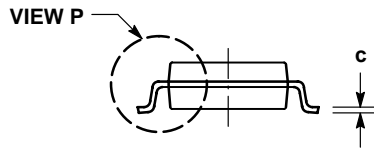
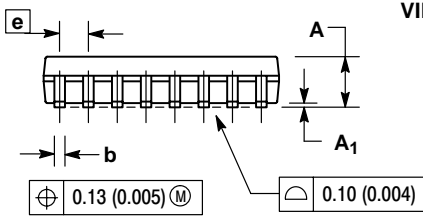
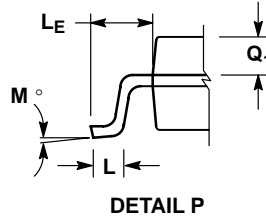
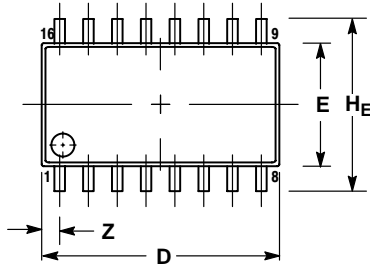
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01



# JLC1562B

## PACKAGE DIMENSIONS

EIAJ-16  
F SUFFIX  
CASE 966-01  
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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