

CMOS frequency synthesizer

TDD1742T

GENERAL DESCRIPTION

The TDD1742T is a low power, high-performance frequency synthesizer in local oxidation CMOS (LOCOS) technology. The device is designed for use in channelized VHF/UHF applications especially portable and mobile radios.

The circuit incorporates many of the features of the HEF4750V (frequency synthesizer) and HEF4751 (universal divider), including a high-gain phase comparator together with an on-chip sample-and-hold capacitor and phase modulator.

A multiplexed or bus-structured programming sequence allows interface to a microcontroller or external memory (ROM/PROM); power is applied to the memory only when it is required for programming via additional on-chip circuitry.

Operation is possible with a minimum supply voltage of 7 V and a maximum input frequency of 8,5 MHz.

Encapsulation in a 28-lead mini-pack enables the construction of small, low power consumption synthesizers with low noise performance and high side-band attenuation.

Features

- On-chip sample-and-hold capacitor
- Low power consumption
- High-gain phase comparator with low levels of noise and spurious outputs
- Auxiliary digital phase comparator for fast locking
- On-chip phase modulator
- Simple interfacing to external memory
- Microcontroller compatible
- Power-on reset circuitry

QUICK REFERENCE DATA

Supply voltage ranges

pin 14	$V_{DD1} = V_{14-6}$	7 to 10 V
pin 8	$V_{DD2} = V_{8-6}$	4,5 to 5 V
pin 1	$V_{DD3} = V_{1-6}$	7 to 10 V

Supply current

(at $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{DD1} = V_{DD3} = 7,4\text{ V}$; $V_{DD2} = 5\text{ V}$)

pin 14 (phase modulator OFF)	$I_{DD1} = I_{14}$	max. 1,5 mA
pin 8	$I_{DD2} = I_8$	max. 100 μA

CMOS frequency synthesizer

TDD1742T

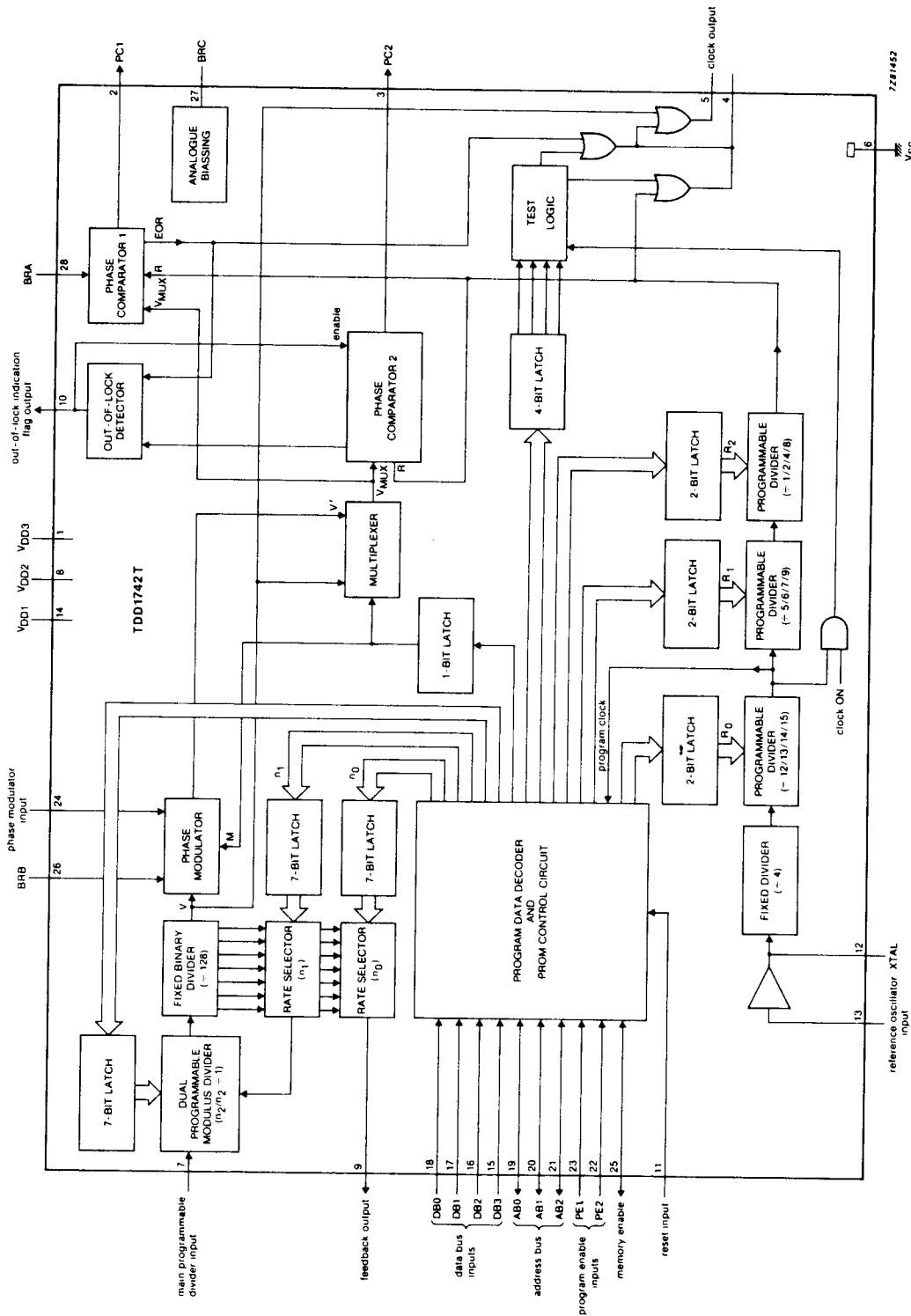


Fig. 1 Block diagram.

CMOS frequency synthesizer

TDD1742T

PINNING

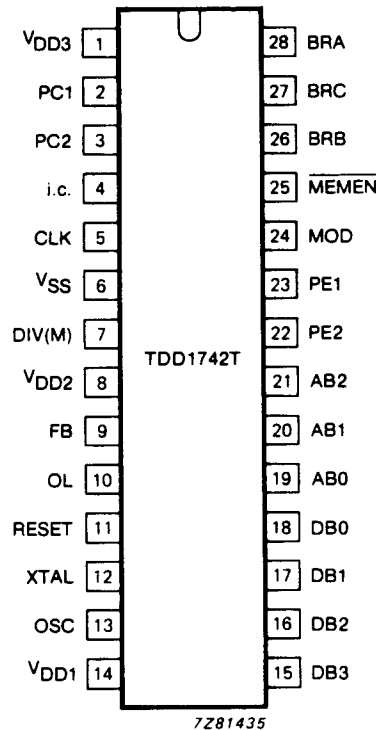


Fig. 2 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1	V _{DD3}	Power Supply 3: analogue supply voltage (7 to 10 V).
2	PC1	Phase Comparator 1: high-gain analogue phase comparator output which is used when the system is in-lock to give low levels of noise and spurious outputs.
3	PC2	Phase Comparator 2: low-gain digital phase comparator 3-state output which enables the achievement of fast lock times when the system is initially out-of-lock. Phase comparator 2 is inhibited when the phase is within the locking range of phase comparator 1.
4	i.c.	internally connected (must be left floating).
5	CLK	Clock: clock output.
6	V _{SS}	Ground: circuit earth potential.
7	DIV(M)	Divider: input to the main programmable divider (8,5 MHz max.), usually from prescaler.
8	V _{DD2}	Power Supply 2: supply voltage for TTL-compatible stages (+ 5 V ± 10%).
9	FB	Feedback: feedback output to control the modulus of the external prescaler.
10	OL	Out-of-lock: out-of-lock indication flag output. This output is HIGH when phase comparator 2 is in operation (when the system is out-of-lock).
11	RESET	Power-on-Reset: Following power up an initial pulse is applied to this input pin to set the internal counters.

CMOS frequency synthesizer

TDD1742T

Pin functions (continued)

pin no.	mnemonic	description
12	XTAL	Crystal: output to external crystal to form the oscillator circuit in combination with the OSC input. Alternatively this pin may be used as a buffer output.
13	OSC	Oscillator: input to reference oscillator which together with the XTAL output and an external crystal is used to generate the reference frequency. Alternatively to OSC input may be used as a buffer amplifier for an external reference oscillator.
14	V _{DD1}	Power Supply 1: digital supply voltage (7 to 10 V).
15-18	DB3-DB0	Data Bus: Data Bus inputs (TTL compatible).
19-21	AB0-AB2	Address Bus: TTL compatible bidirectional address bus. Provides address output to an external memory or input from microcontroller. The outputs are 3-state with internal pull-downs.
22	PE2	Program Enable 2: { TTL compatible inputs to initiate the programming cycle or strobe the internal data latches.
23	PE1	
24	MOD	Modulator: high impedance linear phase modulator input, which applies a voltage controlled delay to the programmable divider output to the phase comparator.
25	$\overline{\text{MEMEN}}$	Memory Enable: mode control and memory enable bidirectional pin. If pin 25 is LOW at general reset the TDD1742T is set to the microcontroller mode; if pin 25 is HIGH at general reset the TDD1742T is set to the memory mode and the ROM/PROM is enabled.
26	BRB	Bias Resistor B: current mirror which acts as gain control for the phase modulator.
27	BRC	Bias Resistor C: current mirror pin which provides analogue biasing.
28	BRA	Bias Resistor A: current mirror pin which acts as gain control for phase comparator 1.

CMOS frequency synthesizer

TDD1742T

FUNCTIONAL DESCRIPTION

Reference oscillator chain

The reference oscillator chain comprises a crystal oscillator and dividers to give the required frequency to drive the phase comparators.

The oscillator stage is a single inverter connected between pin 12 (XTAL) and pin 13 (OSC). Satisfactory operation is achieved with crystals up to 9 MHz. Alternatively, the OSC input may be used as a buffer amplifier for an external reference oscillator.

The reference divider chain comprises a fixed divide by 4-stage followed by three cascaded programmable dividers of ratios $\div 12/13/14/15$, $\div 5/6/7/9$ and $\div 1/2/4/8$. The output of the last stage is applied as one input (R) to the two phase comparators. Thus a number of division ratios between 240 and 4320 are possible which provides all the required VHF and UHF channel spacings with reference crystals in a 1 to 9 MHz range.

Main programmable divider

The main programmable divider is a rate feedback binary divider. As shown in figure 1 it comprises a fixed 7-bit binary divider ($\div 128$) and two rate selectors (n_1 and n_0). One rate selector controls a 7-bit fully programmable dual modulus divider ($\div n_2/n_2 + 1$) and the other controls the external dual modulus prescaler ($\div A/A + 1$).

The overall division rate (N) is given by:

$$N = (128 n_2 + n_1) A + n_0$$

Where:

$$0 \leq n_0 \leq 127$$

$$0 \leq n_1 \leq 127$$

$$1 \leq n_2 \leq 127.$$

The output from the programmable divider is fed to the phase comparators via the phase modulator and the multiplexer. The phase modulator is bypassed if not selected.

Phase comparison

The TDD1742T contains 2 phase comparators which act in close co-operation. Phase comparator 1 is the main comparator. It is designed to have a high-gain analogue output, 4500 volts/cycle at 10 kHz (typ.). This enables a low noise performance to be achieved. However, the output of phase comparator 1 will saturate at high or low levels for very small phase excursions.

Phase comparator 2 is an auxiliary comparator with a wide range, which enables faster lock times to be achieved than otherwise would be possible. This digital phase comparator has a linear $\pm 2\pi$ radians phase

range, which corresponds to a gain of $\frac{V_{DD}}{2}$ volts/cycle.

To avoid degrading the noise performance of the system by the relatively low gain of phase comparator 2, once a small phase error has been achieved an internal switch disconnects phase comparator 2, leaving only phase comparator 1 connected. Thus the low noise properties of phase comparator 1 are obtained once phase-lock has been achieved.

CMOS frequency synthesizer

TDD1742T

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 1 (see Fig. 3)

Phase comparator 1 is comprised of a linear ramp generator and a sample and hold circuit.

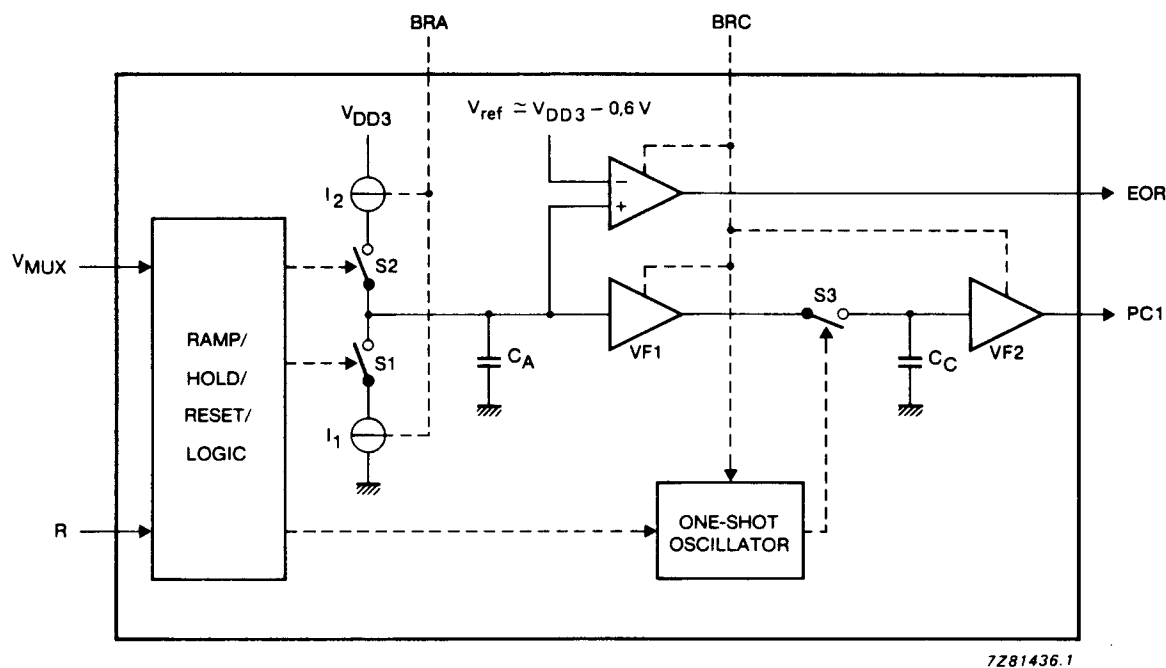


Fig. 3 Simplified block diagram of phase comparator 1.

A negative-going transition at the V_{MUX} input causes the hold capacitor C_A to be discharged via switch S1 and constant current source I_1 .

A positive-going transition at the V_{MUX} input causes the hold capacitor C_A to be charged via switch S2 and constant current source I_2 , which produces a linear ramp.

A negative-going transition at the R input terminates the linear ramp.

Capacitor C_A holds the voltage that the ramp has attained, and is buffered by the voltage follower VF1. After the output of VF1 is stable ($2 \mu s$), the sample switch S3 is closed for approximately $1 \mu s$ by the one-shot oscillator. This enables the capacitor C_C to charge to the voltage level of VF1 and in turn buffered by voltage follower VF2 made available at output PC1.

The construction and small duty cycle of the sample switch S3 provides a low hold step, resulting in a minimum side-band level.

If the linear ramp terminates before a negative-going transition at the R input is present, an end of ramp (EOR) signal is produced, generating in turn an out-of-lock (OL) signal. OL enables phase comparator 2 via the out-of-lock detector.

These actions are illustrated in the waveforms of Fig. 4 and Fig. 5.

The gain of phase comparator 1 as measured at PC1 is given by:

$$PC \text{ gain} \approx \frac{446 I_{BRA}}{F_R}$$

Where:

I_{BRA} is in μA

F_R is the phase comparator reference frequency in kHz

CMOS frequency synthesizer

TDD1742T

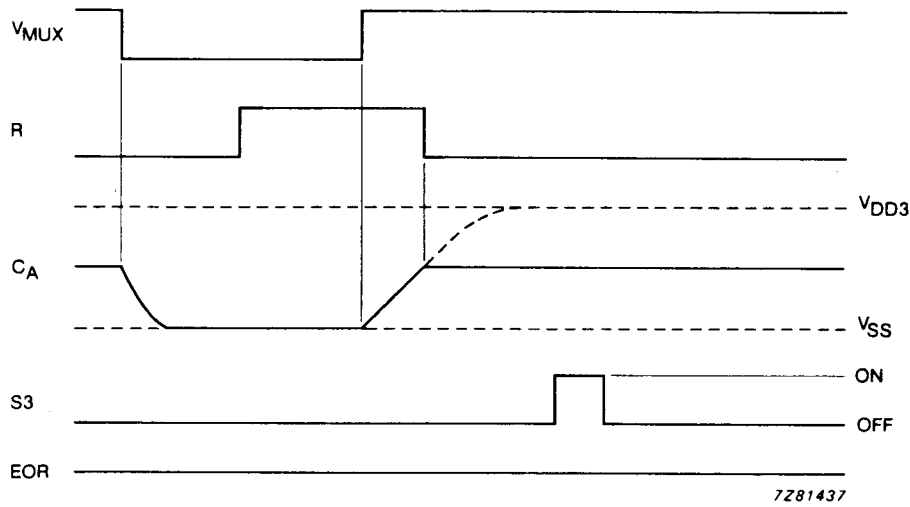


Fig. 4 Waveforms of phase comparator 1; in-lock condition.

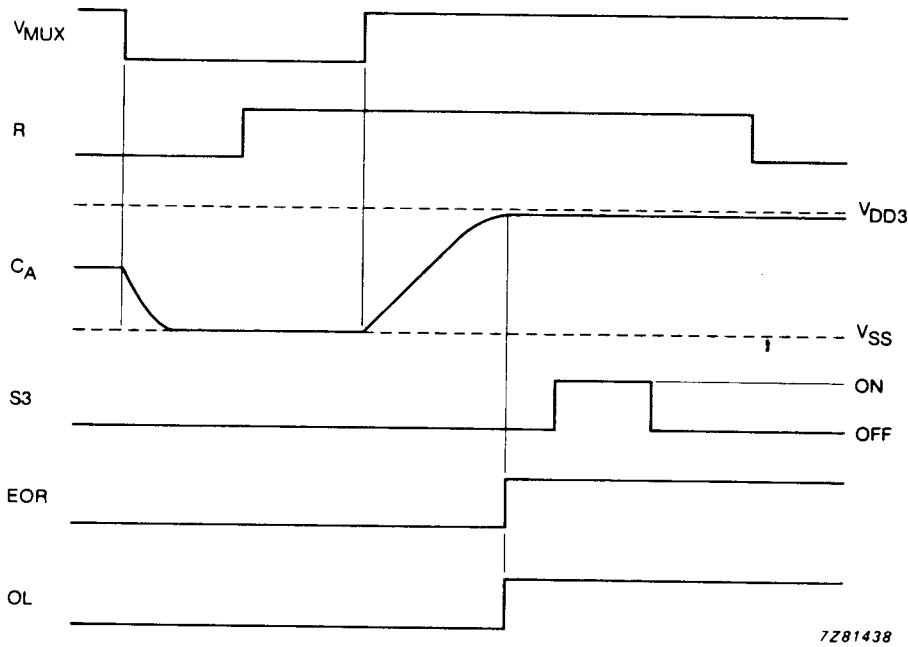


Fig. 5 Waveforms of phase comparator 1; out-of-lock condition.

When V_{MUX} leads R the output signal at pin 2 (PC1) is proportional to the phase difference (in-lock condition) or HIGH (out-of-lock condition).

When R leads V_{MUX} the output signal at pin 2 (PC1) remains LOW.

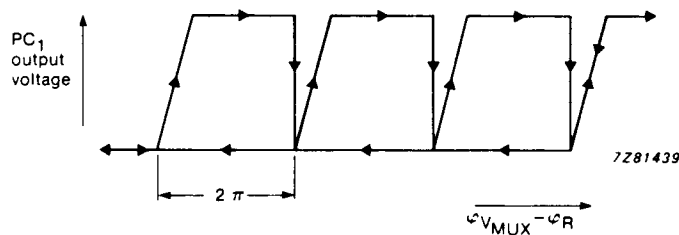


Fig. 6 Phase characteristic of output PC1.

CMOS frequency synthesizer

TDD1742T

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 2 (see Fig. 7)

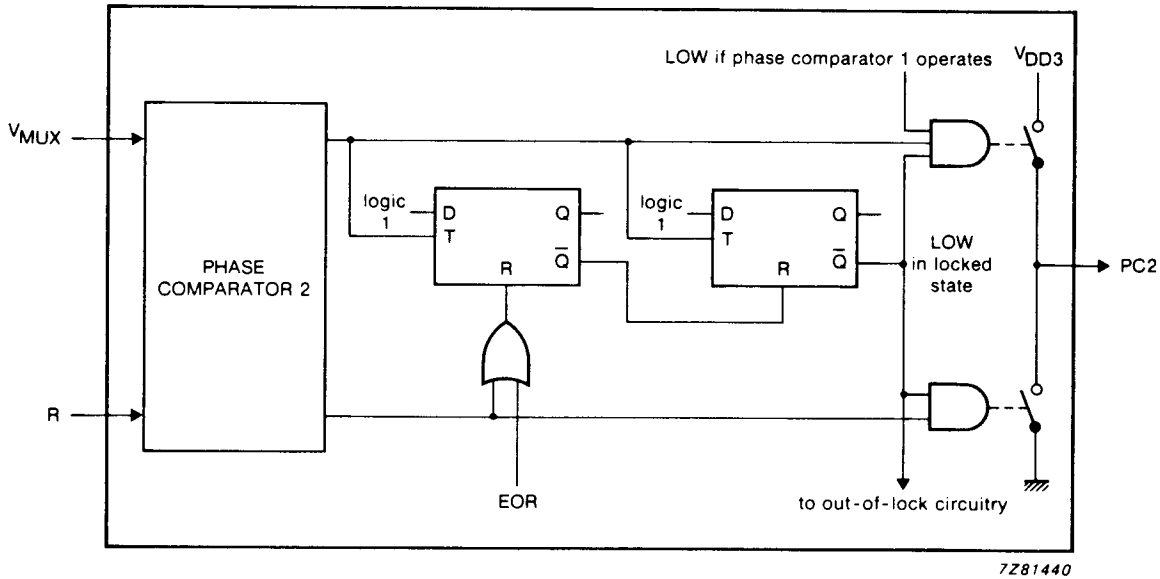


Fig. 7 Simplified block diagram of phase comparator 2.

The digital phase comparator (PC2) has three stable states:

- Reset
- V_{MUX} leads R
- R leads V_{MUX}

Table 1 Phase comparator 2: stable states and corresponding output levels

state	V_{MUX} leads R	R leads V_{MUX}
reset	0	0
V_{MUX} leads R	1	0
R leads V_{MUX}	0	1

Transition from one state to another takes place on command of either an active V_{MUX} -edge or an active R-edge as shown in Fig. 8.

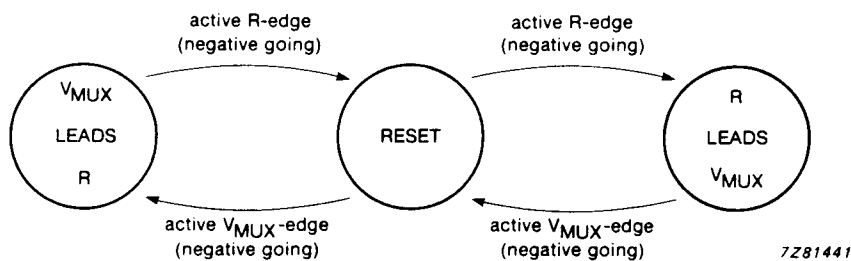


Fig. 8 Transition of state; phase comparator 2.

CMOS frequency synthesizer

TDD1742T

The output of phase comparator 2 produces positive or negative going pulses with variable width, dependent on the phase relationship of R and V_{MUX} .

The average output voltage is a linear function of the phase difference. Output at pin 3 (PC2) remains in the high impedance OFF-state in the region in which phase comparator 1 operates

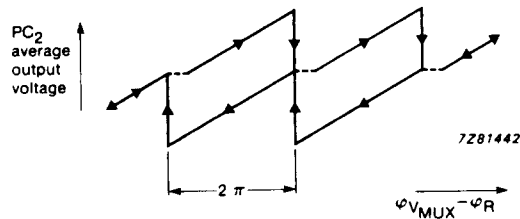


Fig. 9 Phase characteristic of output PC2.

To reach the reset state of phase comparator 2 it is necessary to apply:

- $2V_{MUX} + R^*$
- or
- $2R + V_{MUX}$

Thus to achieve the R leads V_{MUX} state $2R$ must be applied; to achieve the V_{MUX} leads R state $2V_{MUX}$ must be applied.

Out-of-lock function

There are several situations when the system goes from the locked to the out-of-lock state (OL output goes HIGH):

- V_{MUX} leads R, however out of the range of phase comparator 1
- R leads V_{MUX}
- R-pulse is missing
- V_{MUX} -pulse is missing

In the first three situations the locked state can be reset by applying two successive cycles within the range of phase comparator 1.

In the fourth situation the locked state can be reset by applying a V_{MUX} pulse followed by two successive cycles within the range of phase comparator 1.

Phase modulator (see Fig. 10)

The linear phase modulator applies a voltage controlled delay to the signal from the programmable divider to the phase comparator input. The gain of the phase modulator is adjustable via an external bias resistor (BRB) which is connected between pin 26 and ground.

The time delay introduced into the V path to the phase modulator is:

$$\frac{909}{I_{BRB}} \text{ ns/volt of input applied to pin 24 (MOD)}$$

When a positive-going transition appears at the V-input, the D type flip-flop produces a HIGH V' level and causes capacitor C_B to produce a positive-going ramp via switch S1 and constant current source I_1 starting at the V_{SS} potential. When the ramp has reached a value equal to the modulation input voltage (at MOD), the comparator resets the D type flip-flop, which terminates the V pulse. C_B now discharges to V_{SS} via switch S1 and constant current source I_2 and the circuit returns to the start position. Because the trailing edge of the V' pulse is the active edge for the phase comparators, a linear phase modulation is achieved. The associated waveforms are shown in Fig. 11. The phase modulator can be switched OFF, via the programming logic, to avoid superfluous dissipation. To achieve, this the M signal must be programmed to logic 0. The V pulse will then be connected via switch S2 to V_{MUX} .

* This means apply two successive active V_{MUX} edges followed by one active R edge.

CMOS frequency synthesizer

TDD1742T

FUNCTIONAL DESCRIPTION (continued)

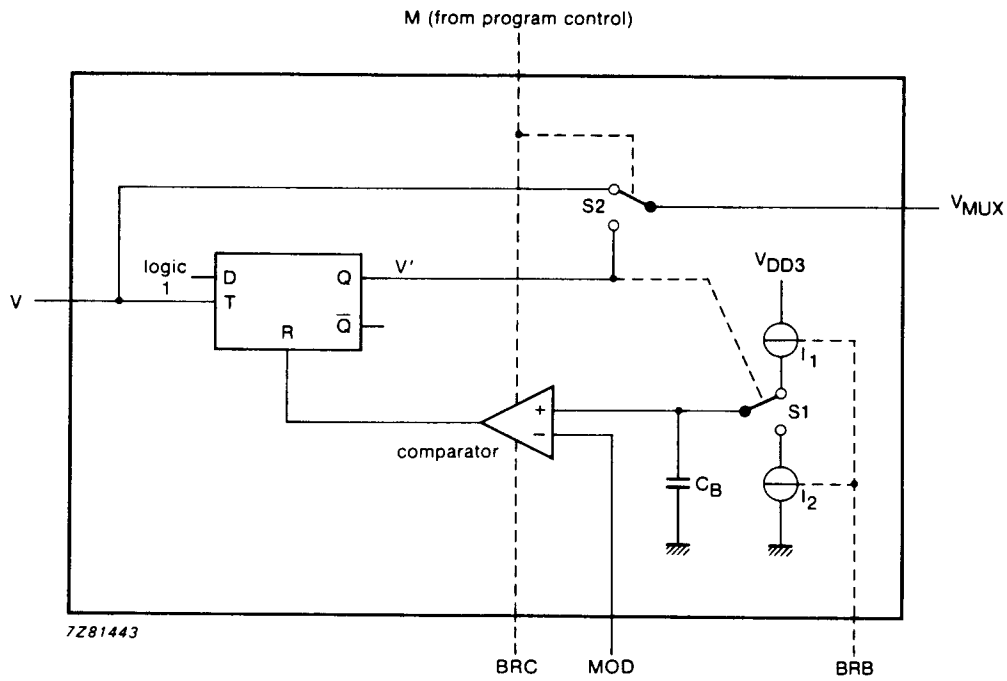


Fig. 10 Simplified block diagram of the phase modulator.

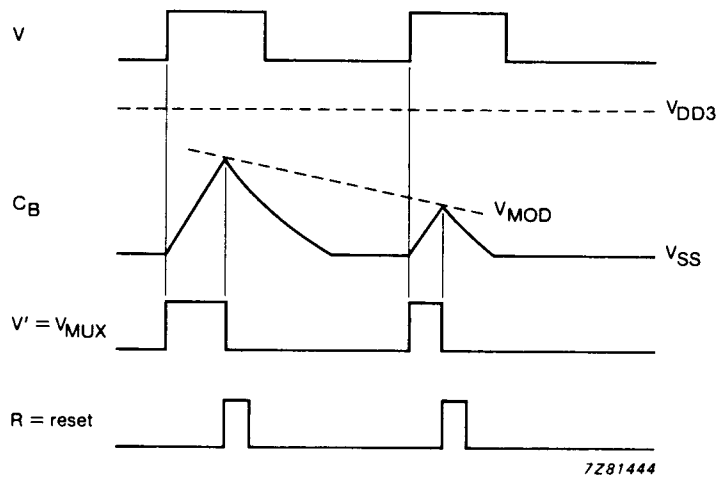


Fig. 11 Phase modulator waveforms; M = 1.

CMOS frequency synthesizer

TDD1742T

Program control

A multiplexed or bus structured sequence allows the TDD1742T to be interfaced to a microcontroller or a PROM.

The device is fully programmable in terms of:

- 6 bits to define the reference divider ratio
- 21 bits to define the main divider ratio
- 1 bit to switch the modulator
- 4 bits to determine the test status

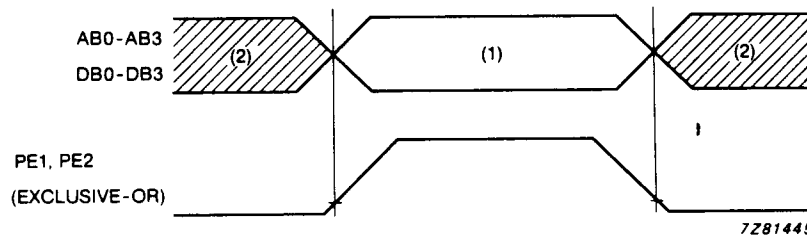
Thus the TDD1742T is programmed with a total of 32 bits which are organized as eight 4-bit words.

The address bus is 3 bits wide and the data bus is 4 bits wide. Both buses are TTL compatible.

The data words are described in detail in Tables 3 to 7.

Microcontroller mode

If pin 25 ($\overline{\text{MEMEN}}$) is LOW at general reset, the device is set to the micro-controller mode. In this mode a 7-bit word, comprised of 3 address bits (AB0 to AB2) and 4 data bits (DB0 to DB3), may be strobed into the TDD1742T when the program enable pins PE1 and PE2 are set to opposite state (EXCLUSIVE-OR condition; see Fig. 12 and Table 2). One frame of 8 words is necessary to completely program the TDD1742T. Incoming data is not clocked into the internal counter latches until after the receipt of data corresponding to address 111. Upon subsequent reprogramming it is not necessary to change all eight words but a reprogramming sequence must always finish with the data corresponding to address 111.



(1) Address and data valid.

(2) Address and data not valid.

Fig. 12 Waveforms for program enable function; microcontroller mode.

Table 2 Truth table for program enable function; microcontroller mode

PE1	PE2	load
0	0	NO
1	0	YES
0	1	YES
1	1	NO

CMOS frequency synthesizer

TDD1742T

Program control (continued)*Memory mode (PROM)*

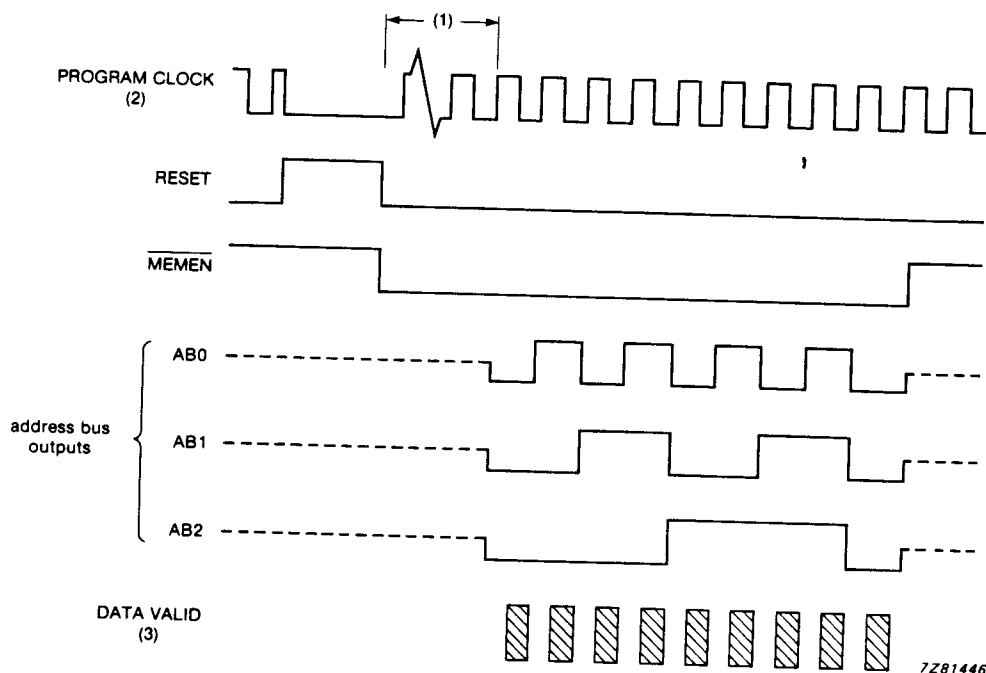
If pin 25 ($\overline{\text{MEMEN}}$) is HIGH at general reset, TDD1742T is set to the memory mode and a programming cycle is initiated. Subsequent reprogramming is performed by applying a pulse to program enable PE1 (pin 23) or PE2 (pin 22). If PE1 is LOW, programming will occur on the LOW-to-HIGH transition of PE2. If PE1 is HIGH, programming will occur on the HIGH-to-LOW transition of PE2. PE1 and PE2 are interchangeable. Reprogramming will also occur by applying a pulse to RESET (pin 11).

At the start of a programming sequence pin 25 goes LOW and may be used to apply power to the memory via an external driver. After a settling time the address bus outputs 000 followed by the remaining seven addresses. During the second half of each address period data, from the memory is latched into the TDD1742T so that the access time of the PROM is not critical.

Note

The program clock is derived from the reference divider chain and its frequency equals $f_{\text{OSC}}/4R_0$.

After the full 32 bits have been read the address returns to address 000 before going 3-state. This step transfers data from the internal data latches to the appropriate divider latches. Pin 25 now returns to a high impedance state and power is removed from the memory. Fig. 13 shows the timing for a reset initiated programming sequence; the timing is similar for program enable initiated sequence.



- (1) Delay time for PROM settling.
 (2) The program clock is derived from the reference divider chain.
 (3) Data is valid during the shaded period.

Fig. 13 Timing diagram for TDD1742T PROM control.

CMOS frequency synthesizer

TDD1742T

Data memory maps

Table 3 Bit programming of the eight 4-bit words

address			data			
AB2	AB1	AB0	DB3	DB2	DB1	DB0
0	0	0	see Table 4			
0	0	1	n ₀₃	n ₀₂	n ₀₁	n ₀₀
0	1	0	R ₀₀	n ₀₆	n ₀₅	n ₀₄
0	1	1	n ₁₃	n ₁₂	n ₁₁	n ₁₀
1	0	0	R ₀₁	n ₁₆	n ₁₅	n ₁₄
1	0	1	n ₂₃	n ₂₂	n ₂₁	n ₂₀
1	1	0	M	n ₂₆	n ₂₅	n ₂₄
1	1	1	R ₂₁	R ₂₀	R ₁₁	R ₁₀

In Table 3

n₀, n₁ and n₂ comprises the main programmable divider.

n₀₀ is the LSB of n₀, n₀₆ the MSB and so forth.

If M is 1 the modular is ON.

Table 4 Memory map for address 000

DB3	DB2	DB1	DB0	program clock to output CLK	mode
0	0	X	X	yes	idle
0	1	0	0	no	idle
all other combinations				not defined	not defined

Where

X = don't care.

For optimum performance (minimum crosstalk) 0100 should be programmed into address 000.

CMOS frequency synthesizer

TDD1742T

Memory maps (continued)

Table 5 Reference divider control; part 1

R ₀₁	R ₀₀	division ratio
0	0	12
0	1	13
1	0	14
1	1	15

In Table 5:

R₀₀ and R₀₁ control the ÷ 12/13/14/15 portion of the reference divider.

Table 6 Reference divider control; part 2

R ₁₁	R ₁₀	division ratio
0	0	9
0	1	5
1	0	6
1	1	7

In Table 6:

R₁₀ and R₁₁ control the ÷ 5/6/7/9 portion of the reference divider.

Table 7 Reference divider control; part 3

R ₂₁	R ₂₀	division ratio
0	0	1
0	1	2
1	0	4
1	1	8

In Table 7:

R₂₀ and R₂₁ control the ÷ 1/2/4/8 portion of the reference divider.

Current biasing

Current biasing is provided by 3 external bias resistors A, B and C.

Bias Resistor A: is connected between pin 28 (BRA) and ground. The value of the resistor must be such that $I_{BRA} = 20 \mu A$, which acts as gain control for analogue phase comparator 1.

Bias Resistor B: is connected between pin 26 (BRB) and ground. The value of the resistor must be such that $I_{BRB} = 3$ to $25 \mu A$, which acts as gain control for the phase modulator.

Bias Resistor C: is connected between pin 27 (BRC) and ground. The value of the resistor must be such that $I_{BRC} = 5$ to $30 \mu A$, which provides biasing for the remainder of the analogue circuitry.

CMOS frequency synthesizer

TDD1742T

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges

pin 14	V_{DD1}		-0,5 to + 15 V
pin 8	V_{DD2}		-0,5 to + 15 V
pin 1	V_{DD3}		-0,5 to + 15 V
Voltage on any input	V_I		-0,5 to $V_{DD1} + 0,5$ V
Relative supply voltage	$V_{DD2} - V_{DD1}$	max.	0,5 V
Relative supply voltage	$V_{DD3} - V_{DD1}$	max.	0,5 V
D.C. current into any input or output	$\pm I$	max.	10 mA
Power dissipation per package for $T_{amb} = 0$ to + 85 °C	P_{tot}	max.	400 mW
Power dissipation per output for $T_{amb} = 0$ to + 85 °C	P_O	max.	100 mW
Storage temperature range	T_{stg}		-65 to 150 °C
Operating ambient temperature range	T_{amb}		-40 to 85 °C

CMOS frequency synthesizer

TDD1742T

D.C. CHARACTERISTICS

$V_{DD1} = V_{DD3} = 7,4 \text{ V}$; $V_{DD2} = 5 \text{ V}$; $V_{SS} = 0 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ unless otherwise specified; for definitions see note 1.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage					
pin 14	V_{DD1}	7	—	10	V
pin 8	V_{DD2}	4,5	—	5	V
pin 1	V_{DD3}	7	—	10	V
Supply current					
pin 14 (phase modulator OFF)	I_{DD1}	—	—	1,5	mA
pin 8	I_{DD2}	—	—	100	μA
pin 1 (phase modulator OFF)	I_{DD3}	—	—	1,5	mA
Input leakage current (notes 2 and 3) logic inputs, MOD	$\pm I_{LI}$	—	—	300	nA
Output leakage current (notes 2 and 3) at $\frac{1}{2} V_{DD}$					
PC2 high impedance OFF state	$\pm I_{LO}$	—	—	50	nA
MEMEN high impedance state	$\pm I_{LO}$	—	—	1,6	μA
I/O current					
AB0 to AB2 high impedance state	$I_{I/O}$	5	—	30	μA
Logic input voltage LOW					
CMOS inputs; CMOS I/Os	V_{IL}	—	—	$0,3V_{DD1}$	V
TTL inputs; TTL I/Os	V_{IL}	—	—	0,8	V
Logic input voltage HIGH					
CMOS inputs; CMOS I/Os	V_{IH}	$0,7V_{DD1}$	—	—	V
TTL inputs; TTL I/Os	V_{IH}	2	—	—	V
Logic output voltage LOW (note 2) at $ I_O < 1 \mu\text{A}$	V_{OL}	—	—	50	mV
Logic output voltage HIGH (note 2) at $ I_O < 1 \mu\text{A}$	V_{OH}	$V_{DD1}-50$	—	—	mV

CMOS frequency synthesizer

TDD1742T

parameter	symbol	min.	typ.	max.	unit
Logic output voltage LOW (note 2)					
MEMEN at $I_{OL} = 4$ mA	V_{OL}	—	—	1	V
PC2 at $I_{OL} = 1,5$ mA	V_{OL}	—	—	0,5	V
CLK; OL at $I_{OL} = 1$ mA	V_{OL}	—	—	0,5	V
XTAL at $I_{OL} = 3$ mA	V_{OL}	—	—	0,5	V
FB at $I_{OL} = 1$ mA	V_{OL}	—	—	0,5	V
AB0; AB1; AB2 at $I_{OL} = 0,2$ mA	V_{OL}	—	—	0,4	V
Logic output voltage HIGH (notes 2 and 3)					
PC2 at $-I_{OH} = 1,5$ mA	V_{OH}	$V_{DD1}-0,5$	—	—	V
CLK; OL at $-I_{OH} = 1$ mA	V_{OH}	$V_{DD1}-0,5$	—	—	V
XTAL at $-I_{OH} = 3$ mA	V_{OH}	$V_{DD1}-1$	—	—	V
FB at $-I_{OH} = 1$ mA	V_{OH}	$V_{DD2}-1$	—	—	V
AB0; AB1 at $I_{OH} = 0,2$ mA	V_{OH}	2,4	—	—	V
AB2 at $I_{OH} = 0,8$ mA	V_{OH}	2,4	—	—	V
Output PC1					
sink current (notes 2, 3 and Fig. 15)	I_O	1	—	—	mA
source current (notes 2, 3 and Fig. 16)	$-I_O$	1	—	—	mA
Internal resistance of					
phase comparator 1 (notes 2 and 3)					
locked state output swing < 200 mV					
specified output range:					
$0,5 V_{DD} - 0,5$ V to $0,5 V_{DD} + 0,5$ V	R_i	—	2,0	—	Ω

CMOS frequency synthesizer

TDD1742T

A.C. CHARACTERISTICS

A dynamic specification is given for the circuit, built-up with external components as shown in Fig. 14, under the following conditions; for definitions see note 1; $V_{DD} = 7,4 \pm 0,4$ V; $T_{amb} = 25$ °C; input transition times ≤ 40 ns; $C_A = C_B = C_C = 10$ nF; R_A chosen so that $I_{RA} = 20 \mu\text{A} \pm 1 \mu\text{A}$; R_B chosen so that $I_{RB} = 3$ to $25 \mu\text{A}$; R_C chosen so that $I_{RC} = 5$ to $30 \mu\text{A}$; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Main programmable divider (DIV(M); pin 7) input frequency all divider ratios (square wave input)	$f_{DIV(M)}$	8,5	—	—	MHz
Reference divider input frequency all divider ratios (square wave input)	$f_{DIV(R)}$	9	—	—	MHz
Oscillator frequency (OSC; pin 13)	f_{OSC}	9	12	—	MHz
Input capacitance DIV(M); OSC	C_I	—	—	3	pF
DB0 to DB3; PE1; PE2; AB0 to AB2	C_I	—	—	5	pF
Propagation delay (see Fig. 17)					
Feedback output to external prescaler DIV (M) \rightarrow FB at $C_L = 10$ pF					
HIGH to LOW*	t_{PHL}	—	35	70	ns
LOW to HIGH*	t_{PLH}	—	35	70	ns
Average power supply current (notes 3 and 4) in-lock state	I_{DD1}	—	2	—	mA
	I_{DD2}	—	0,15	—	mA
	I_{DD3}	—	0,45	—	mA

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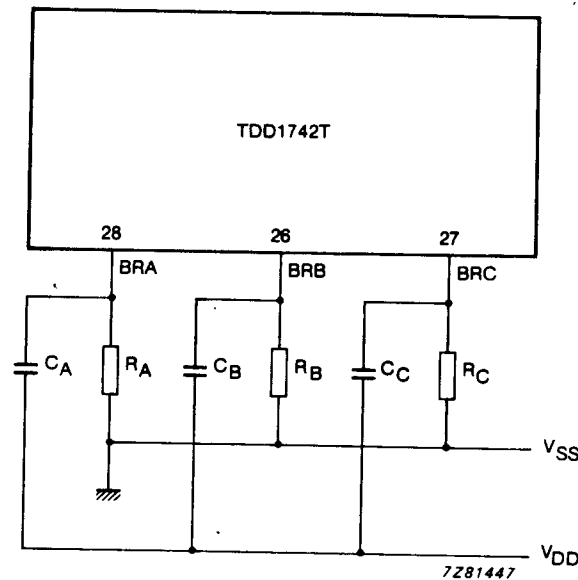


Fig. 14 Test circuit for measuring a.c. characteristics.

Notes to the characteristics

1. Definitions:

R_A = external biasing resistor between pins BRA and V_{SS} .

R_B = external biasing resistor between pins BRB and V_{SS} .

R_C = external biasing resistor between pins BRC and V_{SS} .

C_A = decoupling capacitor between pins BRA and V_{DD} .

C_B = decoupling capacitor between pins BRB and V_{DD} .

C_C = decoupling capacitor between pins BRC and V_{DD} .

CMOS logic inputs: RESET, OSC.

CMOS logic outputs: PC2, CLK, OL, XTAL.

CMOS logic I/O: MEMEN.

TTL logic inputs: DB0 to DB3, PE2, PE1.

TTL logic output: FB.

TTL logic I/O: AB0 to AB2.

Analogue inputs: DIV(M), MOD.

Analogue output: PC1.

Analogue biasing pins: BRA, BRB, BRC.

2. All logic inputs at V_{SS} or V_{DD} .3. R_A connected; its value chosen such that $I_{BRA} = 20 \mu A$.

R_B connected; its value chosen such that $I_{BRB} = 20 \mu A$.

R_C connected; its value chosen such that $I_{BRC} = 20 \mu A$.

4. Average power supply current measured at:

$f_{OSC} = 5 \text{ MHz}$, external clock, divider ratio 420;

$f_{DIV(M)} = 2 \text{ MHz}$, divider ratio 168.

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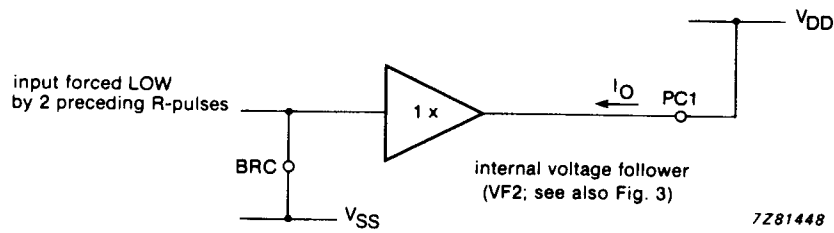


Fig. 15 Equivalent circuit for output PC1 sink current.

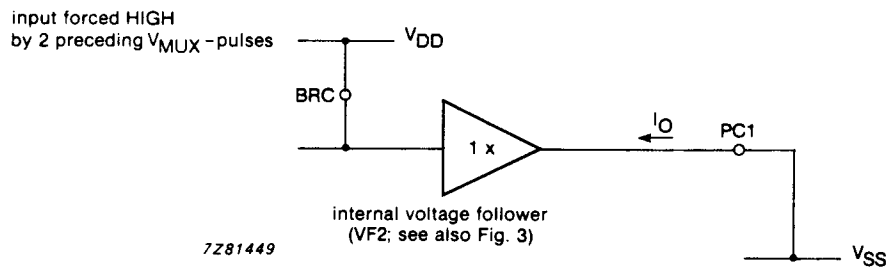


Fig. 16 Equivalent circuit for output PC1 source current.

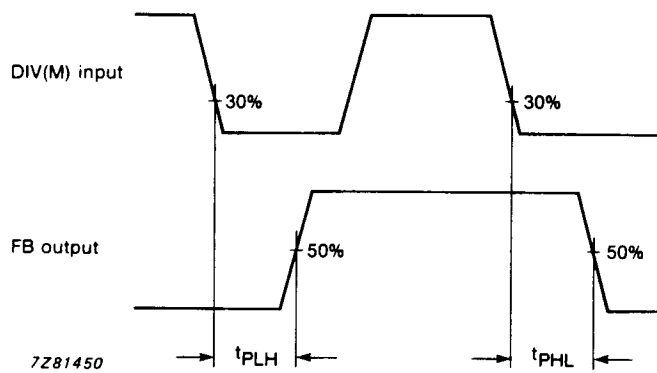


Fig. 17 Waveforms showing propagation delay; DIV (M) → FB.

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APPLICATION INFORMATION

Fig. 18 shows a typical application circuit using the TDD1742T in the memory mode with the following design parameters:

Frequency range	150 to 155 MHz
VCO sensitivity	1 MHz/V
Reference frequency	12,5 kHz
Prescaler	$\div 80/81$
Reference crystal frequency	5,25 MHz
Reference divider chain	$\div 15; \div 7; \div 1$
Total division ratio	12000 to 12400
Loop bandwidth	300 Hz

