

GENERAL

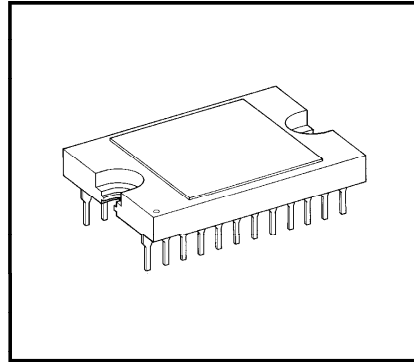
TCD5130AC is a frame interline CCD area image sensor developed for a 3-CCD color camera (PAL/SECAM TV system).

This device has signal pixels of 754 (horizontal) × 583 (vertical), and its image size agrees with 2/3 inch type optical system.

This device offers high sensitivity and resolution, low smearing and reduces lag, picture sticking, after image, picture distortion and microphonic noise. It can be used for video cameras, surveillance cameras, object detection and pattern recognition.

FEATURES

- Total Signal Pixel Number : 803 (H) × 586 (V)
- Signal Pixel Number : 754 (H) × 583 (V)
- Pixel Size : 12.0 μm (H) × 11.5 μm (V)
- Image Size : 9.05mm (H) × 6.70mm (V)
- Package : 24 pin DIP, Ceramics, Multi-Coring Glass
- Additional Function : Electronic Shutter (1 / 50~2000 s)

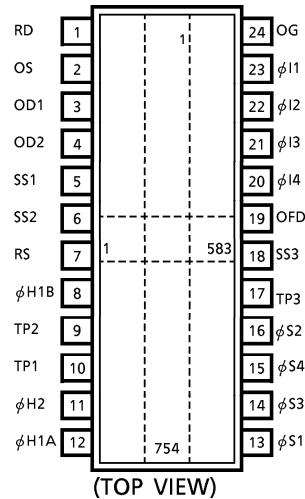


Weight : 7.8g (Typ.)

MAXIMUM RATINGS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Vertical CCD Clock Pulse Voltage	V _φ V	-10~18	V
Horizontal CCD Clock Pulse Voltage	V _H	-0.3~18	V
Reset Pulse Voltage	V _{RS}		
Output Gate Voltage	V _{OG}		
Reset Drain Voltage	V _{RD}		
Output Transistor Drain Voltage	V _{OD}		
Test Terminal Voltage	V _{TP}		
Overflow Drain Voltage	V _{OFD}	-0.3~30	V
Operating Temperature	T _{op}	-20~60	°C
Storage Temperature	T _{stg}	-40~85	°C

PIN CONNECTIONS



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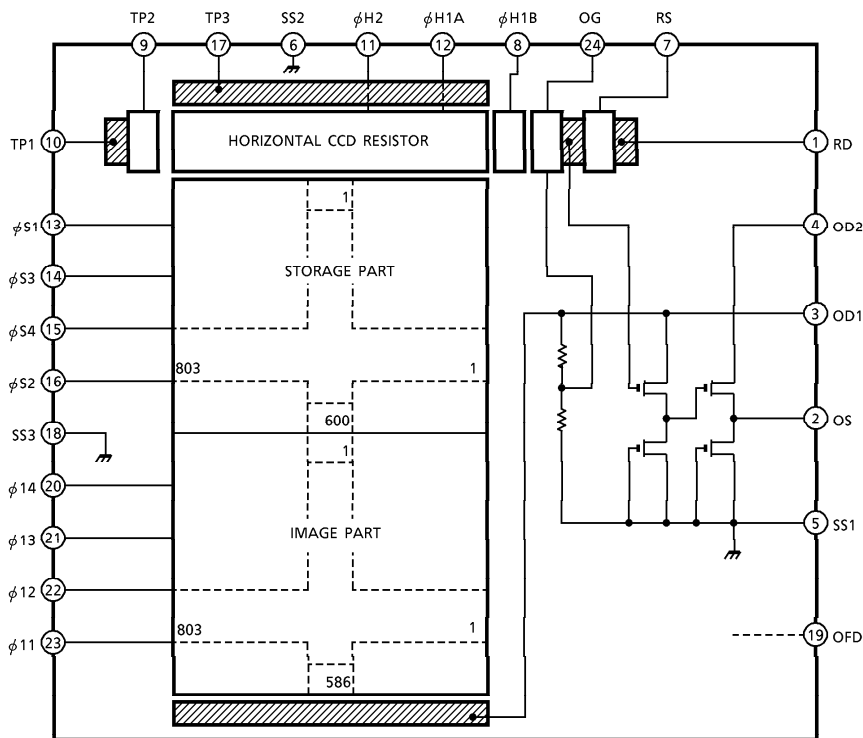
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CIRCUIT DIAGRAM



PIN NAMES

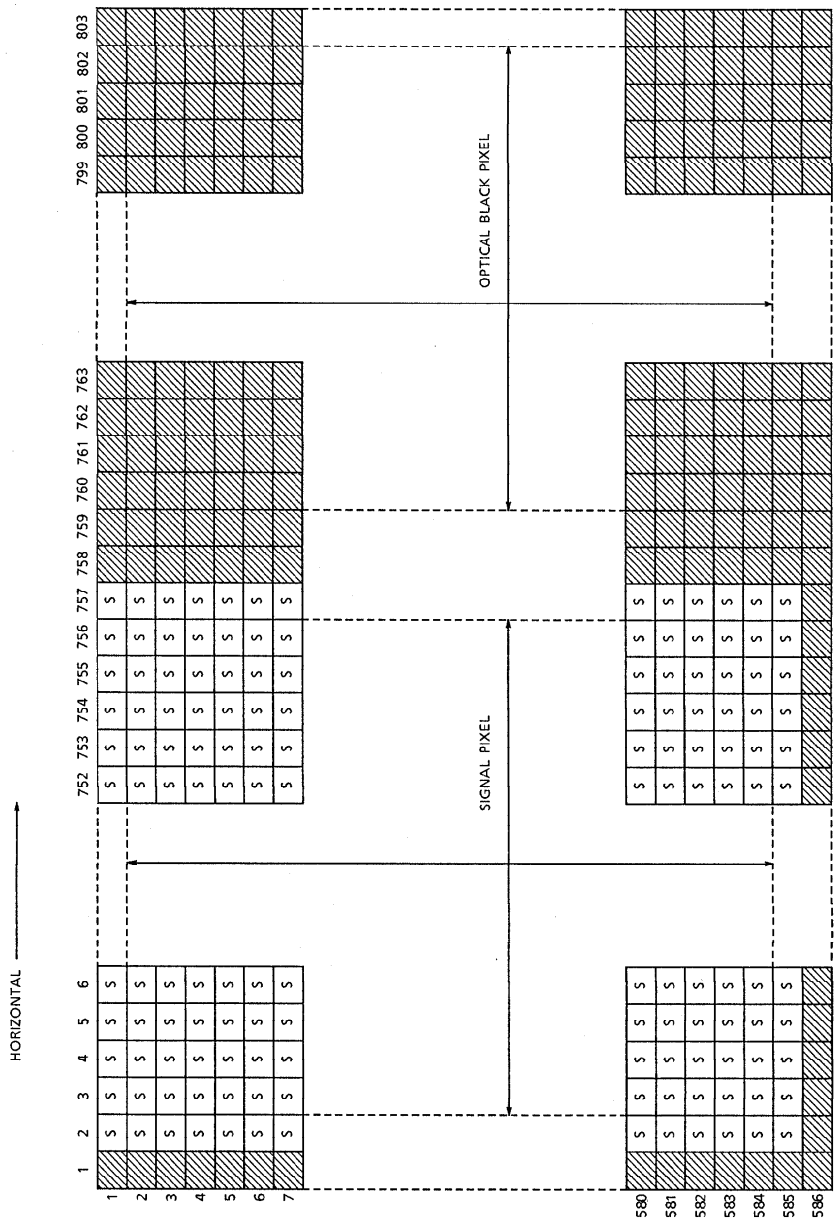
SYMBOL	PIN NAME	SYMBOL	PIN NAME
$\phi I1$	Image Part V-CCD Clock (Phase 1)	OD1	First Output Transistor Drain
$\phi I2$	Image Part V-CCD Clock (Phase 2)	OD2	Second Output Transistor Drain
$\phi I3$	Image Part V-CCD Clock (Phase 3)	OFD	Overflow Drain
$\phi I4$	Image Part V-CCD Clock (Phase 4)	TP1	Test Pin
$\phi H1A$	Horizontal CCD Clock (Phase 1)	TP2	Test Pin
$\phi H1B$	Final Stage Clock (Phase 1)	OS	Output Transistor Source
$\phi H2$	Horizontal CCD Clock (Phase 2)	RS	Reset Gate
$\phi S1$	Storage Part Transfer Clock (Phase 1)	OG	Output Gate
$\phi S2$	Storage Part Transfer Clock (Phase 2)	SS1	Substrate (1) (Ground)
$\phi S3$	Storage Part Transfer Clock (Phase 3)	SS2	Substrate (2) (Ground)
$\phi S4$	Storage Part Transfer Clock (Phase 4)	SS3	Substrate (3) (Ground)
TP3	Test Pin	RD	Reset Drain

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PHOTOSENSING ELEMENT ARRANGEMENT



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OPTICAL AND ELECTRICAL CHARACTERISTICS

Tungsten electric lamp light of 3000K color temperature passing a cyan filter C500 (1.0mm thick, made by HOYA GLASS CO.) and an infrared cut filter (mesial magnitude 680nm).

CCD drive timing pulse generator IC is TC6024AU, TC6085AU and TC6134AF on the field storage mode. A measurement point is CCD output signal (emitter follower output).

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Photo Sensitivity	R		65	80	—	mV / lx
Saturation Voltage	V _{SAT}	V _{OFD} adjustment	600	900	—	mV
Dark Signal Voltage	V _{DRK}	T _c = 60°C	—	1	2	mV
Reset Pulse Feed Through	RFT		—	400	700	mV
Smear	SMR		—	-120	-110	dB
Output Impedance	Z _O		—	250	300	Ω
Output Transistor Current	I _{OD}		—	—	10	mA
Lag	LAGd	V _{sig} = 20mV	—	0.1	1	mV
Blooming Margin	BLM	V _{OFD} adjustment	8500	—	—	Time

(Note) V_{OFD} adjustment
Operate CCD under 8.5×10^3 times the light intensity of the standard condition. CCD output signal is 200mV under the standard condition.
And then set up V_{OFD} to a voltage not to be occurred Blooming.

OPERATING CONDITION

CHARACTERISTIC			SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
Image Part Clock Pulse Voltage	Field Shift		$V_{\phi FS}$	13.0	13.5	14.0	V	
	Line Shift	"H" Level	$V_{\phi IH}$	-0.5	0	0.5		
		"L" Level	$V_{\phi IL}$	-9.5	-9.0	-8.5		
Storage Part Clock Pulse Voltage	"H" Level		$V_{\phi SH}$	-0.5	0	0.5	V	
	"L" Level		$V_{\phi SL}$	-9.5	-9.0	-8.5		
Horizontal CCD Clock Pulse Voltage			$V_{\phi H}$	4.75	5.0	5.5	$V_{p.p}$	
Reset Pulse Voltage	DC. Bias		$V_{\phi RS}$	3.1	3.6	4.1	V	
	AC. Amplitude			4.75	5.0	5.25	$V_{p.p}$	
Output Gate Voltage			V_{OG}	3.1	3.6	4.1	V	
Reset Drain Voltage			V_{RD}	14.5	15.0	15.5	V	
First Output Transistor Drain Voltage			V_{OD1}	14.5	15.0	15.5	V	
Second Output Transistor Drain Voltage			V_{OD2}	14.5	15.0	15.5	V	
Test Pin (1) Voltage			V_{TP1}	14.5	15.0	15.5	V	
Test Pin (2) Voltage			V_{TP2}	0	0	0	V	
Test Pin (3) Voltage			V_{TP3}	0	0	0	V	
Overflow Drain Voltage			V_{OFD}	7~26			V	(Note)

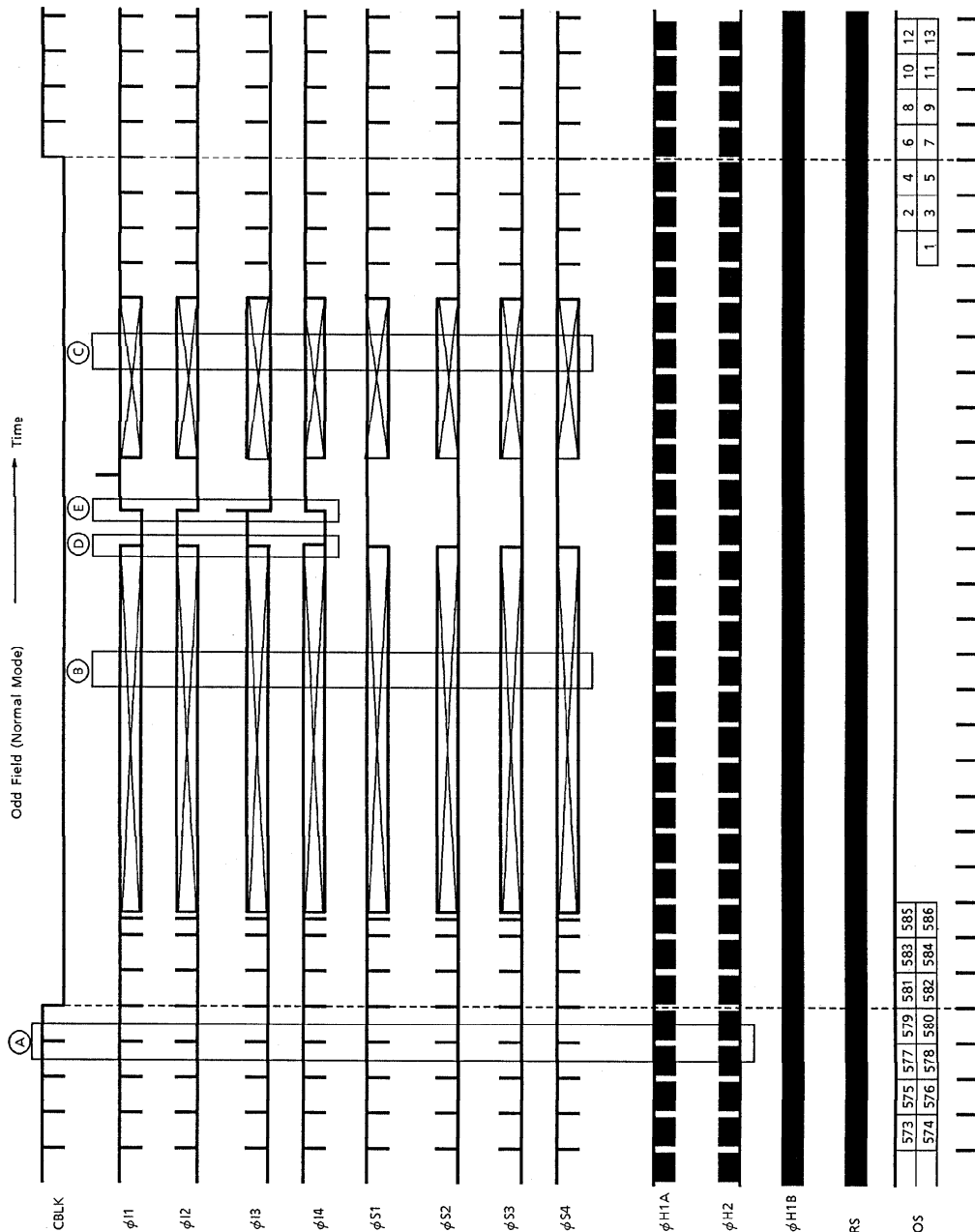
(Note) V_{OFD} values is indicated on package. Adjustment voltage is $\pm 0.2V$. Symbol and voltage is as follows;

Symbol	3CA	3CB	3CC	3CD	3CE	3CF	3CG	3CH	3CI	3CJ	3CK
Voltage (V)	7.0	7.5	8.0	8.5	9.0	9.5	10.0	10.5	11.0	11.5	12.0
Symbol	3CL	3CM	3CN	3CO	3CP	3CQ	3CR	3CS	3CT	3CU	3CV
Voltage (V)	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5
Symbol	3CW	3CX	3CY	3CZ	3CAA	3CAB	3CAC	3CAD	3CAE	3CAF	3CAG
Voltage (V)	18.0	18.5	19.0	19.5	20.0	20.5	21.0	21.5	22.0	22.5	23.0
Symbol	3CAH	3CAI	3CAJ	3CAK	3CAL	3CAM					
Voltage (V)	23.5	24.0	24.5	25.0	25.5	26.0					

CLOCK CHARACTERISTICS

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT
Horizontal CCD Clock Frequency		$f_{\phi H}$	—	14.187	—	MHz
Reset Pulse Frequency		$f_{\phi RS}$	—	14.187	—	
Image Part Clock Pulse Frequency	Charge Sweep	$f_{\phi I(1)}$	—	1.2	—	
	Field Transfer	$f_{\phi I(2)}$	—	1.0	—	
Storage Part Clock Pulse Frequency	Charge Sweep	$f_{\phi S(1)}$	—	1.2	—	
	Field Transfer	$f_{\phi S(2)}$	—	1.0	—	
	Line Shift	$f_{\phi S(3)}$	—	15.625	—	kHz
Image Part Vertical CCD Clock Capacitance	Phase 1	$C_{\phi I1}$	—	4000	—	pF
	Phase 2	$C_{\phi I2}$	—	4600	—	
	Phase 3	$C_{\phi I3}$	—	4000	—	
	Phase 4	$C_{\phi I4}$	—	4600	—	
Storage Part Vertical CCD Clock Capacitance	Phase 1	$C_{\phi S1}$	—	3000	—	
	Phase 2	$C_{\phi S2}$	—	3900	—	
	Phase 3	$C_{\phi S3}$	—	3000	—	
	Phase 4	$C_{\phi S4}$	—	3900	—	
Horizontal CCD Clock Capacitance		$C_{\phi H1A}$	—	200	—	
		$C_{\phi H2}$	—	200	—	
Final Stage Clock Capacitance		$C_{\phi H1B}$	—	7	—	
Reset Gate Clock Capacitance		$C_{\phi RS}$	—	5	—	

TIMING CHART



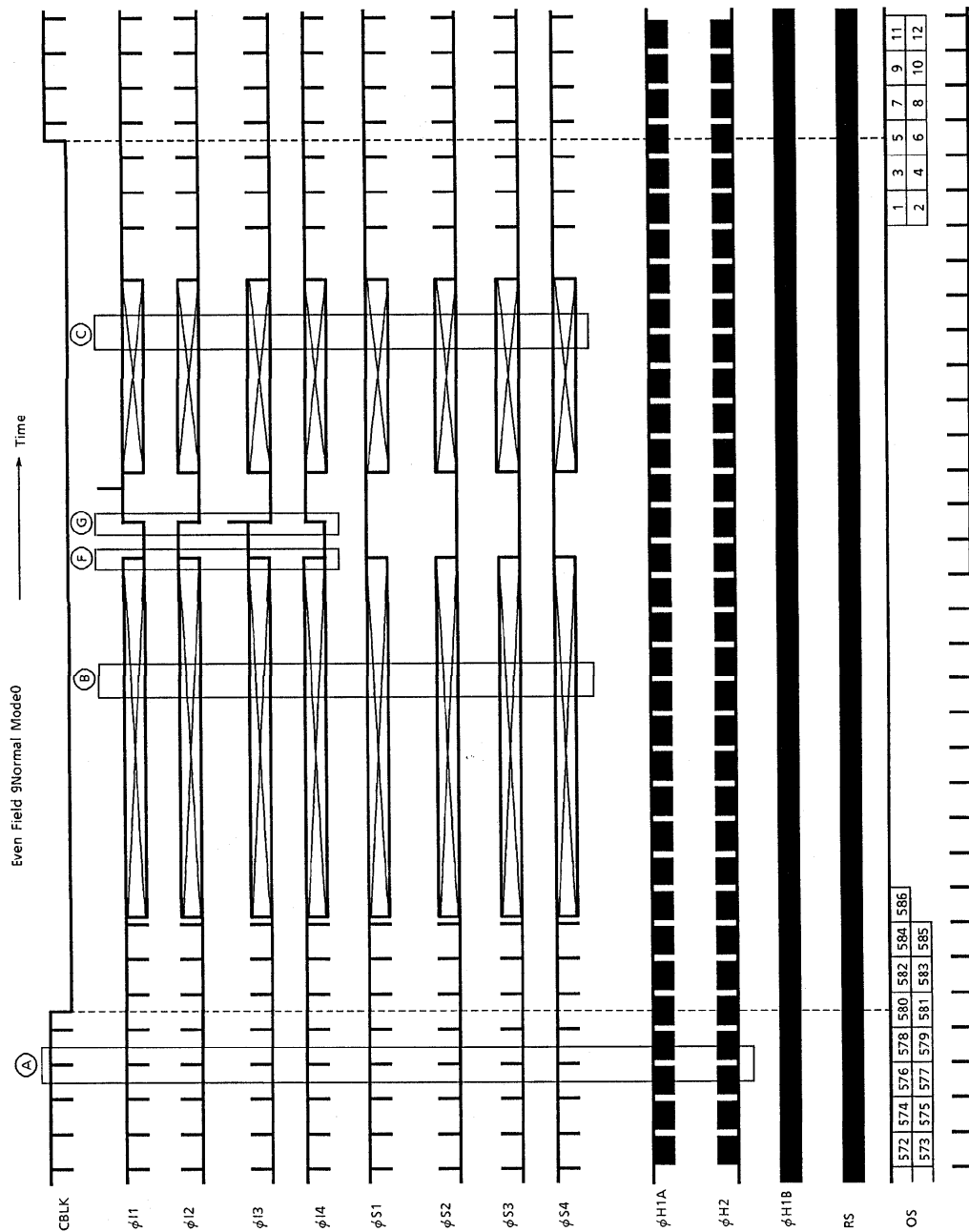
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TIMING CHART



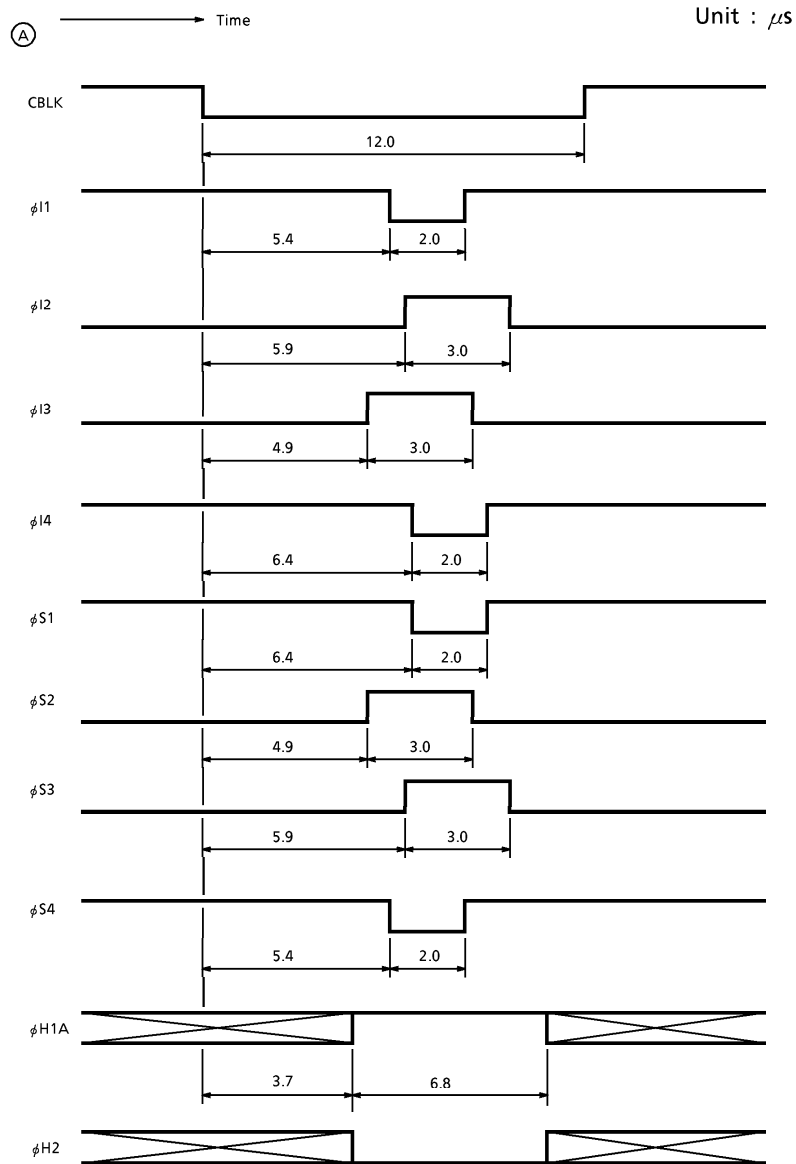
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TIMING CHART (EXPANDED)

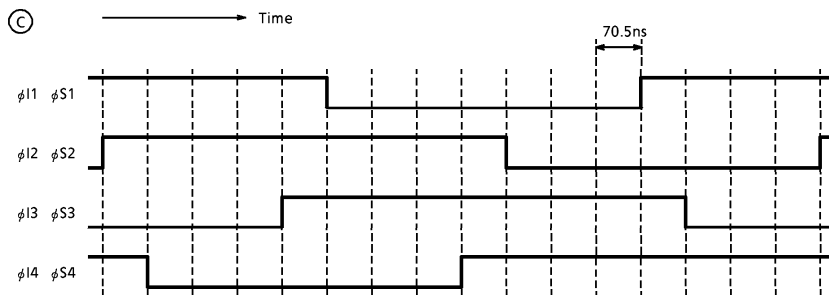
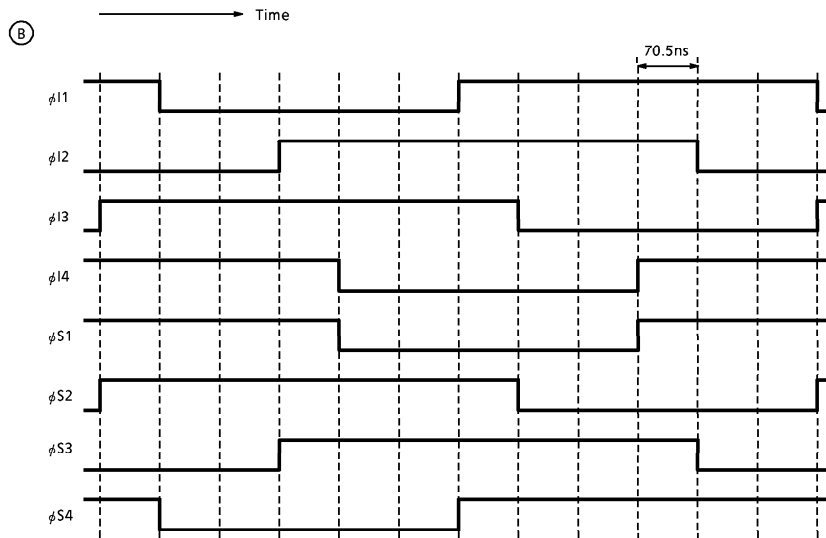


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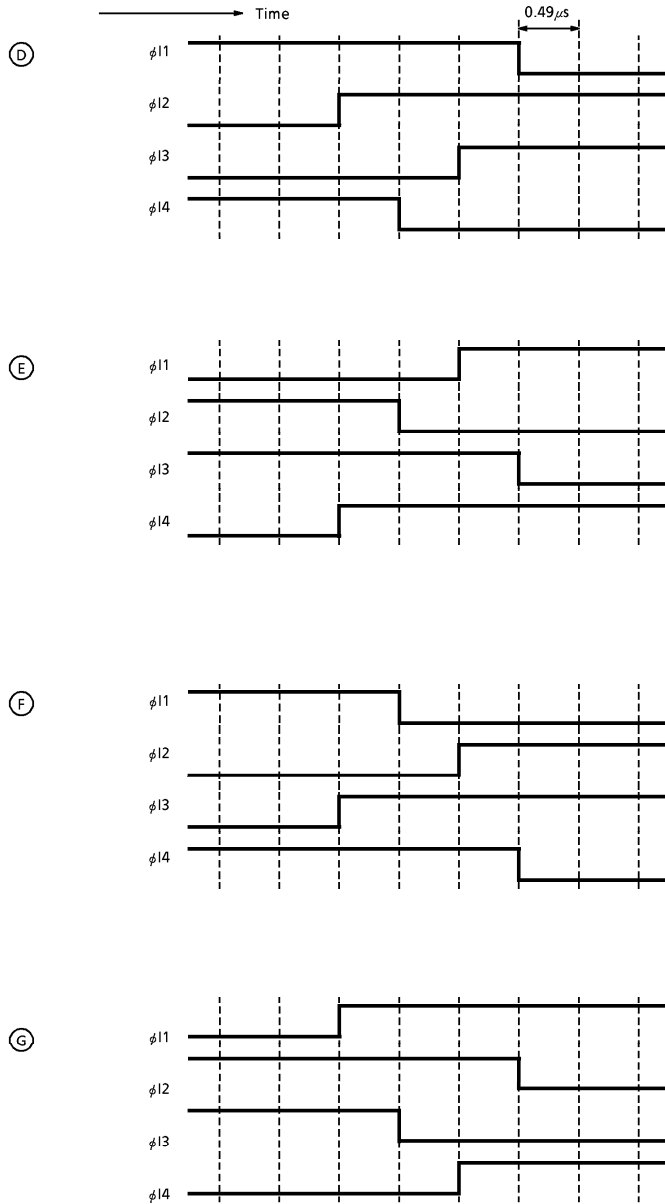
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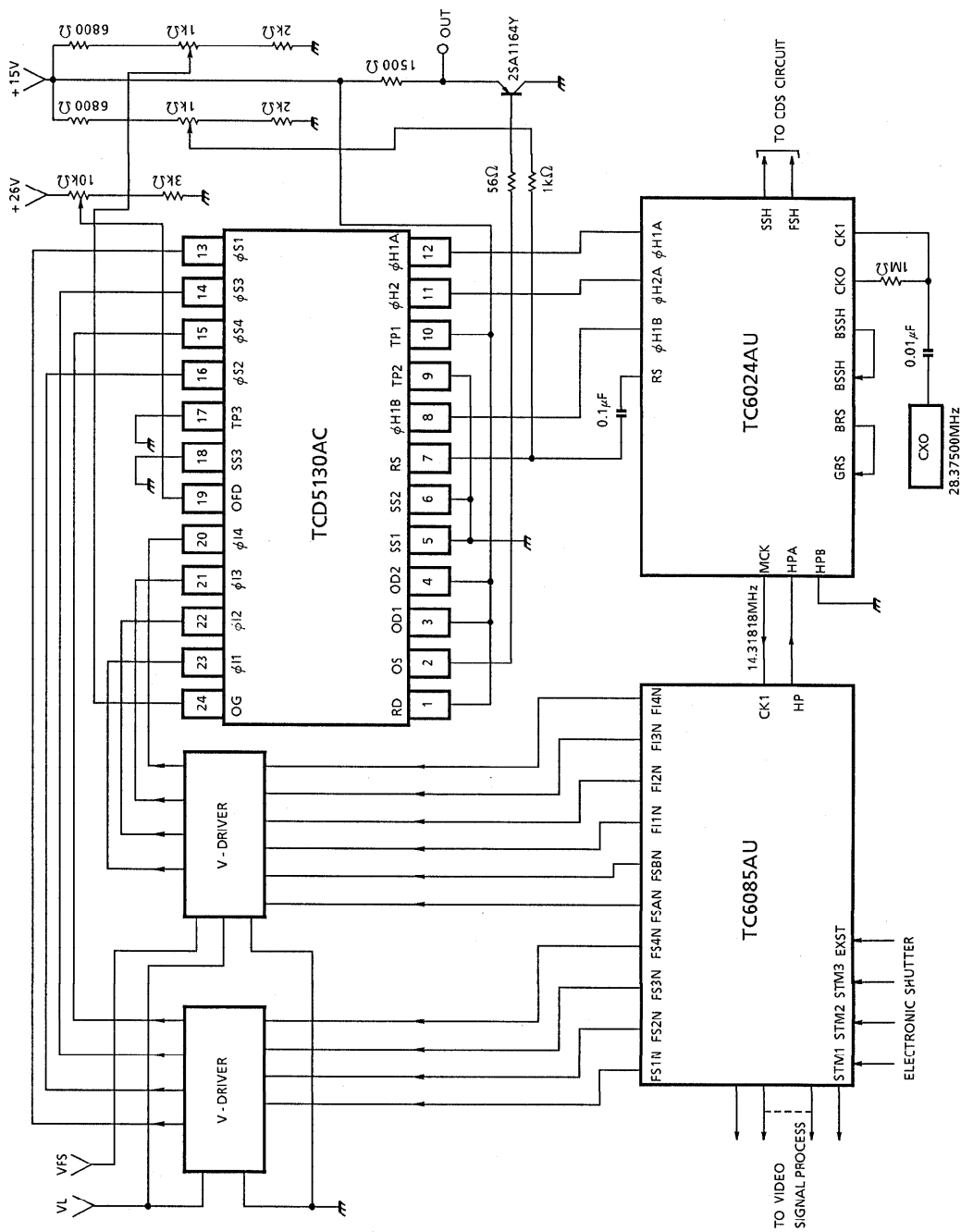
TIMING CHART (EXPANDED)



TIMING CHART (EXPANDED)



TYPICAL DRIVE CIRCUIT



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PRECAUTIONS FOR USE OF CCD IMAGE SENSOR

1. Static Electricity

CCD Image Sensor is protected against static electricity, but inferior puncture mode device due to static electricity is sometimes detected. In handling the device, it is necessary to execute the following static electricity preventive measures, in order to prevent the trouble rate increase of the manufacturing system due to static electricity.

- a. Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.
- b. Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.
- c. Ground the tools such as soldering iron, radio cutting plier or pincette.

It is not necessarily required to execute all precaution items for static electricity.

It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.

2 Window Glass

As the dust and station on the glass window of the package will cause black flow on the picture, never fail to clean the glass surface before using. (Blow compressed vapor, and wipe off the dust, and dirt with soft cloth or paper slightly moistened with alcohol).

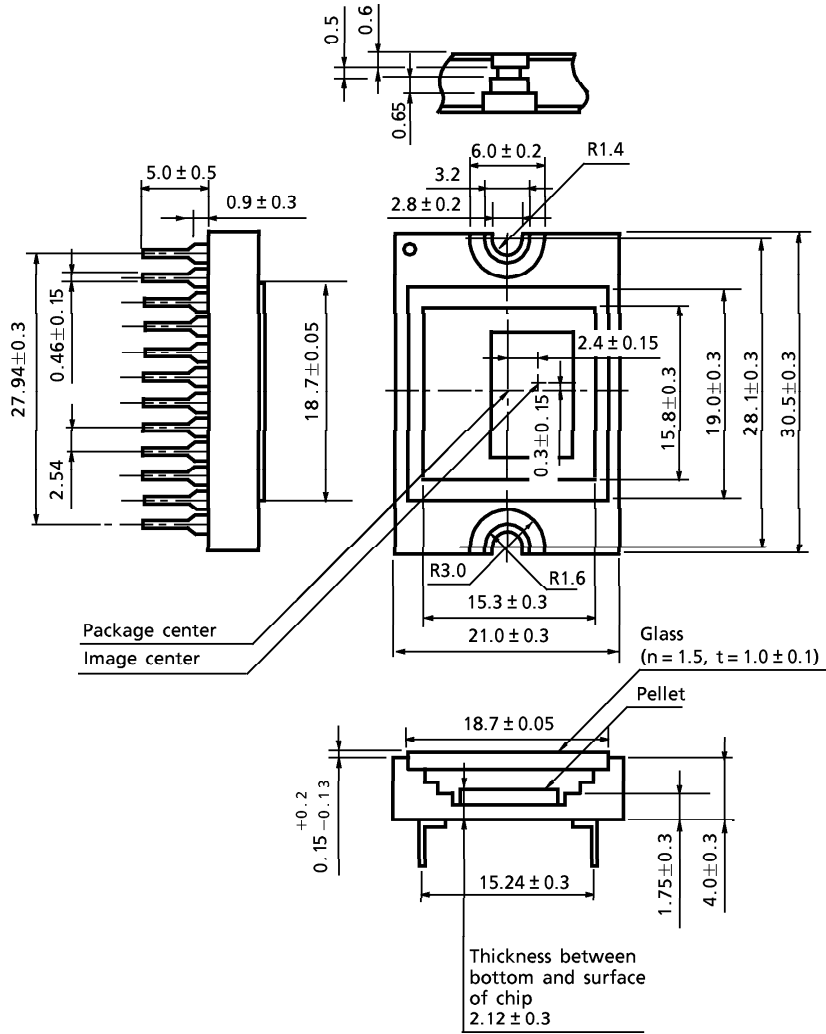
Fully take care for the handling of the device as the window glass will break or a strong friction is given to the window glass surface.

3. Incident Light

CCD image sensor has sensitivity in a wide range zone of light wave length, but its characteristics will sometimes widely change when used with long wave length input light outside the visual light zone.

OUTLINE DRAWING

Unit: mm



Weight : 7.8g (Typ.)

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