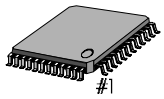
INTRODUCTION

48–QFP–1010E



S1T8527C is a monolithic circuit which can be used in high performance 60MHz MCA type CLP System. The S1T8527C is a subsystem IC for FM / FSK receiving systems and a complete one chip FM / FSK receiver IC for 60MHz system. It's feature includes receiving functions for FM / FSK systems, a compander to remove external noise, and PLL (Phase Lock Loop) of channel selection which blocks surrounding frequency interference.
The S1T8527C can be used with a wide range of FM / FSK VHF bandwidth systems, including cordless phone, and the narrow band voice and data sending / receiving systems.
To make applications easily and simply, peripheral parts are minimized.

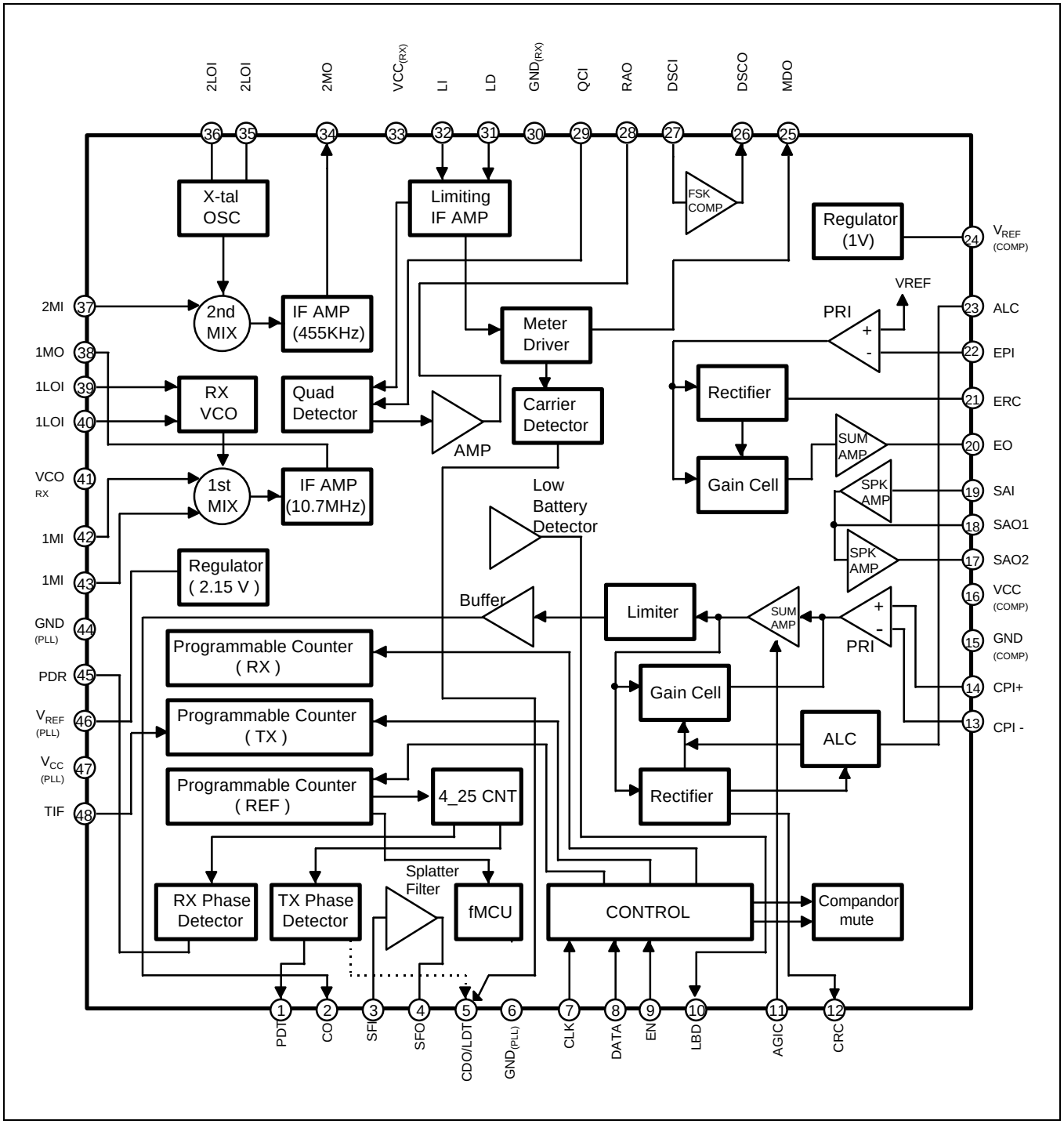
FEATURES

- Operating voltage range: 2.0V — 5.5V
- Typical supply current: 13.5mA at 3.6V
- Built–in low battery detection function (selectable 3.45V, 3.3V, 3.0V, 2.2V, 2.1V)
- Built–in speaker amplifier
- Built–in splatter filter
- Built–in dual conversion receiver, compander and universal PLL
- FM Receiver
  - — Complete dual conversion circuit
  - — Excellent input sensitivity (0.7μVrms at 12dB SINAD)
- Compader
  - — Easy gain control to use external component
  - — Included ALC (Automatic Level Control) circuit
  - — Included Mute logic
- Universal PLL
  - — RX (TX) divided counter range: 1/16 — 1/16383
  - — Reference frequency divided counter range: 1/16 — 1/4095
  - — Lock detector signal output
  - — Serial interface with MCU for controlling each block

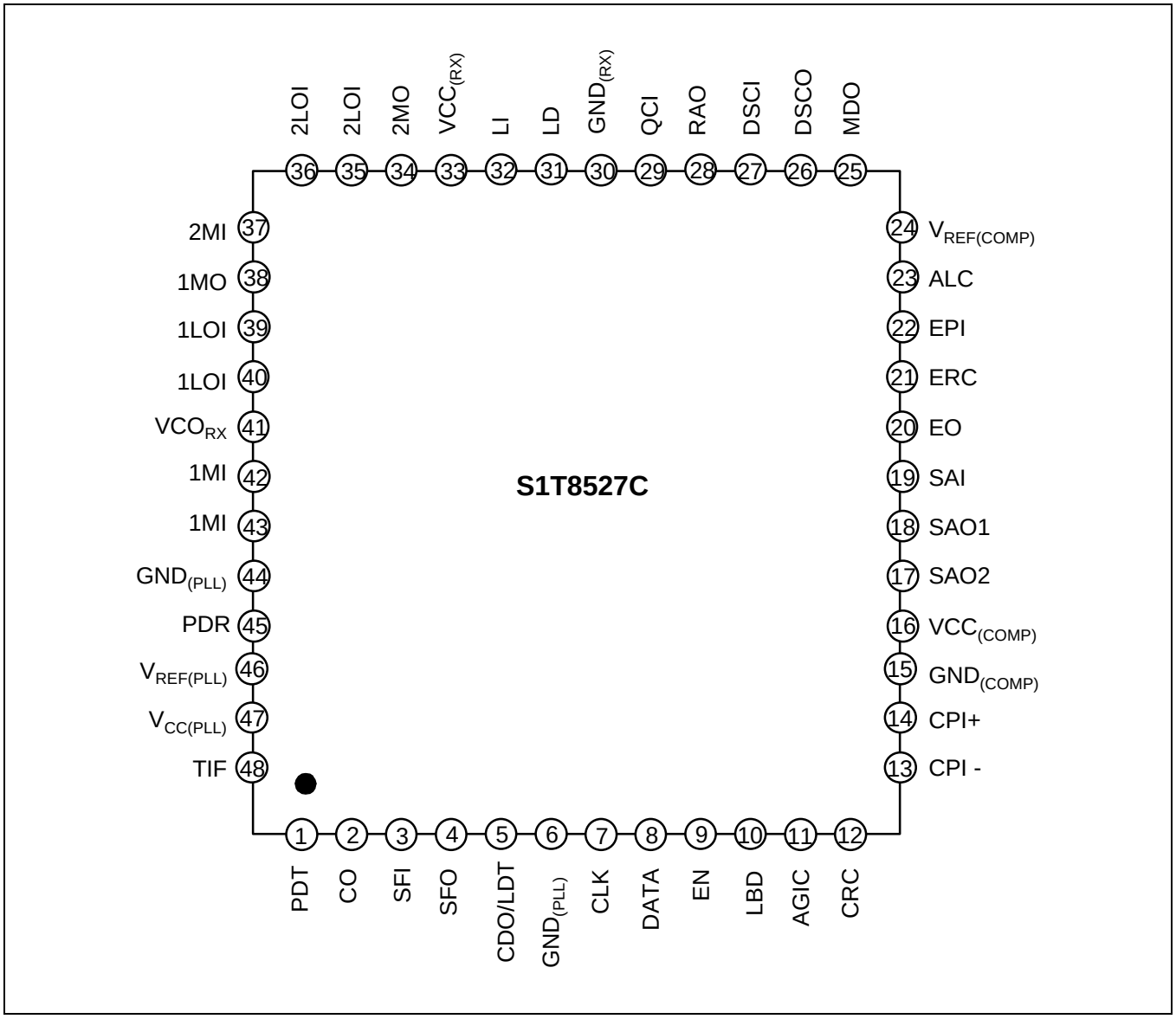
ORDERING INFORMATION

Device	Package	Operating Temperature
S1T8527C01-Q0R0	48–QFP–1010E	–20°C — + 70C

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No	Symbol	Description
1	PDT3	Phase detector output terminal of the transmitter at PLL. If $f_{TX} > f_{REF}$ or f_{TX} is leading $\rightarrow$ the output is negative pulse If $f_{TX} < f_{REF}$ or f_{TX} is lagging $\rightarrow$ the output is positive Pulse if $f_{TX} = f_{REF}$ and the same phase $\rightarrow$ the output is High Impedance
2	CO	Compressor output terminal of compander; connected to the splatter filter amp input terminal.
3	SFI	Input terminal of Splatter filter amp.
4	SFO3	Output terminal of Splatter filter amp.
5	LDT/CDO	LDT: Output terminal of transmitter lock detector in PLL block. The output is low if PLL is in lock state and the output is high if PLL is in unlock state. CDO: As an output terminal of the carrier detector buffer, connected to (RSSI) terminal of MCU. This pin outputs the contents of Meter Driver buffer which is turned on / off, according to the signal level detected by Meter Driver.
6	GND_{PLL}	Ground. Ground of logic section at PLL.
7 8 9	CLK DATA EN	These pins are serial interface terminals for programming reference counter, auxiliary reference counter, TX channel counter, RX channel counter and control block that controls internal each block with test mode and power saving mode.
10	LBD	Low Battery Detecting output. (Selectable 3.45V, 3.3V, 3.0V, 2.2V, 2.0V). During the normal operation, output level is low, but it is high at low battery detection. As this pin is an open collector type, it requires a pull - up resistor.
11	AGIC	This pin bypasses AC elements at the feedback loop which come from the SUM amp block of COMPRESSOR. A capacitor should be connected between this terminal and GND. (C = 2.2uF)
12	CRC	Converts waveform from the full wave rectifier to DC element at the rectifier block of Compressor. (RC = 33msec)
13	CPI -	Pre-amp inverting input terminal of Compressor. Adjusts the negative feedback loop gain. (in application, gain is 5)
14	CPI +	Pre-amp non-inverting input terminal of Compressor. Used as an input terminal for voice signals.
15	$GND_{(COMP)}$	Ground of Compander block.
16	$Vcc_{(COMP)}$	Supply voltage. Power supply terminal of Compander.
17	SAO 2	Output terminal of speaker amp 2. This signal is the same as SAO1 output, but phase difference is180° for SAO1. DC voltage level is (Vcc — 0.7V) / 2.

PIN DESCRIPTION (Continued)

Pin No	Symbol	Description
18	SAO 1	Output terminal of Speaker amp 1. DC voltage level is (Vcc — 0.7V) / 2.
19	SAI	Speaker Amp 1 input terminal. Between this terminal and Expander output terminal, uses a AC coupled.
20	EO	Output terminal of Expander, from which a regenerated voice signals are emitted.
21	ERC	Converts waveform from the full wave rectifier to DC element at the rectifier block of Expander. (RC = 33 msec)
22	EPI –	Pre-amp inverting input terminal of Expander. Adjusts the negative feedback loop gain. (in application, gain is 5).
23	ALC	Reference current input terminal of Automatic Level Control (ALC); Adjusts THD of compressor output voltage to less than 3% or limits the frequency deviation of TX if the input is higher than a certain level. The ALC circuit may be turned off depending on the ALC reference current or the magnitude of output voltage may be limited if it is higher than a certain level.
24	$V_{REF(COMP)}$	Reference voltage (V_{REF}= 1V). Supplies a regulator voltage to the Compressor and Expander of COMPANDER.
25	MDO	Output terminal of the Meter Driver. Amplitude of RF input signal for useful frequency is detected by Meter Driver circuit. The Meter Driver circuit has perfect linear characteristic of 60dB range for input signal level. (0.1μA / dB).
26	DSCO	Output terminal of Data Slicing comparator. Separates Frequency Shift Keying (FSK) serial data and executes data shaping and limiting.
27	DSCI	Input terminal of Data slicing comparator. Non-inverting type with the negative input terminal biased to 1/2 Vcc.
28	RAO	Recovered Audio Output terminal. Voice signals detected by the Quadrature Detector are amplified and then output through this terminal.
29	QCI3	Quadrature coil input terminal. The 455kHz oscillator circuit is an Lp = 680uH, Cp = 180pF valued LC tank circuit. Voice signals are detected by mixture of 455kHz (by phase difference) which is converted from mixer 2.
30	GND_{RX}	Ground . Ground for Receiver.
31 32	LD LI	Limiter input and decoupling terminal. Removes amplitude modulation elements caused by fading or FM signal noise. Limiting IF amplifies and limits the second intermediate frequency, 455kHz.The input impedance of the limiting IF amplifier is set to 1.5kΩ. While FM waves are transmitted with constant magnitude, their magnitudes are slightly modulated due to reflection from obstacles, fading phenomenon, noise wave, and mixing with AM wave elements before entering the receiver's antenna.The limiter makes amplitude uniform by removing these AM wave elements.

PIN DESCRIPTION (Continued)

Pin No	Symbol	Description
33	$V_{CC(RX)}$	Supply voltage. Supplies power to the Receiver.
34	2MO3	Output terminal of Mixer 2. Second intermediate frequency (455kHz), generated by mixing first intermediate frequency (10.7MHz) and Second Local Oscillator is output.
35 36	2LOI 2LOI	Input terminal of second local oscillator. Generates second local oscillator frequency to convert output from mixer 1 (10.7MHz) into second intermediate frequency. It is an oscillator with crystal of 10.24MHz and 10.245MHz.
37	2MI	Input terminal of mixer 2. Output from mixer 1 is entered to mixer 2 input terminal via 10.7MHz ceramic filter. Second mixer converts frequency to second intermediate frequency (455kHz: AM IF).
38	1MO3	Output terminal of mixer 1. The signal from mixer 1 and the frequency of the first local oscillator are mixed to produce the first intermediate frequency, which is the output through this terminal. The output terminal is an emitter follower with an output impedance of 330Ω to match the 330Ω input/output impedance of the 10.7MHz ceramic filter.
39 40	1LOI 1LOI	Input terminal of the first local oscillator. The local oscillator is a voltage controlled oscillator. local oscillation frequency and received frequency are mixed at mixer 1 and then converted to the first intermediate frequency of 10.7MHz or 10.695MHz.
41	VCO_{RX}	The terminal which variable capacitor is included in the chip. Used as an input terminal where 1st local oscillation frequency is changed by varying the capacitor connected between 1st local oscillator terminals.The internal variable capacitor has the value of 18.73 ~ 15.86pF depending on the applied voltage. (1.0 ~ 2.0 V).
42 43	1MI 1MI	Input terminal of Mixer 1. This mixer is made of double balanced multiplier. The received signal amplified at RF AMP is input to this terminal.
44	$GND_{(PLL)}$	Ground. Ground for analog at PLL
45	PDR	Phase detector output terminal of the receiver at PLL. If $f_{RX} > f_{REF}$ or f_{RX} is Leading → The output is negative pulse If $f_{RX} < f_{REF}$ or f_{RX} is Lagging → The output is positive pulse If $f_{RX} = f_{REF}$ and the same phase → The output is high impedance
46	$V_{REF(PLL)}$	PLL voltage reference output pin. An internal voltage regulator provides a stable power supply voltage for the RX and TX PLLs.
47	$V_{CC(PLL)}$	Power supply terminal of PLL.
48	TIF	Input terminal of TX channel counter. AC coupling with TX VCO. Minimum input level is 300mVp-p (at 60MHz).

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Maximum Supply Voltage	V_{CC}	5.5	V
Power Dissipation	P_D	600	mW
Operating Temperature	T_{OPR}	–20 — + 70	°C
Storage Temperature	T_{STG}	– 55 — + 150	°C

CURRENT CONSUMPTION AT EACH MODE (VCC = 3.6V)

MODES	Min.	Typ.	Max.
Inactive mode	–	350uA	600uA
RX mode	–	6.6mA	–
Communication mode (Active mode)	–	13.5mA	

CURRENT CONSUMPTION IN EACH BLOCK (VCC = 3.6V)

MODES		Min.	Typ.	Max.
Receiver part		–	5.0mA	7.5mA
Expander part		–	1.4mA	2.1mA
Speaker part		–	1.7mA	2.5mA
compressor part		–	3.0mA	4.5mA
PLL	RX part	–	1.6mA	2.4mA
	TX part	–	0.8mA	1.2mA

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	Vcc	–	2.0	–	5.5	V

RECEIVER

(V_{CC} = 3.6V, f_C = 49.7MHz, f_{DEV} = ±3kHz, f_{MOD} = 1kHz,Ta = 25°C, unless otherwise specified)

Input for –3dB Sensitivity	V_{LIM}	–3dB Point	–	0.7	2.0	µVrms
Input for 20dB Sensitivity	$V_{I(SEN)}$	Modulation Input	–	0.7	2.0	µVrms
S/N Ratio	S/N	Modulation Input No Modulation Input	48	55	–	dB
Recovered Audio Output	$V_{O(RA)}$	RFin = 1mVrms	145	185	225	mVrms
Noise Output Level	V_{NO}	RFin = No Input	–	130	205	mVrms
Recovered Audio Output Voltage Drop	$V_{O(RAD)}$	Vcc = 5V → 2V RFin = 1mVrms	–8	–3.3	–	dB
Detect Output Voltage	$V_{O(DET)}$	RFin = 1mVrms	1.0	1.5	2.0	V
Carrier Detector Threshold	$V_{TH(DET)}$	RFin = No Input	0.49	0.60	0.73	V
Comparator Threshold Voltage Difference	ΔV_{TH}	V_{COMP} = 150mVp-p R_L = 180kΩ	70	110	150	mV
Comparator Output Voltage 1	V_{OH}	V_{COMP} = 150mVp-p RL = 180kΩ	2.7	3.0	–	V
Comparator Output Voltage 2	V_{OL}	V_{COMP} = 150mVp-p R_L = 180kΩ	–	0.25	0.5	V
First Mixer Conversion Voltage Gain	$\Delta G_{V(1M)}$	$V_{I(43)}$ = 1mVrms $R_{L(38)}$ = 330Ω	14	18	22	dB
Second Mixer Conversion Voltage Gain	$\Delta G_{V(2M)}$	$V_{I(37)}$ = 1mVrms $R_{L(34)}$ = 1.5kΩ	17	21	25	dB
Detector Output Distortion	THD_{DET}	RFin = 1mVrms	–	1.5	2.5	%
Detector Output Resistance	$R_{O(DET)}$	RFin = 1mVrms	–	1.2	–	kΩ
Detector Output DC Voltage Change Ratio	$\Delta V_{O(DET)}$	RFin = 1mVrms	–	0.15	0.23	V/kHz
Meter Drive Slope	MDS		70	100	135	nA/dB
First Mixer Input Resistance	$R_{I(1M)}$	fc = 50MHz	500	690	–	Ω
First Mixer Input Capacitance	$C_{I(1M)}$	fc = 50MHz	–	7.2	10	pF
Limiter Input Sensitivity	$V_{I(LIM)}$	fc = 455kHz, 20dB SINAD	–	100	250	µVrms
Second Mixer Input Sensitivity	$S_{V(2M)}$	fc = 10.7MHz, 20dB SINAD	–	10	25	µVrms

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
First Mixer 3rd Order Sensitivity	3RD	–	–	-22	–	dBm
Low Battery Detector	LBD3	LBD0— LBD3 = 0 (Default) Only LBD2 = 0 Only LBD1 = 0	–0.15	3.45 3.3 3.0	0.1	V
		Only LBD3 = 0 LBD0 — LBD3 = 1	–0.1	2.2 2.1	0.075	
AM Rejection Ratio	AMRR	RFin = 1mVrms — 10mVrms AM MOD = 30%	25	25	–	dB

Compressor

(Vcc = 3.6V, fc = 1kHz, Ta = 25°C, unless otherwise specified)

Reference Voltage	V_{REF}	No Signal	0.9	1.0	1.1	V
Standard Output Voltage	Vo(com)	Vinc = 13mVrms (0dB), Ralc = GND	255	300	345	mVrms
Compressor Gain Difference	$\Delta GV1_{(COM)}$	Vinc=1.3mVrms (–20dB), ΔGv1 (COM) = 20 × log (Voc1/Voc) + 10K	–1.0	–0.5	–	dB
	$\Delta GV2_{(COM)}$	Vinc = 0.13mVrms (–40dB) ΔGv2 (COM) = 20 × log (Voc2/Voc) + 20K	–2.0	–1.0	–	dB
Compressor Output Distortion	THD_{COM}	Vinc = 0dB	–	0.5	1.0	%
Mute Attenuation Ratio	ATT_{MUTE}	Vinc = 0dB	60	80	–	dB
Compressor Limiting Voltaget	$V_{LIM(COM)}$	Vinc = Variable	1.41	1.65	1.83	Vp-p
ALC	V_{ALC}	I_{ALC} = 8uA (R_{ALC} = 120kΩ)	280	330	380	mVrms
Splatter filter	Vo(SF)	VINC = 13mVrms = 0dB	255	300	345	mVrms

Expander

(Vcc = 3.6V, fc = 1kHz, Ta = 25°C, unless otherwise specified)

Standard Output Voltage	$V_{O(EXP)}$	Vine=30mVrms (0dB)	104	130	156	mVrms

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Expander Gain Difference	$\Delta G_{V1(EXP)}$	Vine = 9.5mVrms (–10dB) ΔGv1(EXP) = 20 × log (Voe1/ Voe) + 20	0	0.5	1.0	dB
	$\Delta G_{V2(EXP)}$	Vine = 3mVrms (–20dB) ΔGv2 (EXP) = 20 × log (Voe2/Voe) + 40T	0	1.0	2.0	dB
	$\Delta G_{V3(EXP)}$	Vine = 0.95mVrms (–30dB) ΔGv3 (EXP) = 20 × log (Voe3/Voe) + 60K	0	1.5	3.0	dB
Expander Output Distortion	THDEXP	VinE = 0dB	–	0.5	1.0	%
Mute Attenuation Ratio	ATTMUTE	VinE = 0dB	60	80	–	dB
Expander Maximum Output Voltage	$V_{OEXP(MAX)}$	VinE = Variable THD = 10%l	500	600	–	mVrms
Speaker amp output 1	Vo(SA1)	VINE = 30mVrms = 0 dB	104	130	156	mVrms
Speaker amp output 2	Vo(SA1)	VINE = 30mVrms = 0 dB	104	130	156	mVrms

PLL

(Vcc = 3.6V, Ta = 25°C, unless otherwise specified)

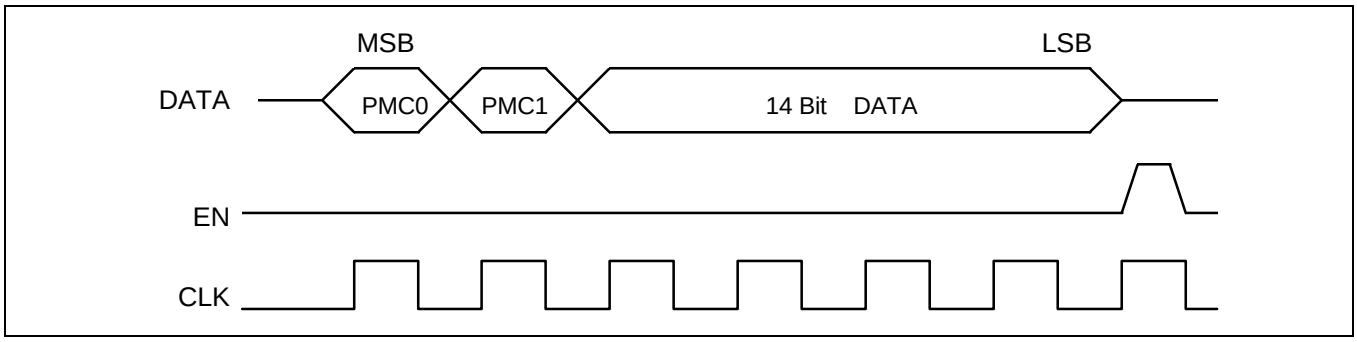
Operating Current	I_{CCPLL}	Vcc = 3.6V	–	2.0	3.5	mA
Input Current	I_{IH}	Vin = Vcc	–	–	5	µA
	I_{IL}	Vin = 0V	–5	–	–	µA
Input Voltage	V_{IH}	–	Vcc-0.3	–	–	V
	V_{IL}	–	–	–	0.3	V
Output Current	I_{OH}	Vout = Vcc	0.3	–	–	mA
	I_{OL}	Vout = 0V	0.3	–	–	mA
Output Voltage	V_{OH1}	PDT, PDR: Io = –0.3mA (Sourcing)	Vcc-0.4	–	–	V
	V_{OL1}	PDT, PDR: Io = 0.3mA (Sinking)	–	–	0.4	V
	V_{OH2}	LD, fMCU: Io = –0.1mA (Sourcing)	Vcc-0.5	–	–	V
	V_{OL2}	LD, fMCU: Io = 0.1mA (Sinking)	–	–	0.5	V
PLL regulator voltage	V_{PLLREG}		1.95	2.15	2.25	V

PLL PROGRAM SUMMARY

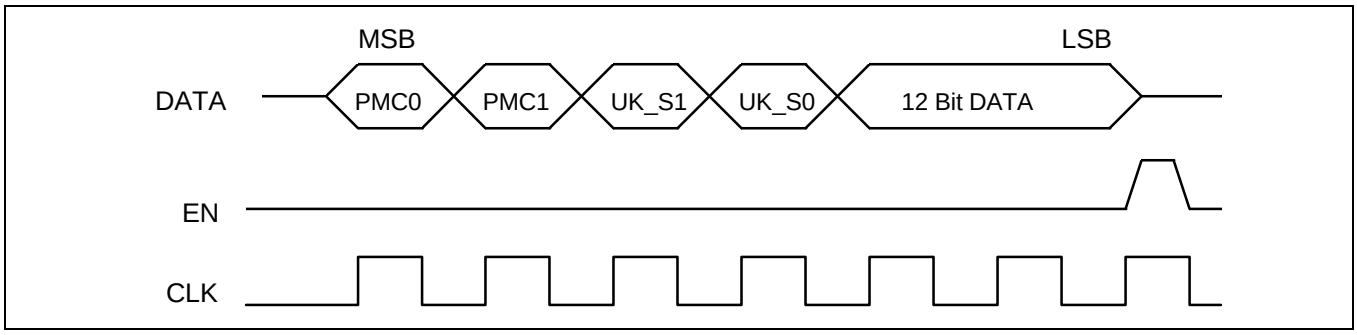
MCU (MICOM) SERIAL INTERFACE (MSB : 1ST INPUT)

Use CLK (Pin 7), DATA (Pin 8) , EN (Pin 9) terminals for program. DATA and CLK terminals are used for loading data to internal Shift - Register. When EN terminal is 'Low' It is possible to program TX-Channel Counter, RX - Channel Counter and various control functions of PLL. When EN terminal is 'High' Program 1st Local Oscillator Capacitor Selection in receiver for U.S.A - 25 CH function.

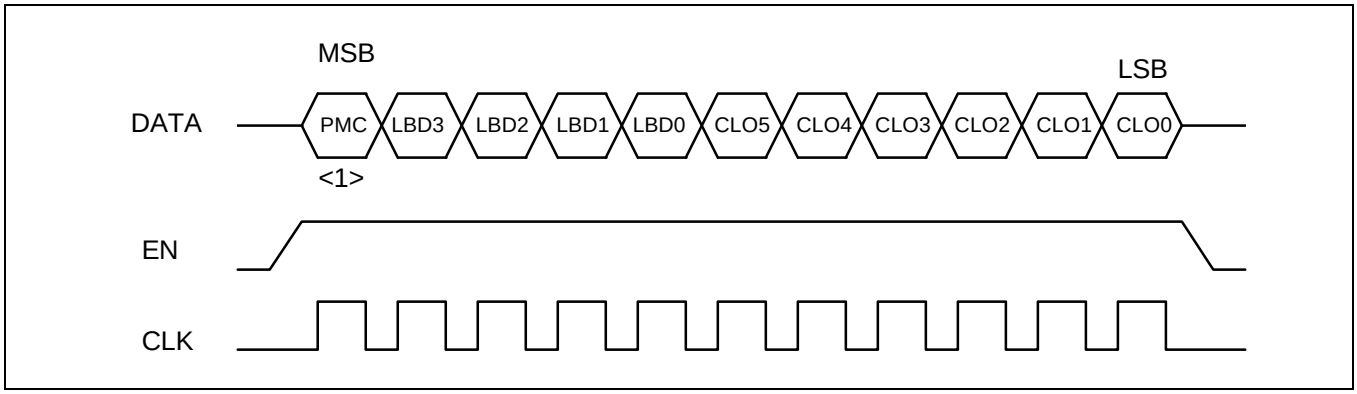
— TX - Register, RX-Register, Control Register



— Reference - Register



— RECEIVER -1st local oscillator internal capacitor selection register & low battery detector voltage register [CLO_LBD-Register]



- **Programmable Counter**

— RX - counter: Setting frequency for RX.VCO (14 Bits --> 1/16 — 1/16383)
[Default_CH. = USA_#21 (REMOTE): 36.075MHz (Div._NO = 7215)]c

< RX. Register (16bits) >

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Name	PMC0	PMC1	D13	D12	D11	D10	D9	D8
Default value 7215	*		0	1	1	1	0	0

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	D7	D6	D5	D4	D3	D2	D1	D0
Default value 7215	0	0	1	0	1	1	1	1

— TX - counter: Setting frequency for TX.VCO (14 Bits --> 1/16 — 1/16383)
[Default_CH. = USA_#21 (REMOTE): 49.830MHz (Div._NO = 9966)]'

< TX. Register (16 bits) >

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Name	PMC0	PMC1	D13	D12	D11	D10	D9	D8
Default value 9966	*		0	1	1	1	0	0

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	D7	D6	D5	D4	D3	D2	D1	D0
Default value 9966	1	1	1	0	1	1	1	0

*** Program mode control**

PMC0	PMC1	Program mode	PMC0	PMC1	Program mode
0	0	Control Block	0	1	UPLL_RX. Block
1	0	UPLL_Ref. Block	1	1	UPLL_TX. Block

— Ref - counter: Setting reference frequency for phase detector (12 Bits --> 1/16 ~ 1/4095)
[Default_Divider = 2048, X-tal_OSC = 10.240 MHz --> Fref = 5kHz]

< Ref. Register (16bits) >

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Name	PMC0	PMC1	UK_S1	UK_S0	D11	D10	D9	D8
Default value 2048	*		Ref.freq. selection for United KingdomD		1	0	0	0

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	D7	D6	D5	D4	D3	D2	D1	D0
Default value 2048	0	0	0	0	0	0	0	0

— UK_Selection

UK_S0	UK_S1	FR1	FR2	FrefTX	FrefRX
0	0	fREF (A)	–	fREF (A)	fREF (A)
1	0	fREF (A)	fREF/4 (B)	fREF/4 (B)	fREF/4 (B)
0	1	fREF/4 (B)	fREF/25 (C)	fREF/4 (B)	fREF/25 (C)
1	1	fREF/4 (B)	fREF/25 (C)	fREF/25 (C)	fREF/4 (B)

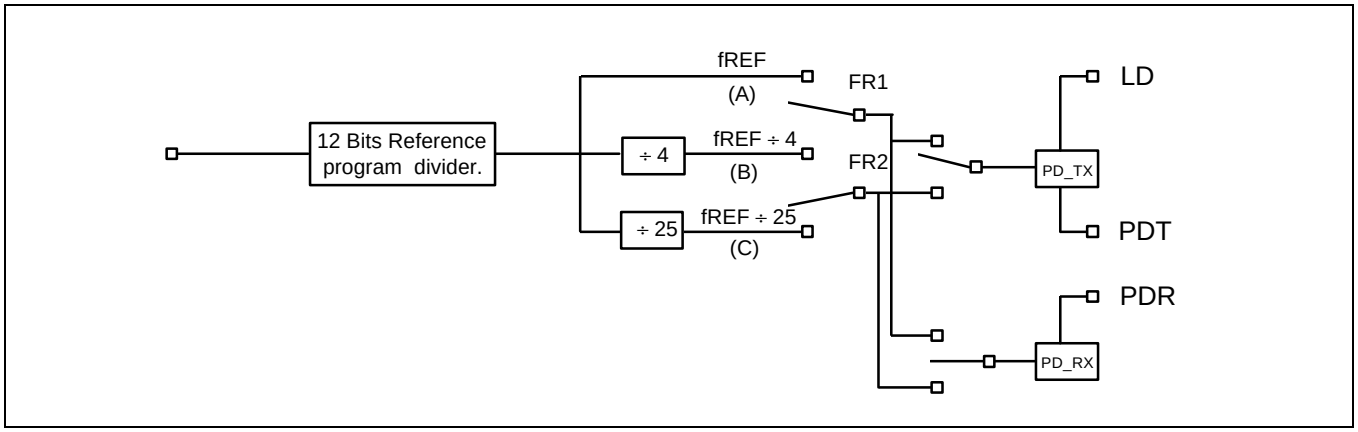


Figure 1. < Reference frequency selection >

- **Control program**

— Control register (16 Bits)

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Name	PMC0	PMC0	-	PLL_{TX}-BS	CO_M	CO_BS	CO_BS	EX_BS
Description	Program Mode Control_0	Program Mode Control_1	Don't Care	PLL_Tx Battery Save	Compress or Mute Selection	Compress or Battery Save	Expander Mute Selection	Expander Battery Save
Function	* Program Latch Assign		Don't Care	0:Normal (PLL_TX-On) 1:PLL_TX Power-Off	0:Normal 1:Mute	0: CO-On 1: Normal (CO-part Power-Off)	0:Normal 1:Mute	0: EX-On 1: Normal (EX-part Power-Off)

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LDT_ CDO	LBD-BS	Rx-Bs	–	–	–	TEST2	TEST1
Description	LDT or CDO Select	Low Battery Detector Battery Save	RX Battery Save	Don't care	Don't care	Don't care	TEST Mode 2	TEST Mode 1
Function	LDT or CDO Select	0:Normal (LBD-ON) 1:LBD-Part Power-Off	0:Normal (RX-ON) 1:RX-Part Power-Offf	–			* * * Function Test On each block of UPLL	

*** TEST Mode & LDT-CDO Mode

LDT/CDO	TEST1	TEST2	LDT / CDO	Remark
0	0	0	Rx block CDO	Default
	1	0	Rx block CDO	
	0	1	4_25cnt block FR2	
	1	1	4_25cnt block FR2	
1	0	0	PLL block LDT	
	1	0	PLL block LDT	
	0	1	PLL block LDT	
	1	1	Test PLL_TX	

- **Operating internal circuit blocks in each mode**

Mode (state)	Operating circuit blocks
Active state (Communication mode)	PLL regulator/MICOM I/F (Data, CLK, EN) / 2nd local oscillator / Receiver / 1st local oscillator / RX PLL / Carrier detector / FSK comparator / Low battery detector / TX PLL / Expander & speaker amp / Compressor / Splatter filter amp
Receiving mode	PLL regulator / MICOM I/F (Data, CLK, EN)/ 2nd local oscillator / Receiver / 1st local oscillator / RX PLL / Carrier detector / FSK comparator / Low battery detector.
Inactive state	PLL regulator / MICOM I/F(Data, CLK, EN)

- **CLO_LBD - Register Program**
  [Rx - 1'st local oscillation internal cap. for U.S.A - 25CH & Alarm sensor detect voltage]

— CLO register (6 bits) : Receiver 1'st local oscillator internal capacitor selection

Bit	Bit10 (MSB)	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PMC	CLO5	CLO4	CLO3	CLO2	CLO1	CLO0
Default Value 0	1 * * * * *	0	0	0	0	0	0
Function	–	0:Normal 1:Internal Cap. for USA 25 Channel = 4.4pF	0:Normal 1:Internal Cap. for USA 25 Channel = 1.0pF	0:Normal 1:Internal Cap. for USA 25 Channel = 3.6pF	0:Normal 1:Internal Cap. for USA 25 Channel = 2.4pF	0:Normal 1:Internal Cap. for USA 25 Channel = 1.2pF	0:Normal 1:Internal Cap. for USA 25 Channel = 0.6pF

*****PMC (Program Mode Control)
PMC = 'HIGH' & EN = 'HIGH' ---> CLO_LBD Register Program Modeap

— Rx - Low Battery Detect Voltage

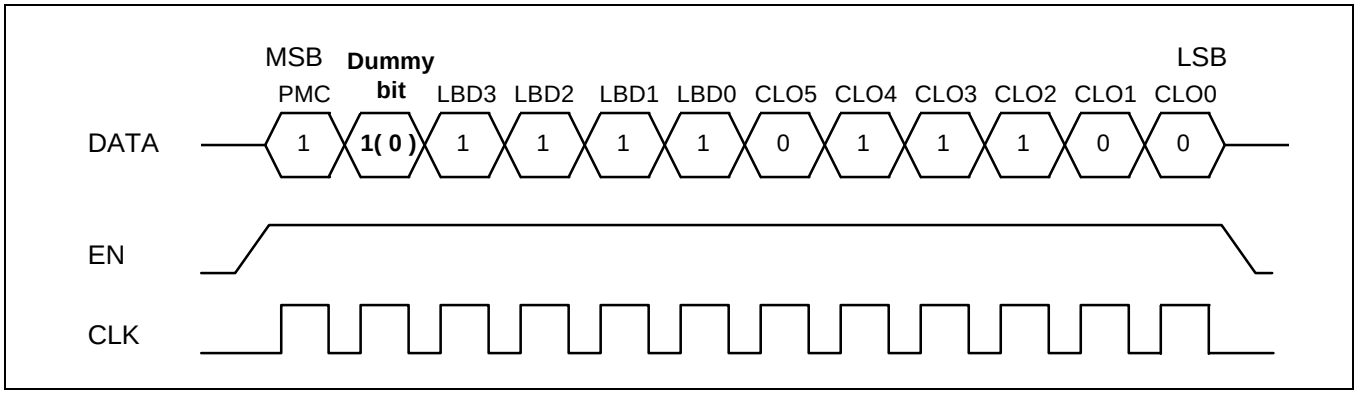
Bit	Bit 10(MSB)	Bit 9	Bit 8	Bit 7	Bit 6	Low Battery Detector Voltagef	Remark
Name	PMC	LBD3	LBD2	LBD1	LBD0		
Default Value	1* * * * *	0	0	0	0	–	Default
Function	1	0	0	0	0	3.45V	–
		1	0	1	1	3.3V	–
		1	1	0	1	3.0V	–
		0	1	1	1	2.2V	–
		1	1	1	1	2.1V	–

***** PMC (Program Mode Control)

PMC = 'HIGH' & EN = 'HIGH' ---> CLO - LBD Register Program Mode

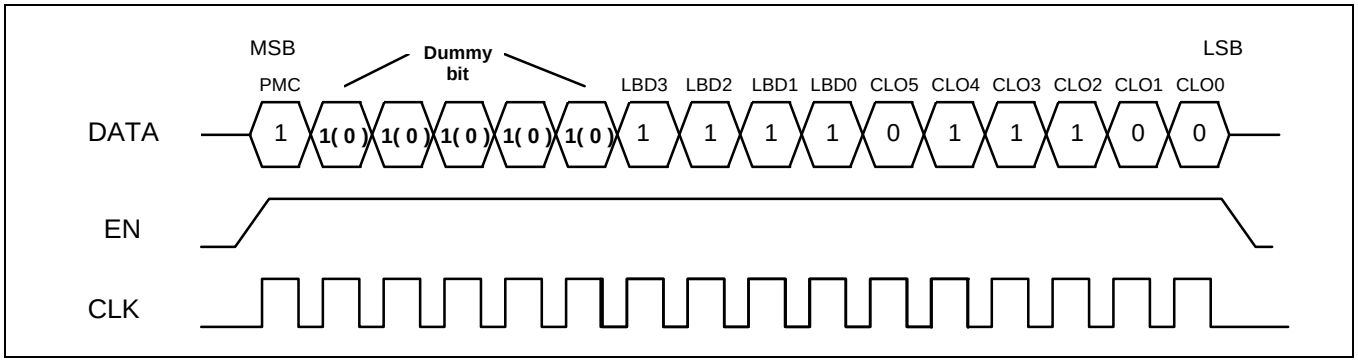
- Example 1 >
  Low battery detector voltage : 2.1V
  U.S.A _CH-#1 (REMOTE) ---> 1st local osc. varicap value = 15.86pF, Internal cap = 7.0pF
  (Ext_L = 0.45uH, EXT_C = 30pF)

— 12 bit data format



In case the 12 bits programming, insert 1 don't care bit (Dummy bit) between PMC and LBD3.

— In case of setting 16 bit data format

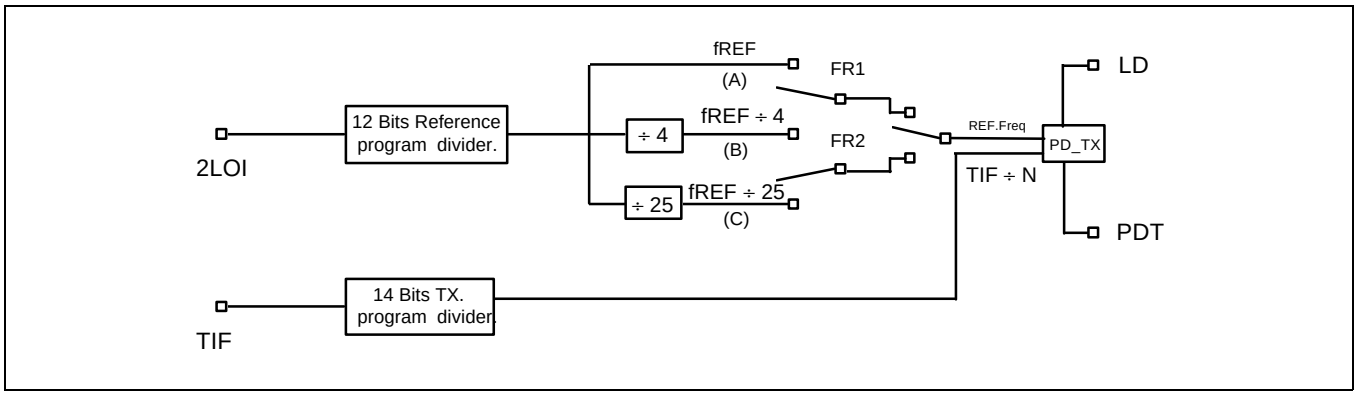


In case of 16 bits programming, insert 5 don't care bits between the PMC and LBD3

EXAMPLE DATA FOR U.S.A 25_CHANNEL SELECTION

1st Local Osc. Internal Capacitor Select						Base Channels	Hand Channels	Varicap Value	External C	External L	Internal C
Bit5 (CLO5)	Bit4 (CLO4	Bit3 (CLO3)	Bit2 (CLO2)	Bit1 (CLO1)	Bit0 (CLO0)	1 — 25CH.	1 — 25CH.	1.0V— 2.0V TYP 1.5Vo	27pF (30pF)	0.45uH	pF
0	0	0	0	0	0	16 — 25CH.		18.73 — 15.86pF	27pF	0.45uH	-
0	0	0	0	0	1		16 — 25CH.	18.73 — 15.86pF	30pF	0.45uH	0.6
0	1	0	0	0	1	01 — 04CH.		18.73 — 15.86pF	27pF	0.45uH	1.6
0	0	0	0	1	0	05 — 10CH.		18.73 — 15.86pF	27pF	0.45uH	1.2
0	0	0	0	0	1	11 — 15CH		18.73 — 15.86pF	27pF	0.45uH	0.6
0	1	1	1	0	0		01 — 06CH.	18.73 — 15.86pF	30pF	0.45uH	7.0
0	1	1	0	1	0		07 — 15CH.	18.73 — 15.86pF	30pF	0.45uH	5.8

- **Phase detector / Lock Detector Output Waveforms**



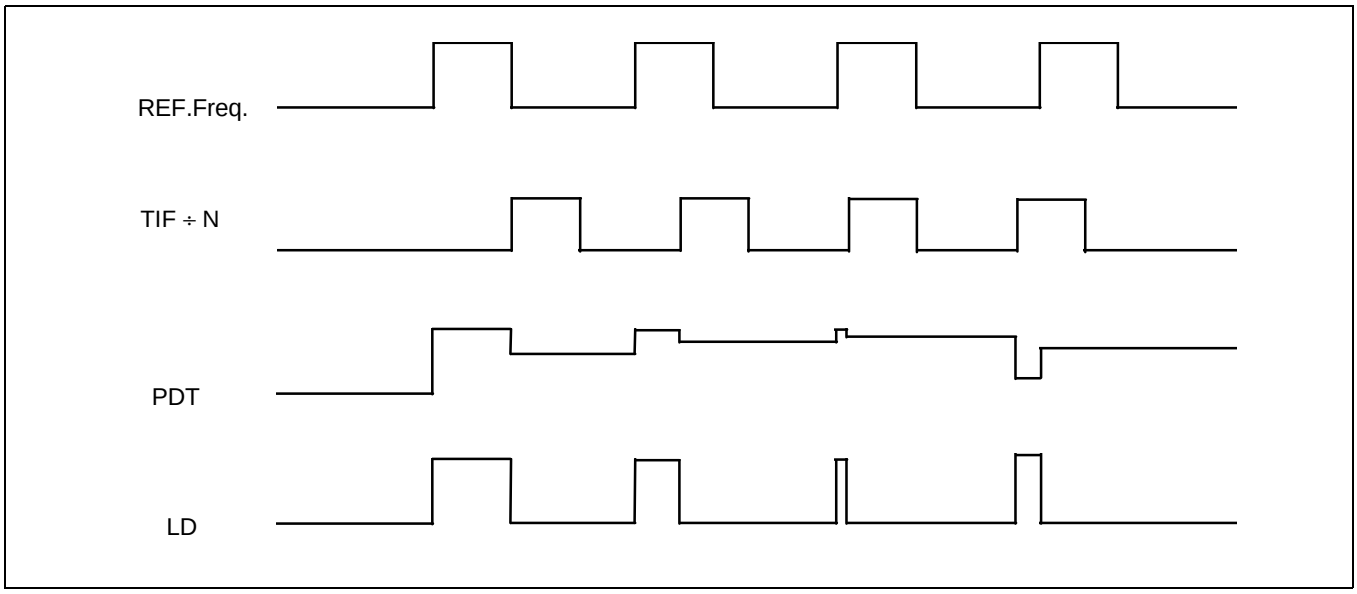
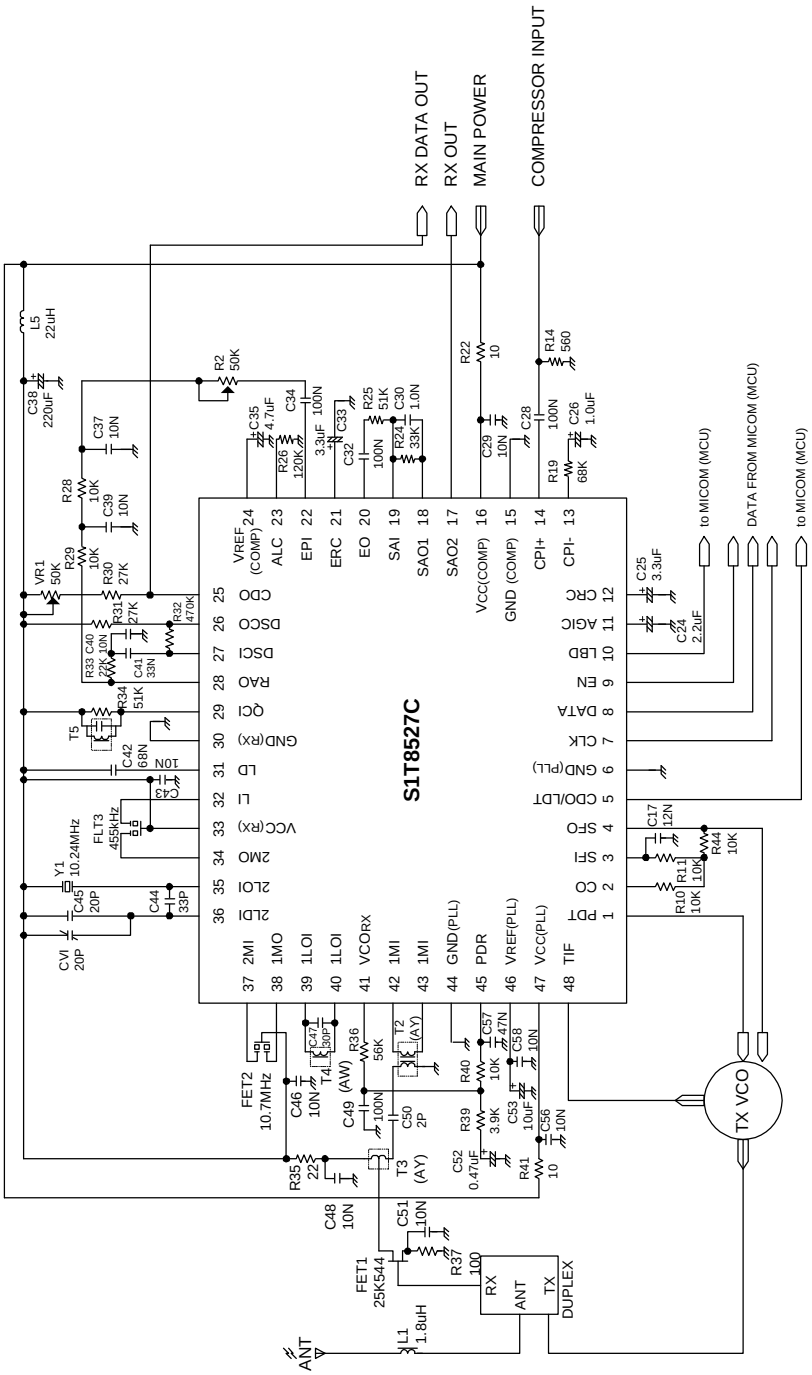


Figure 2. (Phase Detector / Lock Detector Output Waveform)

APPLICATION CIRCUIT (BASE SET)



APPLICATION CIRCUIT (HAND SET)