Description

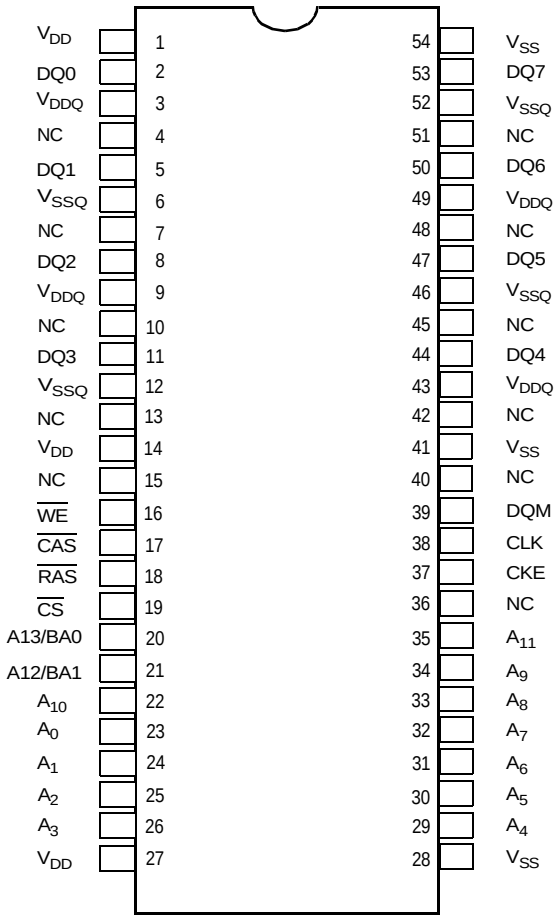
The device is CMOS Synchronous Dynamic RAM organized as 2,097,152 - word x 8-bit x 4-bank. it is fabricated with an advanced submicron CMOS technology and designed to operate from a singly 3.3V only power supply. It is packaged in JEDEC standard pinout and standard plastic TSOP package.

Features

- Single 3.3V (±0.3V) power supply
- High speed clock cycle time : 7/8ns
- Fully synchronous with all signals referenced to a positive clock edge
- Programmable $\overline{\text{CAS}}$ latency (2,3)
- Programmable burst length (1,2,4,8,& Full page)
- Programmable wrap sequence (Sequential/Interleave)
- Automatic precharge and controlled precharge
- Auto refresh and self refresh modes
- Quad Internal banks controlled by A12 & A13 (Bank select)
- Each Bank can operate simultaneously and independently
- LVTTL compatible I/O interface
- Random column access in every cycle
- X8 organization
- Input/Output controlled by DQM
- 4,096 refresh cycles/64ms
- Burst termination by burst stop and precharge command
- Burst read/single write option

Pin Configuration

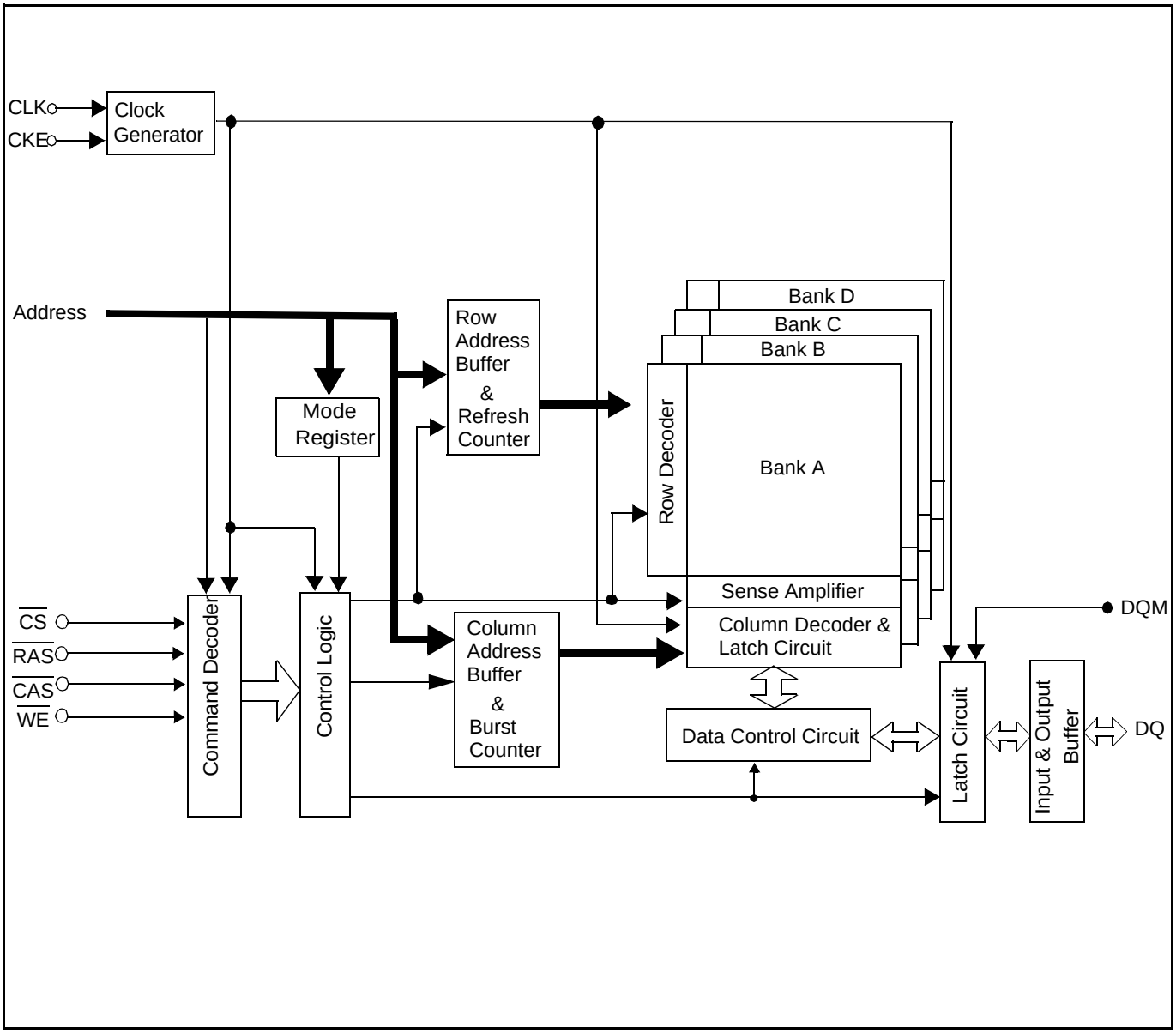
VG36648041



Pin Description
VG36648041

Pin Name	Function	Pin Name	Function
A0 - A11 A12,A13	Address inputs Bank select	DQM	DQ Mask enable
DQ0 ~ DQ7	Data - in/data - out	CLK	Clock input
$\overline{RAS}$	Row address strobe	CKE	Clock enable
$\overline{CAS}$	Column address strobe	$\overline{CS}$	Chip select
$\overline{WE}$	Write enable	V_{DDQ}	Supply voltage for DQ
V_{SS}	Ground	V_{SSQ}	Ground for DQ
V_{DD}	Power (+ 3.3V)		

Block Diagram



Absolute Maximum D.C. Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to + 4.6	V
Supply voltage relative to Vss	V_{DD}, V_{DDQ}	-0.5 to + 4.6	V
Short circuit output current	I_{OUT}	50	mA
Power dissipation	P_D	1.0	W
Operating temperature	T_{OPT}	0 to + 70	℃
Storage temperature	T_{STG}	-55 to + 125	℃

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause peumanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Maximum A.C. Operating Requirements for LVTTL Compatible

Parameter	Symbol	Min	Max	Unit	Notes
Input High Voltage	V_{IH}	2.0	V_{DDQ} + 2.0	V	2
Input Low Voltage	V_{IL}	V_{SSQ} -2.0	0.8	V	2

Recommended DC Operating Conditions for LVTTL Compatible

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{DD,}$ V_{DDQ}	3.0	3.3	3.6	V
Input High Voltage, all inputs	V_{IH}	2.0	-	V_{DD} + 0.3	V
Input Low Voltage, all inputs	V_{IL}	-0.3	-	0.8	V

Capacitance

(Ta = 25°C, f = 1MHZ)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input capacitance (All input pins except CLK pin)	C_{in}	2.5	3.75	5.0	pF	1
CLK pin	C_{CLK}	2.5	3.25	4.0	pF	1
Data input/output capacitance	$C_{I/O}$	4.0	5.25	6.5	pF	1

Notes : 1. Capacitance measured with effective capacitance measuring method.

2. The overshoot and undershoot voltage duration is ≤ 3ns with no input clamp diodes.

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test Conditions		VG36648041B				Unit	Notes
				-7		-8			
				Min	Max	Min	Max		
Operating current	I_{CC1}	Burst length = 1 One bank active $t_{RC} \geq t_{RC(MIN.)}$, Io = 0mA	CL = 3		130		130	mA	1
			CL = 2		130		130		
Precharge standby current in power down mode	I_{CC} 2P	CKE $\leq V_{IH(MAX.)}$ t_{CK} = 10ns			2		2	mA	
	I_{CC} 2PS	CKE $\leq V_{IH(MAX.)}$ $t_{CK} = \infty$			2		2		
Precharge standby current in Nonpower down mode	I_{CC} 2N	CKE $\geq V_{IH(MIN.)}$ t_{CK} = 10ns. CS $\geq V_{IH(MIN.)}$ Input signals are changed one time during 2 CLK cycles.			25		25	mA	
	I_{CC} 2NS	CKE $\geq V_{IH(MIN.)}$, tCK = ∞ CLK $\leq V_{IL(MAX.)}$ Input signals are stable.			10		10		
Active standby current in power down mode	I_{CC} 3P	CKE $\leq V_{IL(MAX.)}$, t_{CK} = 10ns			7		7	mA	
	I_{CC} 3PS	CKE $\leq V_{IL(MAX.)}$, $t_{CK} = \infty$			5		5		
Active standby current in Nonpower down mode	I_{CC} 3N	CKE $\geq V_{IH(MAX.)}$, t_{CK} = 10ns CS $\geq V_{IH(MIN.)}$ Input signals are changed one time during 2CLKs.			40		40	mA	
	I_{CC} 3NS	CKE $\geq V_{IH(MIN.)}$ $t_{CK} = \infty$ CLE $\leq V_{IL(MAX.)}$ Input signals are stable.			20		20		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK(MIN.)}$, Io = 0mA All banks Active	CL = 3		170		170	mA	2
			CL = 2		135		120		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC(MIN.)}$			220		200	mA	3
Self refresh current	I_{CC6}	CKE $\leq$ 0.2V			1		1	mA	
Input leakage current (Inputs)	I_{LI}	0 $\leq V_{IN} \leq V_{DD(MAX)}$ Pins not under test = 0V		-1	1	-1	1	µA	
Output leakage current (I/O pins)	I_{IL}	0 $\leq V_{OUT} \leq V_{DD\ (MAX)}$ DQ# in Hi - Z., Dout disabled		-1.5	1.5	-1.5	1.5	µA	
Output Low Voltage	V_{OL}	I_{OL} = 2mA			0.4		0.4	mA	4
Output High Voltage	V_{OH}	I_{OH} = -2mA		2.4		2.4		mA	4

Notes : 1. ICC1 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, ICC1 is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

2. ICC4 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, ICC4 is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

3. ICC5 is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

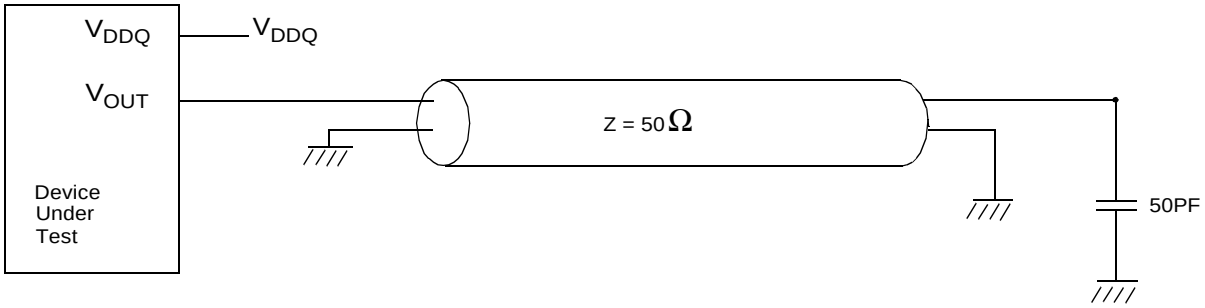
4. For LVTTL compatible, VG36648041.

A. C Characteristics : (Ta = 0 to 70°C V_{DD} = 3.3V ± 0.3V_{SS} = 0V)

Test Conditions for LVTTL Compatible :

AC input Levels (V_{IH}/V_{IL})	2.0/0.8V	Input timing reference level/ Output timing reference level	1.4V
Input rise and fall time	1ns	Output load condition	50pF

AC Test Load Circuits (for LVTTL interface) :

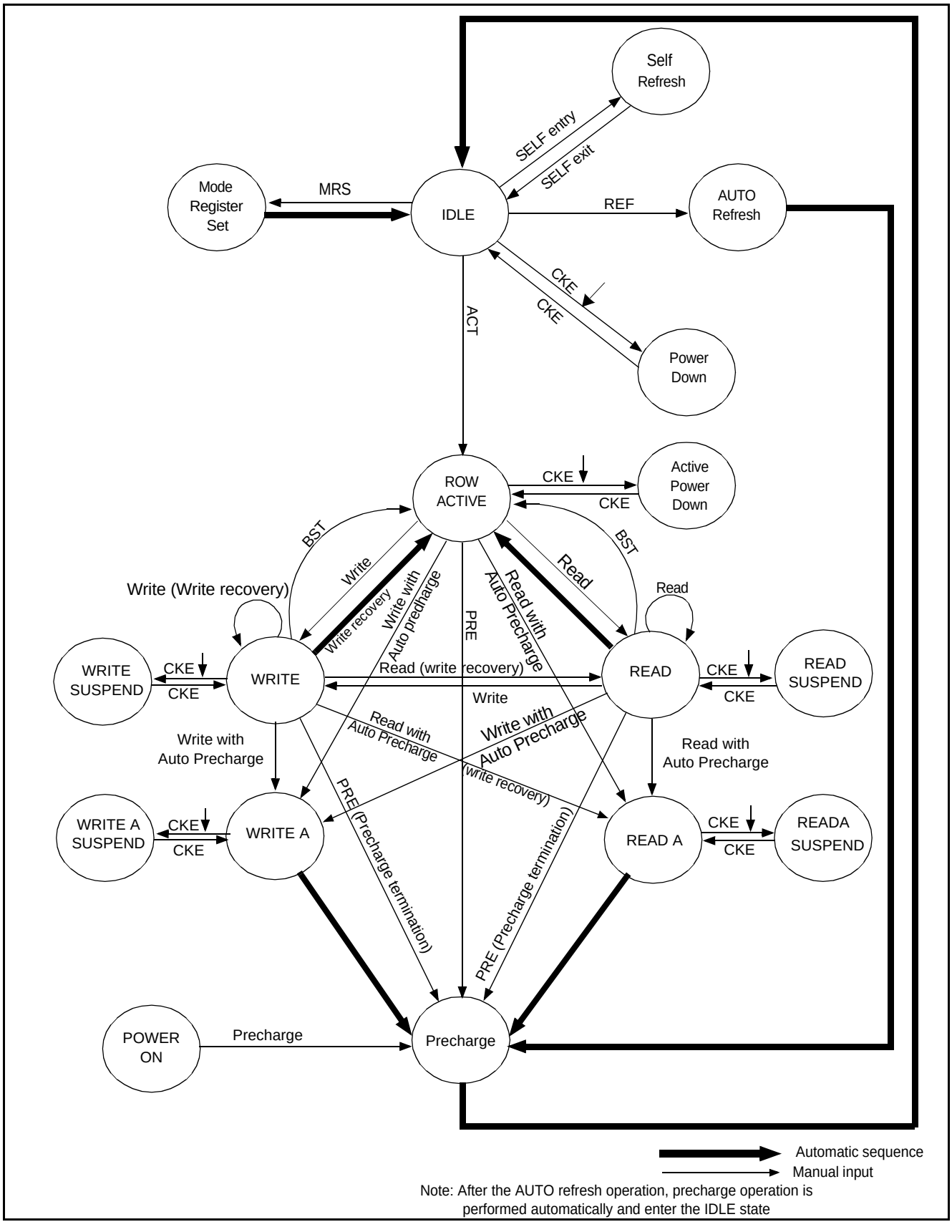


A. C Characteristics : (Ta = 0 to 70°C V_{DD} = 3.3V 0.3V, V_{SS} = 0V)

Parameter	CAS Latency	symbol	VG36648041B				Unit
			-7		-8		
			Min	Max	Min	Max	
CLK cycle time	3	t_{ck3}	7		8		ns
	2	t_{ck2}	10		10		ns
CLK to valid output delay	3	t_{Ac3}		6		6	ns
	2	t_{Ac2}		6		6	ns
CLK high pulse width		t_{CH}	3		3		ns
CLK low pulse width		t_{CL}	3		3		ns
CKE setup time		t_{CKS}	2		2		ns
CKE hold time		t_{CKH}	1		1		ns
Address setup time		t_{AS}	2		2		ns
Address hold time		t_{AH}	1		1		ns
Command setup time		t_{CMS}	2		2		ns
Command hold time		t_{CMH}	1		1		ns
Data input setup time		t_{DS}	2		2		ns
Data input hold time		t_{DH}	1		1		ns
Output data hold time		t_{OH}	3		3		ns
CLK to output in low - Z		t_{LZ}	0		0		ns
CLK to output in H - Z	3	t_{HZ}		5		6	ns
	2			6		6	
Row active to active delay		t_{RRD}	14		16		ns
RAS to CAS delay		t_{RCD}	20		20		ns
Row precharge time		t_{RP}	20		20		ns
ROW active time		t_{RAS}	40	120K	48	120K	ns
ROW cycle time		t_{RC}	60		68		ns
Last data in to burst stop		t_{BDL}	1		1		CLK
Data - in to ACT(REF) command		t_{DAL}	1+ t_{RP}		1+t_{RP}		CLK
Data - in to precharge		t_{DPL}	1		1		CLK
Transition time		t_T	1	10	1	10	ns
Mode reg. set cycle		t_{RSC}	2		2		CLK
Power down exit setup time		t_{PDE}	2		2		ns
Self refresh exit time		t_{SRX}	1		1		CLK
Refresh time		t_{REF}		64		64	ms

Basic Features and Function Description

1.Simplified State Diagram



Note: After the AUTO refresh operation, precharge operation is performed automatically and enter the IDLE state

2.Truth Table

2.1 Command Truth Table

FUNCTION	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10	A11 A9 - A0
		n - 1	n							
Device deselect	DESL	H	X	H	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	L	L	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V
Read	READ	H	X	L	H	L	H	V	L	V
Read with auto precharge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	X	L	H	L	L	V	H	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Burst stop	BST	H	X	L	H	H	L	X	X	X
CBR (Auto) refresh	REF	H	H	L	L	L	H	X	X	X
Self refresh	SELF	H	L	L	L	L	H	X	X	X

2.2 DQM Truth Table

FUNCTION	Symbol	CKE		DQM
		n - 1	n - 1	
Data write/output enable	ENB	H	X	L
Data mask/output disable	MASK	H	X	H

2.3 CKE Truth Table

Current State	Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add - ress
			n - 1	n					
Activating	Clock suspend mode entry		H	L	X	X	X	X	X
Any	Clock suspend		L	L	X	X	X	X	X
Clock suspend	Clock suspend mode exit		L	H	X	X	X	X	X
Idle	CBR refresh command	REF	H	H	L	L	L	H	X
Idle	Self refresh entry	SELF	H	L	L	L	L	H	X
Self refresh	Self refresh exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Idle	Power down entry		H	L	X	X	X	X	X
Power down	Power down exit		L	H	X	X	X	X	X

H : High level, L : Low level

X : High or Low level (Dont care), V : Valid Data input

2.4 Operative Command Table Notes 1 (1/3)

HCurrent state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Idle	H	X	X	X	X	DESL	Nop or Power down	2
	L	H	H	X	X	NOP or BST	Nop or Power down	2
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BR, RA	ACT	Row active	
	L	L	H	L	BA, A10	PRE/PALL	Nop	
	L	L	L	H	X	REF/SELF	Refresh or Self refresh	4
	L	L	L	L	Op-Code	MPS	Mode register access	
Row active	H	X	X	X	X	DESL	Nop	
	L	H	H	X	X	NOP or BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read : Determine AP	5
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin write : Determine AP	5
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Precharge	6
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Read	H	X	X	X	X	DESL	Continue burst to end → Row active	
	L	H	H	H	X	NOP	Continue burst to end → Row active	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Term burst, new read : Determine AP	7
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Term burst, start write : Determine AP	7,8
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Term burst, precharging	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write	H	X	X	X	X	DESL	Continue burst to end → write recovering	
	L	H	H	H	X	NOP	Continue burst to end → write recovering	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Term burst, start read : Determine AP	7,8
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Term burst, new write : Determine AP	7
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Term burst, precharging	9
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

(2/3)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CA}$	$\overline{WE}$	Address	Command	Action	Notes
Read with auto precharge	H	X	X	X	X	DESL	Continue burst to end → Precharging	
	L	H	H	H	X	NOP	Continue burst to end → Precharging	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	11
	L	L	H	H	BA, RA	ACT	ILLEGAL	3,11
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3,11
	L	L	L	H	X	PEF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
Write with auto precharge	H	X	X	X	X	DESL	Continue burst to end → write recovering with auto precharte	
	L	H	H	H	X	NOP	Continue burst to end → write recovering with auto precharge	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	11
	L	L	H	H	BA, RA	ACT	ILLEGAL	3,11
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3,11
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - code	MRS	ILLEGAL	
Precharging	H	X	X	X	X	DESL	Nop → Enter idle after t_{RP}	
	L	H	H	H	X	NOP	Nop → Enter idle after t_{RP}	
	L	H	H	L	X	BST	Nop → Enter idle after t_{RP}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after t_{RP}	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
Row activating	H	X	X	X	X	DESL	Nop → Enter row active after t_{RCD}	
	L	H	H	H	X	NOP	Nop → Enter row active after t_{RCD}	
	L	H	H	L	X	BST	Nop → Enter row active after t_{RCD}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3,9
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	

(3/3)

Current	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Write recovering	H	X	X	X	X	DESL	Nop → Enter row active after t_{DPL}	
	L	H	H	H	X	NOP	Nop → Enter row active after t_{DPL}	
	L	H	H	L	X	BST	Nop → Enter row active after t_{DPL}	
	L	H	L	H	BA, CA, A10	READ/READA	Start read, Determine AP	8
	L	H	L	L	BA, CA, A10	WRIT/WRITA	New write, Determine AP	
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	PEF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
Write recovering with auto precharge	H	X	X	X	X	DESL	Nop → Enter precharge after t_{DPL}	
	L	H	H	H	X	NOP	Nop → Enter precharge after t_{DPL}	
	L	H	H	L	X	BST	Nop → Enter precharge after t_{DPL}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3,8,11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3,11
	L	L	H	H	BA, RA	ACT	ILLEGAL	3,11
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
Auto Refreshing	H	X	X	X	X	DESL	Nop Enter idle after t_{RC}	
	L	H	H	X	X	NOP/BST	Nop Enter idle after t_{RC}	
	L	H	L	X	X	READ/WRIT	ILLEGAL	
	L	L	H	X	X	ACT/PRE/PALL	ILLEGAL	
	L	L	L	X	X	REF/SELF/MRS	ILLEGAL	
Mode register setting	H	X	X	X	X	DESL	Nop → Enter idle after 2 Clocks	
	L	H	H	H	X	NOP	Nop → Enter idle after 2 Clocks	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	X	X	READ/WRITE	ILLEGAL	
	L	L	X	X	X	ACT/PRE/PALL/ REF/SELF/MRS	ILLEGAL	

Note: 1. All entries assume that CKE was active (High level) during the preceding clock cycle.
2. If both banks are idle, and CKE is inactive (Low level), the device will enter Power downmode. All input buffers except CKE will be disabled.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by BankAddress(BA), depending on the state of that bank.
4. If both banks are idle, and CKE is inactive (Low level), the device will enter Self refresh mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RCD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
9. Must mask preceding data which dont satisfy t_{DPL}.
10. Illegal if t_{RRD} is not satisfied.
11. Illegal for single bank, but legal for other banks in multi-bank devices.

2.5 Command Truth Table for CKE Note 1

Current state	CKE n - 1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Notes
Self refresh (S.R.)	H	X	X	X	X	X	X	INVALID, CLK (n - 1)would exit S.R.	
	L	H	H	X	X	X	X	S.R. Recovery	2
	L	H	L	H	H	X	X	S.R. Recovery	2
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	Maintain S.R.	
Self refresh recovery	H	H	H	X	X	X	X	Idle after t_{RC}	
	H	H	L	H	H	X	X	Idle after t_{RC}	
	H	H	L	H	L	X	X	ILLEGAL	
	H	H	L	L	X	X	X	ILLEGAL	
	H	L	H	X	X	X	X	Begin clock suspend next cycle	5
	H	L	L	H	H	X	X	Begin clock suspend next cycle	5
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	H	X	X	X	X	X	Exit clock suspend next cycle	2
	L	L	X	X	X	X	X	Maintain clock suspend	
Power down (P.D.)	H	X	X	X	X	X		INVALID, CLK (n - 1) would exit P.D.	
	L	H	X	X	X	X	X	EXIT P.D. → Idle	2
	L	L	X	X	X	X	X	Maintain power down mode	
Both banks idle	H	H	H	X	X	X		Refer to operations in Operative Command Table	
	H	H	L	H	X	X		Refer to operations in Operative Command Table	
	H	H	L	L	H	X		Refer to operation in Operative Command Table	
	H	H	L	L	L	H	X	Auto Refresh	
	H	H	L	L	L	L	Op - Code	Refer to operations in Operative Command Table	
	H	L	H	X	X	X		Refer to operations in Operative Command Table	
	H	L	L	H	X	X		Refer to operations in Operative Command Table	
	H	L	L	L	H	X		Refer to operations in Operative Command Table	
	H	L	L	L	L	H	X	Self refresh	3
	H	L	L	L	L	L	Op - Code	Refer to operations in Operative Command Table	
	L	X	X	X	X	X	X	Power down	3
Any state other than listed above	H	H	X	X	X	X	X	Refer to operations in Operative Command Table	
	H	L	X	X	X	X	X	Begin clock suspend next cycle	4
	L	H	X	X	X	X	X	Exit clock suspend next cycle	
	L	L	X	X	X	X	X	Maintain clock suspend	

Note: 1. H : Hight level, L : low level, X : High or low level (Don't care).
2. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
3. Power down and Self refresh can be entered only from the both banks idle state.
4. Must be legal command as defined in Operative Command Table.
5. Illegal if t_{SREX} is not satisfied.

5.Mode Register (Address Input for Mode Set)

13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	1	Reserved							JEDEC Standard Test Set
x	x	x	x	1	0	0	LTMODE			WT	BL			Burst Read and Single Write (for Write Through Cache)
x	x	x	x	0	0	0	LTMODE			WT	BL			Burst Read and Burst Write

X = Dont care

Burst length	Bits2 - 0	WT = 0	WT = 1
	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Full page	R

Wrap type	0	Sequential
	1	Interleave

Latency mode	Bits6 - 4	$\overline{\text{CAS}}$ latency
	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

Remark R : Reserved

5.1 Burst Length and Sequence

(Burst of Two)

Starting Address (column address A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

(Burst of Four)

Starting Address (column address A1 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

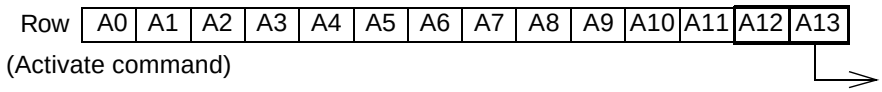
(Burst of Eight)

Starting Address (column address A2 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence(decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1 ,2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6 ,7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7 ,0 ,1 ,2 ,3 ,4 ,5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

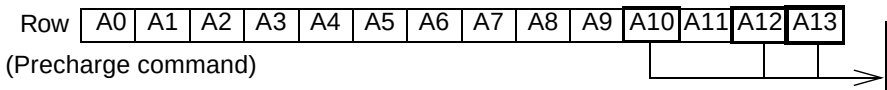
Full page burst is an extension of the above tables of Sequential Addressing, with the length being 512 for 8M x 8 devices.

6.Address Bits of Bank-Select and Precharge

6.1 Quad banks controlled by A12 & A13 (for VG36648041/VG36648042)



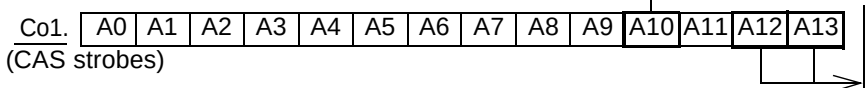
A12	A13	Result
0	0	Select Bank A “Activate “ command
0	1	Select Bank B “Activate” command
1	0	Select Bank C “Activate” command
1	1	Select Bank D “Activate” command



A10	A12	A13	Result
0	0	0	Precharge Bank A
0	0	1	Precharge Bank B
0	1	0	Precharge Bank C
0	1	1	Precharge Bank D
1	X	X	Precharge All Banks

X: Don't care

0	Disables Auto - Precharge (End of Burst)
1	Enables Auto - Precharge (End of Burst)



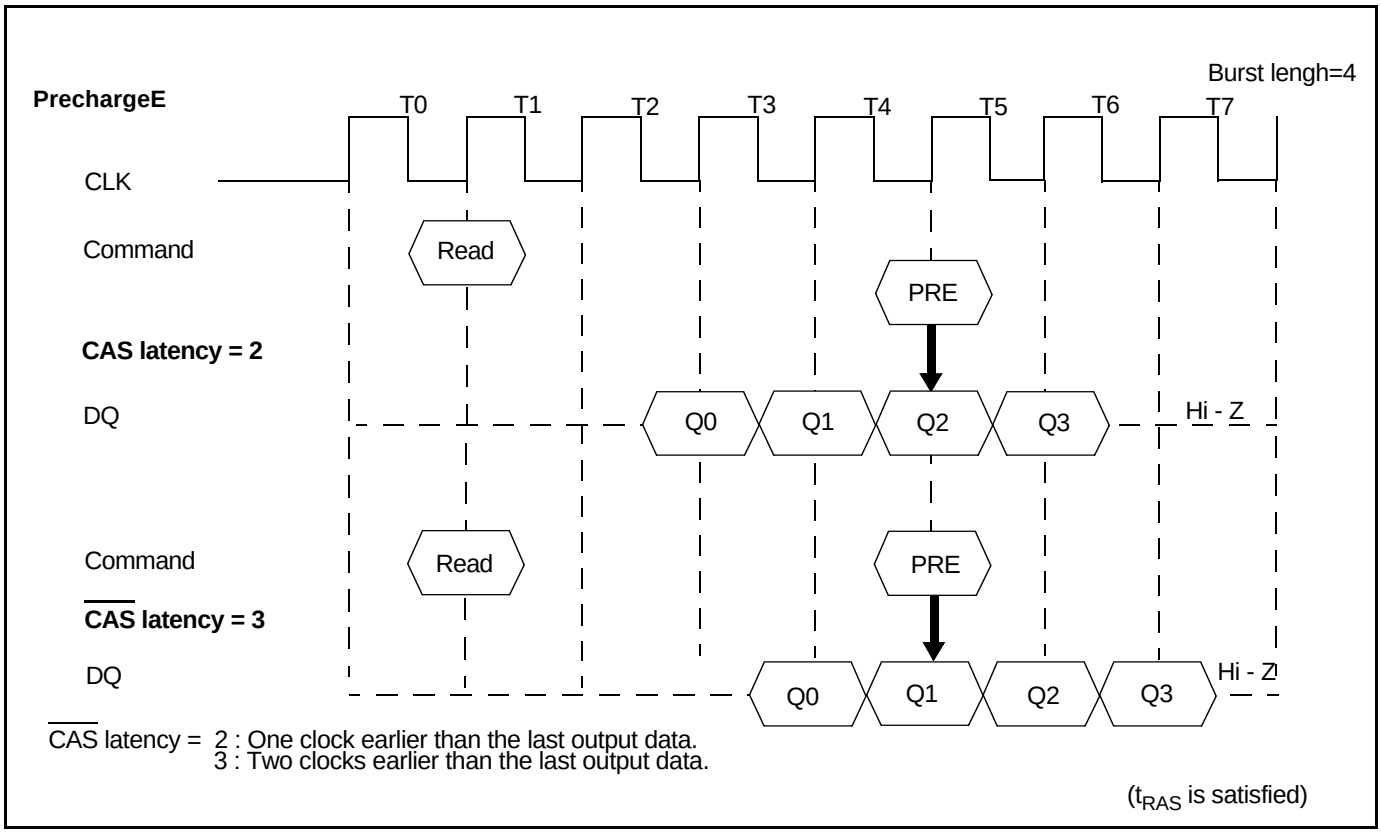
A12	A13	Result
0	0	Enables Read/Write commands for Bank A
0	1	Enables Read/Write commands for Bank B
1	0	Enables Read/Write commands for Bank C
1	1	Enables Read/Write commands for Bank D

7.Precharge

The precharge command can be asserted anytime after $t_{RAS(min)}$ is satisfied.

Soon after the precharge command is asserted, the precharge operation is performed and the synchronous DRAM enters the idle state after $t_{RP(min.)}$ is satisfied. The parameter t_{RP} is the time required to perform the precharge.

The earliest timing in a read cycle that a precharge command can be asserted without losing any data in the burst is as follows.



In order to write all data to the memory cell correctly, the asynchronous parameter "t_{DPL}" must be satisfied. The $t_{DPL(min.)}$ specification defines the earliest time that a precharge command can be asserted. The minimum number of clocks can be calculated by dividing $t_{DPL(min.)}$ by the clock cycle time.

In summary, the precharge command can be asserted relative to the reference clock that indicates the last data word is valid. In the following table, minus means clocks before the reference; plus means time after the reference.

$\overline{\text{CAS}}$ latency	Read	Write
2	-1	+ $t_{DPL(min.)}$
3	-2	+ $t_{DPL(min.)}$

8.Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. If A10 is high in the read or write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and begins automatically after the burst access.

In the write cycle, $t_{DAL(min.)}$ must be satisfied before asserting the next activate command to the bank being precharged.

When using auto precharge in the read cycle, knowing when the precharge starts is important because the next activate command to the bank being precharged cannot be executed until the precharge cycle ends. Once auto precharge has started, an activate command to the bank can be asserted after t_{RP} has been satisfied.

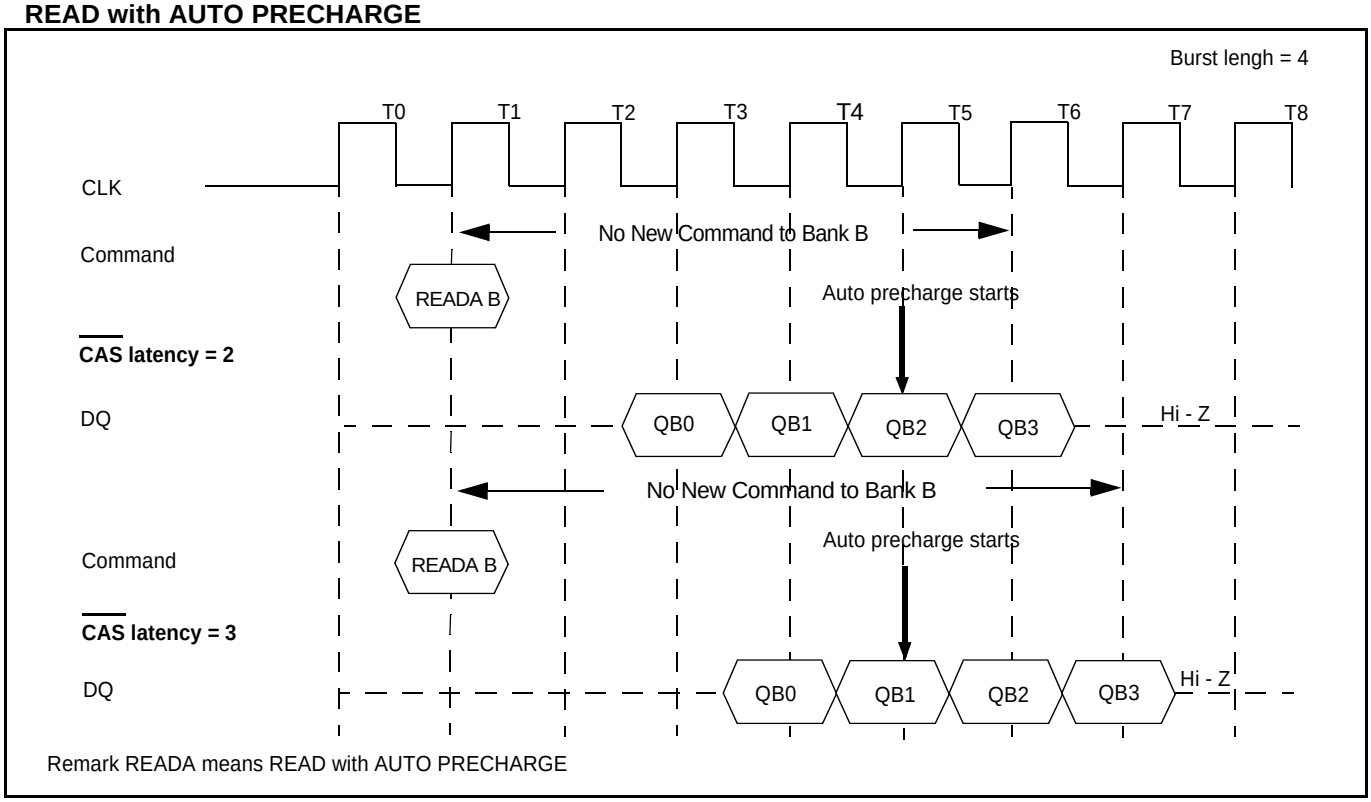
A Read or Write command without auto - precharge can be terminated in the midst of a burst operation. However, a Read or Write command with auto - precharge can not be interrupted by the same bank commands before the entire burst operation is completed. Therefore use of the same bank Read, Write, Precharge or Burst Stop command is prohibited during a read or write cycle with auto - precharge. It should be noted that the device will not respond to the Auto - Precharge command if the device is programmed for full page burst read or write cycles.

The timing when the auto precharge cycle begins depends both on both the $\overline{CAS}$ latency programmed into the mode register and whether the cycle is read or write.

8.1 Read with Auto Precharge

During a READA cycle, the auto precharge begins one clock earlier (CL = 2) or two clocks earlier (CL = 3) than the last word output.

READ with AUTO PRECHARGE

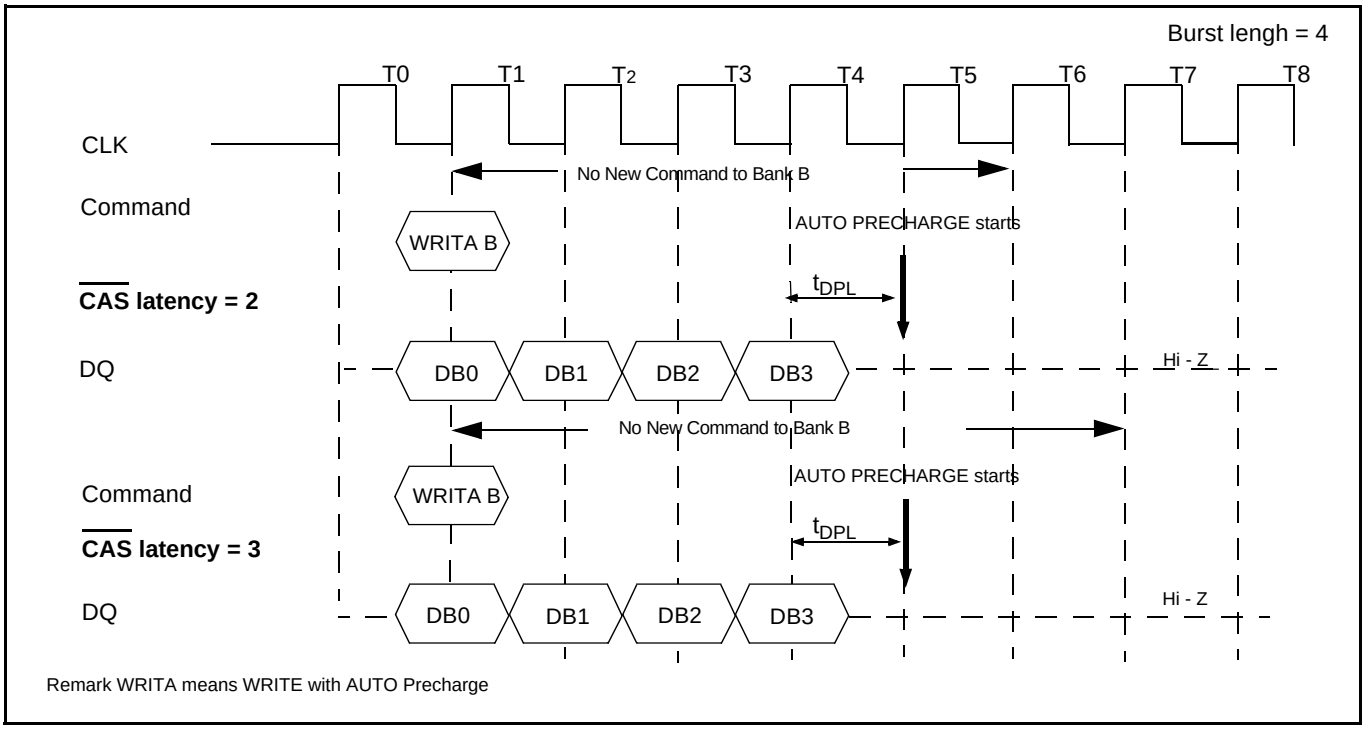


Remark READA means READ with AUTO PRECHARGE

8.2 Write with Auto Precharge

During a write cycle, the auto precharge starts at the timing that is equal to the value of $t_{DPL(min.)}$ after the last data word input to the device.

WRITE with AUTO PRECHRGE



In summary, the auto precharge cycle begins relative to a reference clock that indicates the last data word is valid.

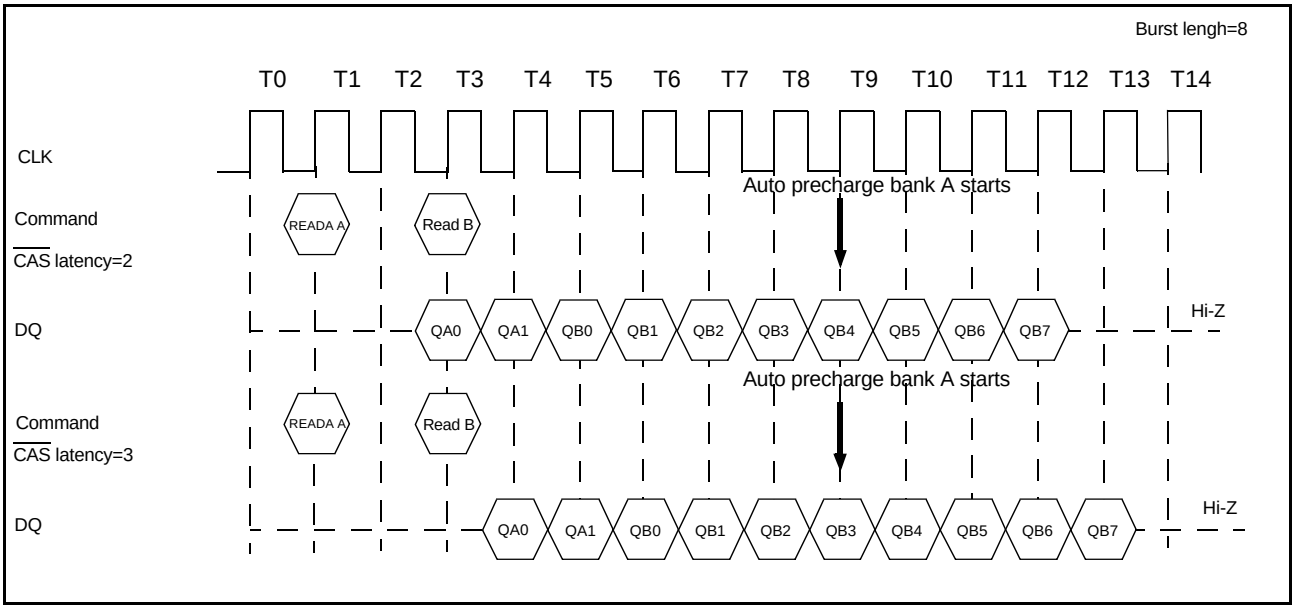
In the table below, minus means clocks before the reference; plus means clocks after the reference.

$\overline{CAS}$ latency	Read	Write
2	-1	+ $t_{DPL(min.)}$
3	-2	+ $t_{DPL(min.)}$

8.3 Multibank Operation- Read with Auto Precharge

During a READA cycle interrupted by a Read, Write command of another banks, the auto-precharge scheduled time would not be changed.

Multibank Operation

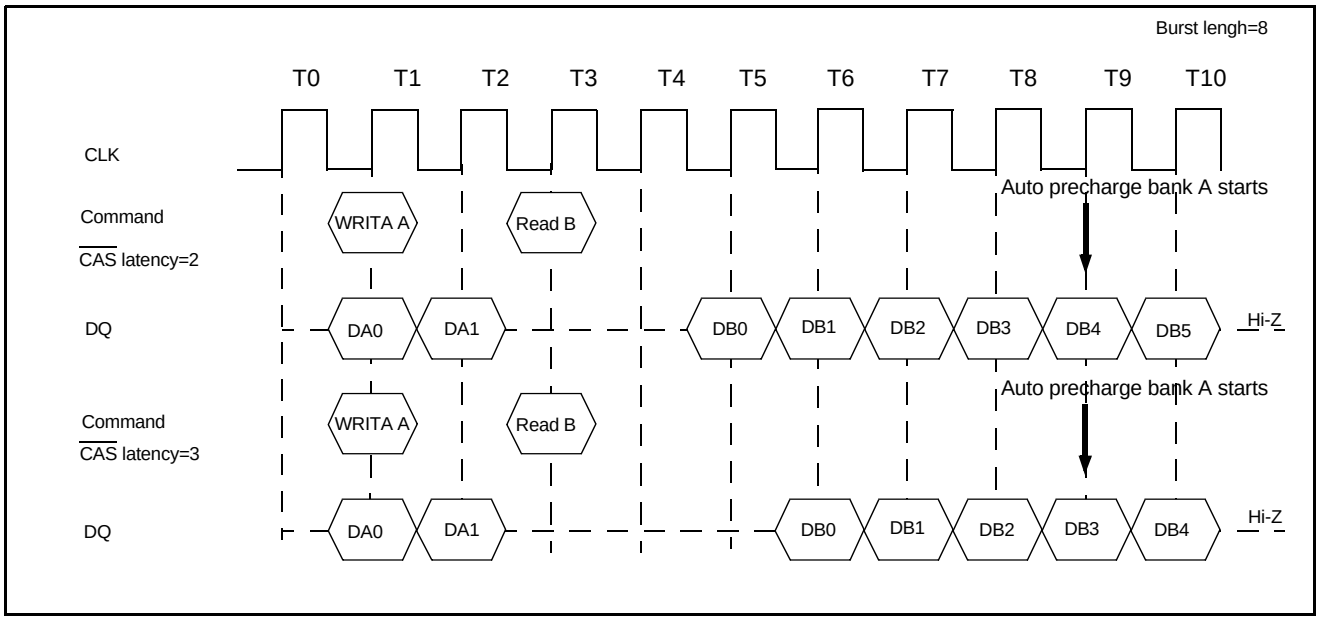


Similiar top.21

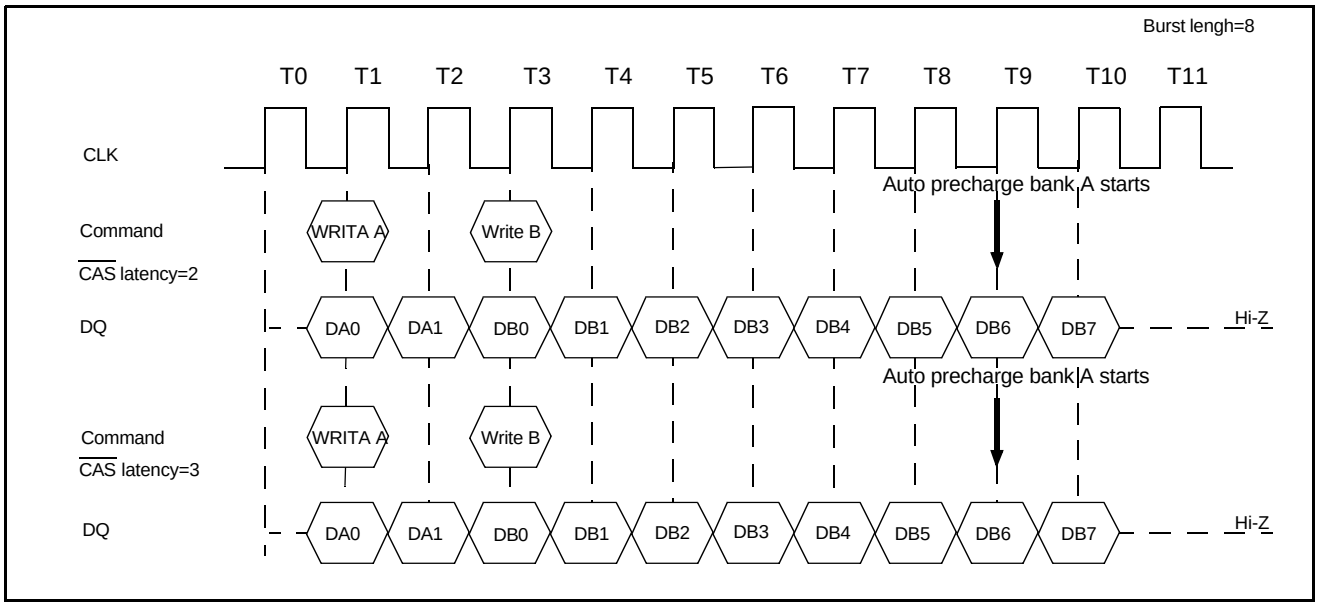
8.4 Multibank Operation- Write with Auto Precharge

During a WRITEA cycle interrupted by a Read, Write command of another banks, the auto-precharge scheduled time would not be changed.

Multibank Operation



Multibank Operation



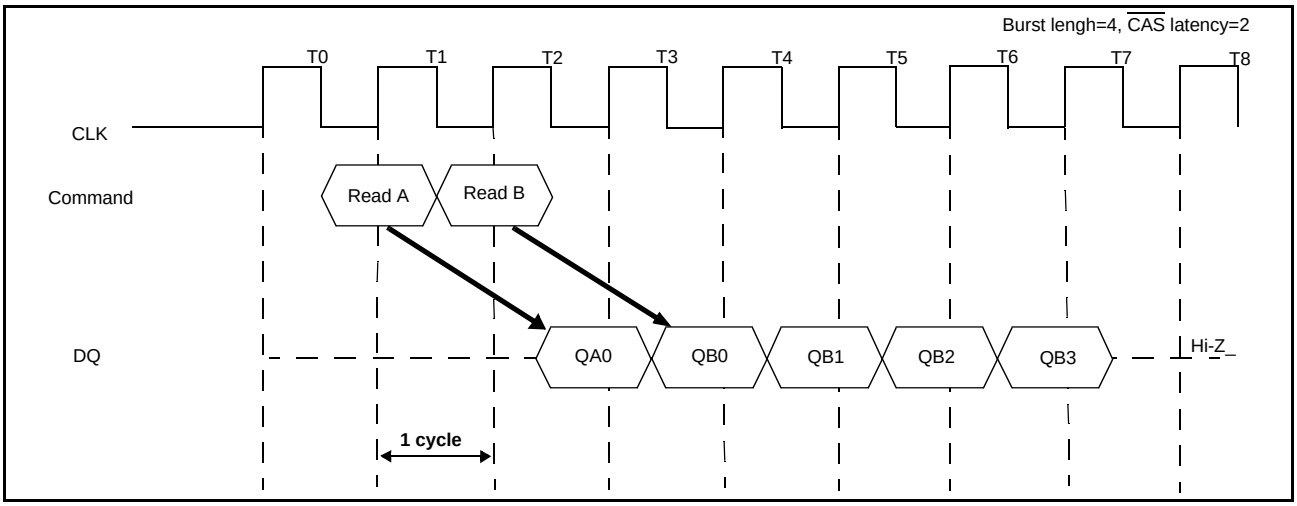
9.Read/Write Command Interval

9.1 Read to Read command interval

During a read cycle when a new read command is asserted, it will be effective after the $\overline{CAS}$ latency, even if the previous read operation has not completed. READ will be interrupted by another READ.

Each read command can be asserted in every clock without any restriction.

READ to READ Command Interval

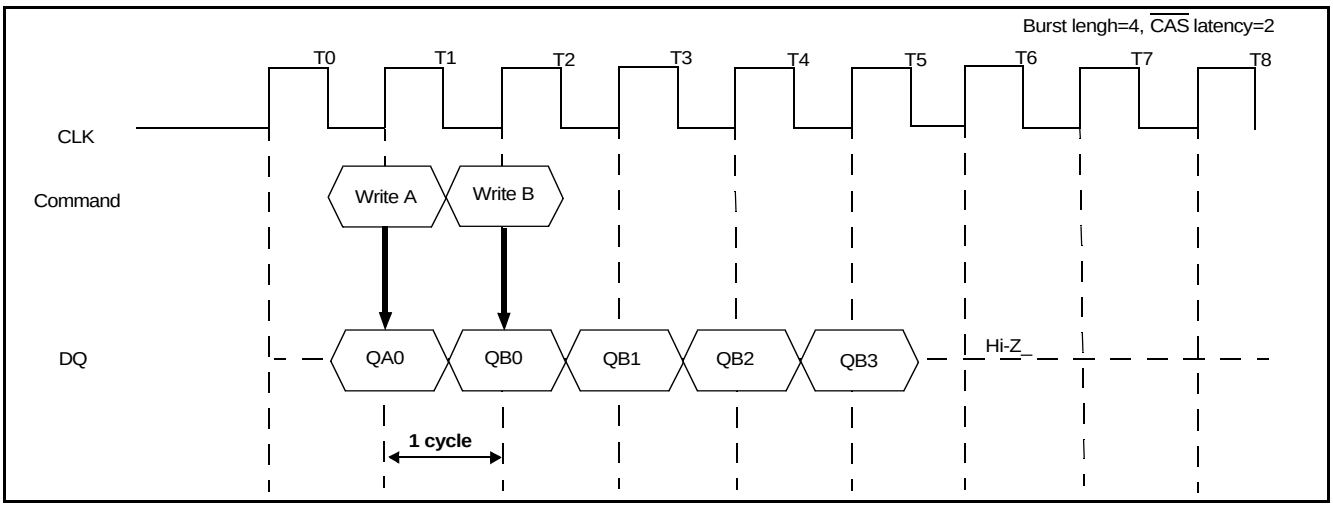


9.2 Write to Write Command Interval

During a write cycle, when a new Write command is asserted, the previous burst will terminated and the new burst will begin with a new write command. WRITE will be interrupted by another WRITE.

Each write command can be asserted in every clock without any restriction.

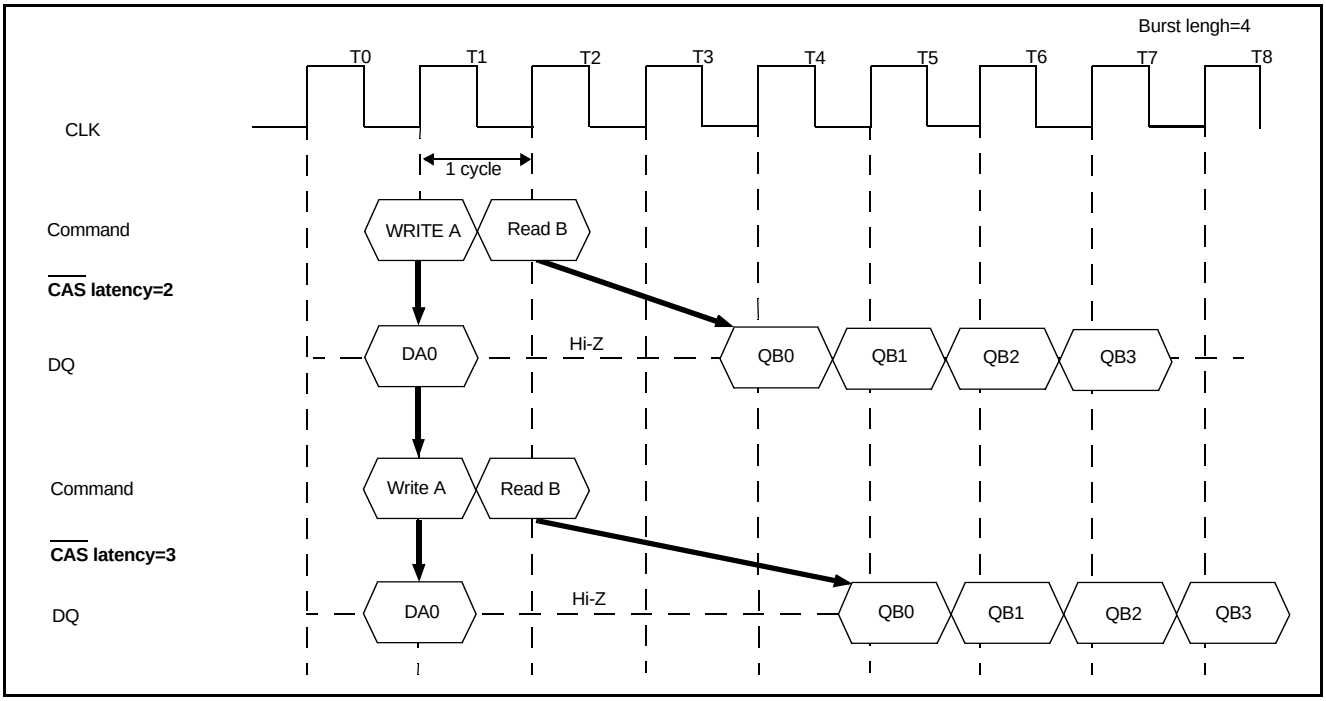
WRITE to WRITE Command Interval



9.3 Write to Read Command Interval

The write command to read command interval is also a minimum of 1 cycle. Only the write data before the read command will be written. The data bus must be Hi-Z at least one cycle prior to the first D_{OUT}.

WRITE to READ Command Interval

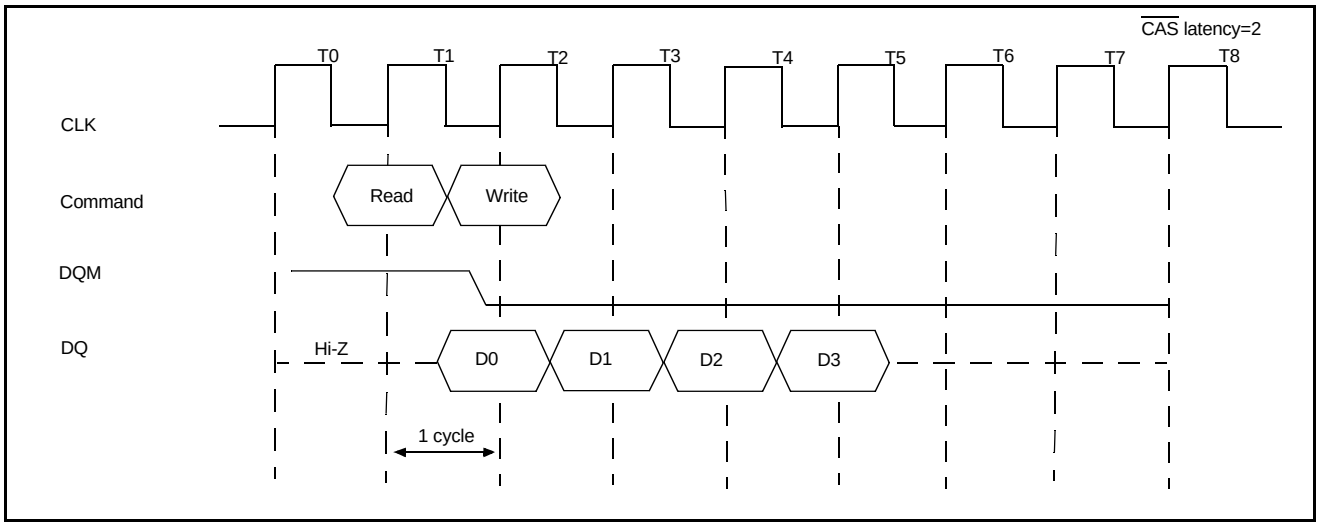


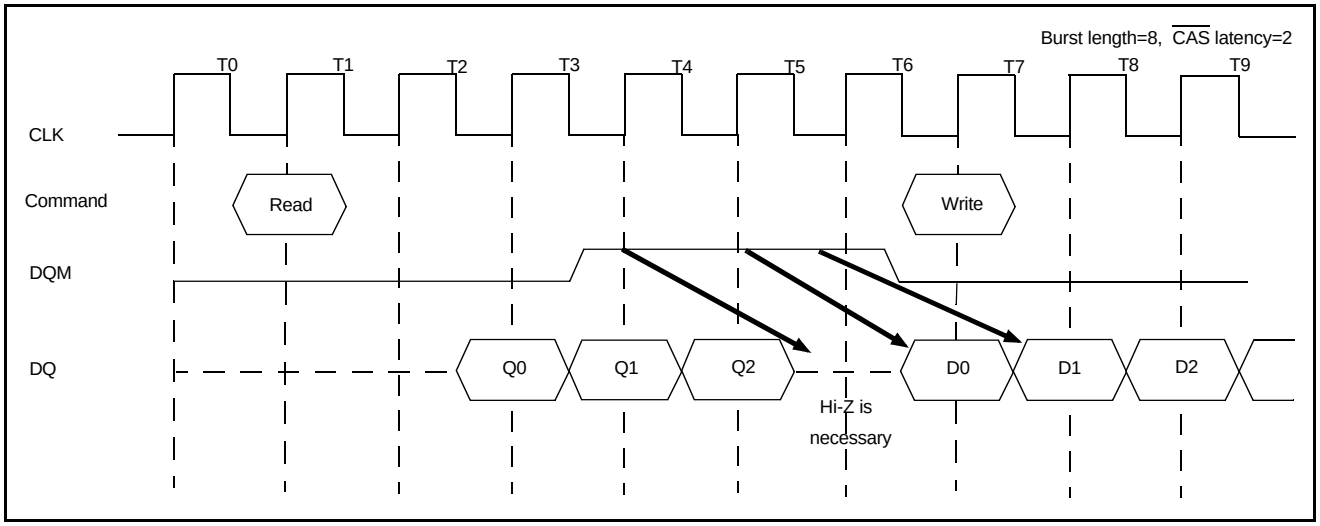
9.4 Read to Write Command Interval

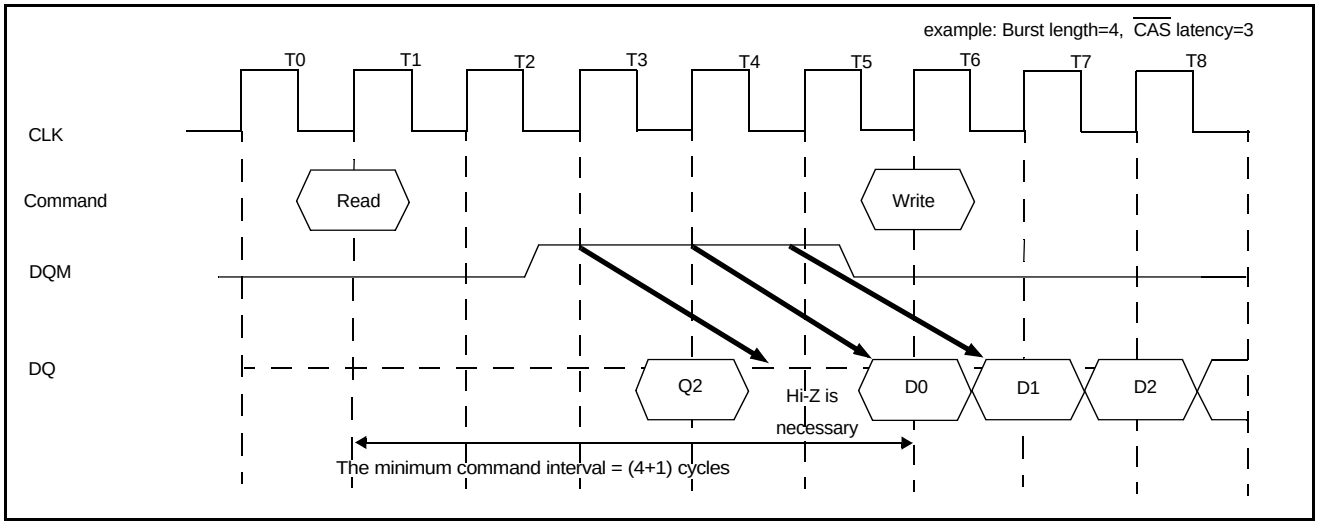
During a read cycle, READ can be interrupted by WRITE.

DQM must be in High at least 3 clocks prior to the write command. There is a restriction to avoid a data conflict. The data bus must be Hi-Z using DQM before Write.

READ to WRITE Command Interval







10.BURST Termination

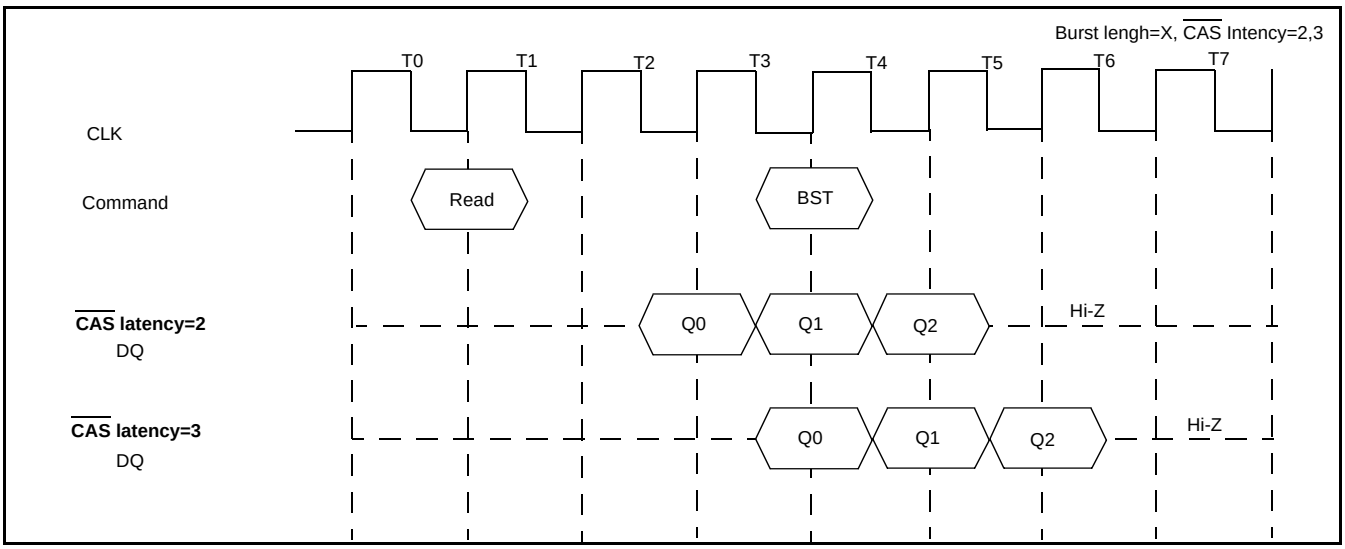
There are two methods to terminate a burst operation other than using a read or a write command. One is the burst stop command and the other is the precharge command.

10.1 BURST Stop Command

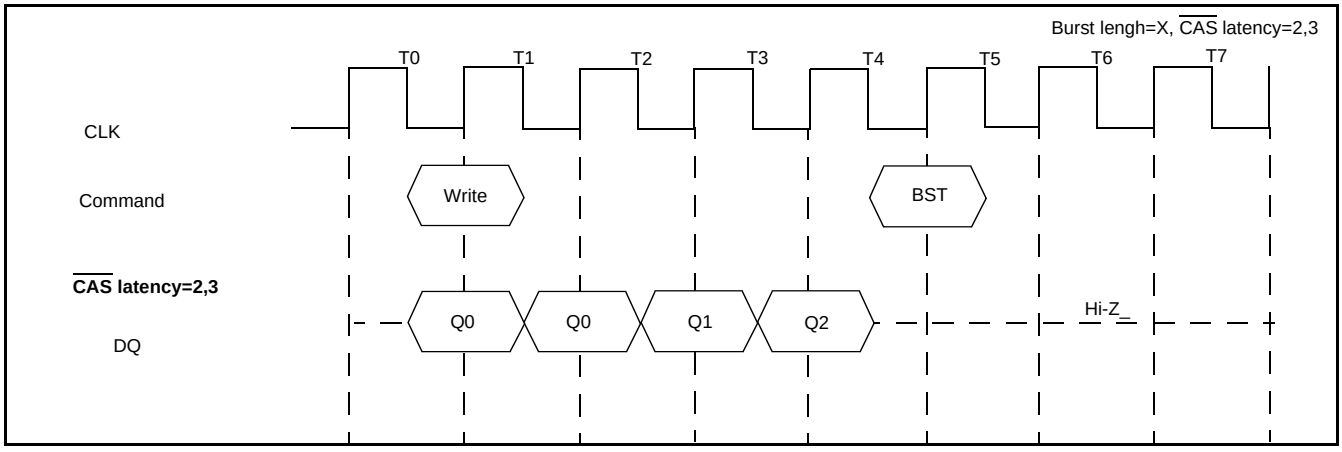
During a read burst. when the burst stop command is asserted, the burst read data are terminated and the data bus goes to high-impedance after the $\overline{\text{CAS}}$ latency from the burst stop command.

During a write burst, when the burst stop command is asserted, any data provided at that cycle will not be written. The burst write is effectively terminated and no further data can be written until a new write command is asserted.

Burst Termination



Remark BST: Burst stop command



Remark BST: Burst command

10.2 PRECHARGE TERMINATION

10.2.1 PRECHARGE TERMINATION in READ Cycle

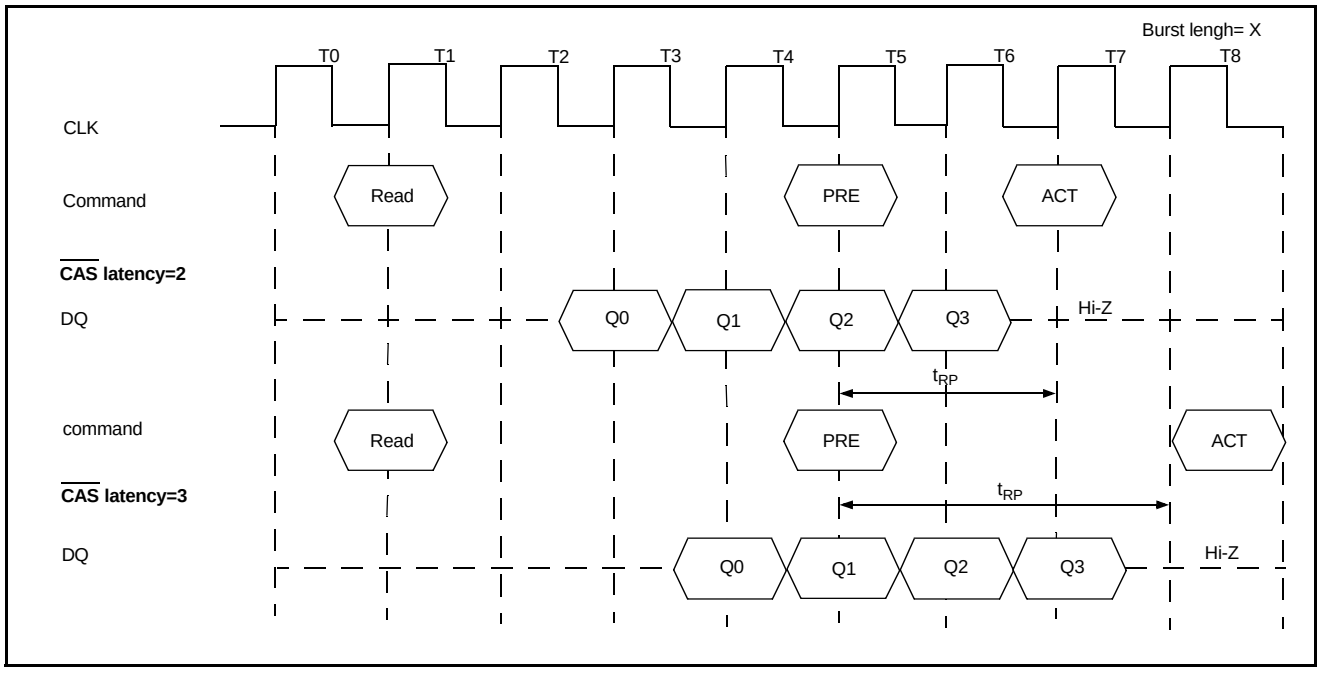
During READ cycle, the burst read operation is terminated by a precharge command. When the precharge command is asserted, the burst read operation is terminated and precharge starts.

The same bank can be activated again after t_{RP} from the precharge command.

When CAS latency is 2,the read data will remain valid until one clock after the precharge command.

When CAS latency is 3, the read data will remain valid until two clocks after the precharge command.

Precharge Termination in READ Cycle



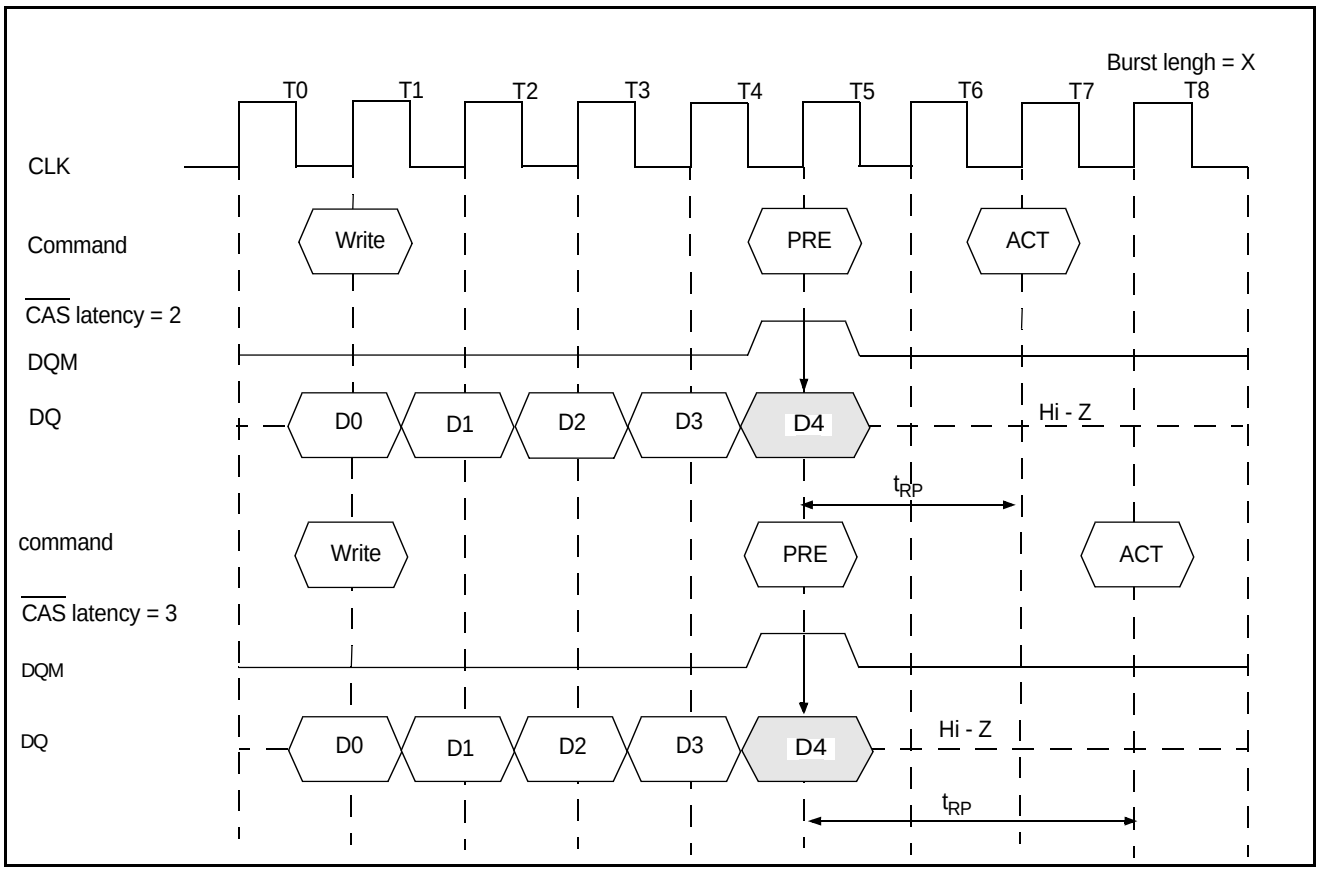
10.2.2 Precharge Termination in WRITE Cycle

During WRITE cycle, the burst write operation is terminated by a precharge command. When the precharge command is asserted, the burst write operation is terminated and precharge starts.

The same bank can be activated again after t_{RP} from the precharge command. The DQM must be high to mask invalid data in.

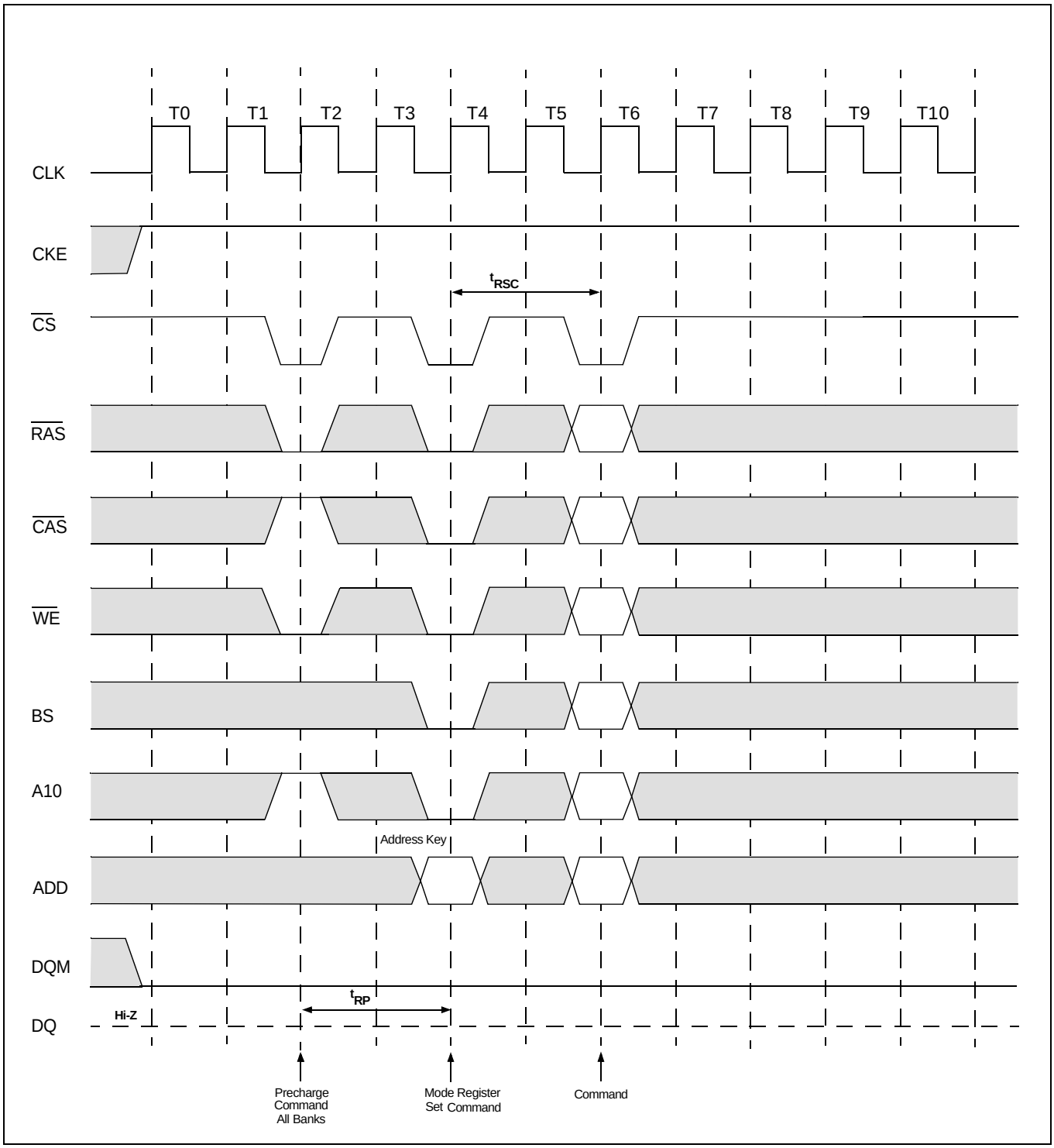
During WRITE cycle, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.

PRECHARGE TERMINATION in WRITE Cycle

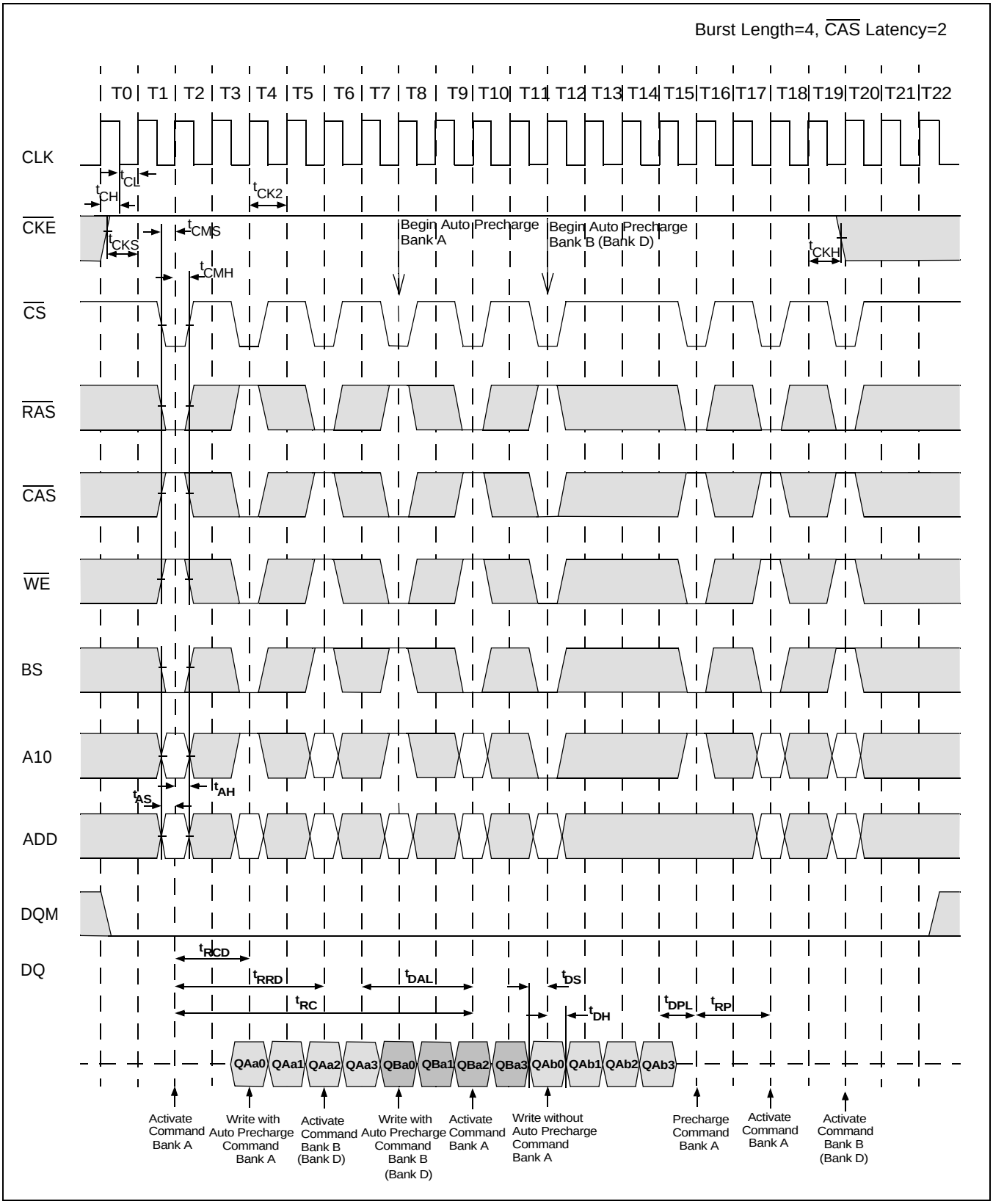


Timing Diagram

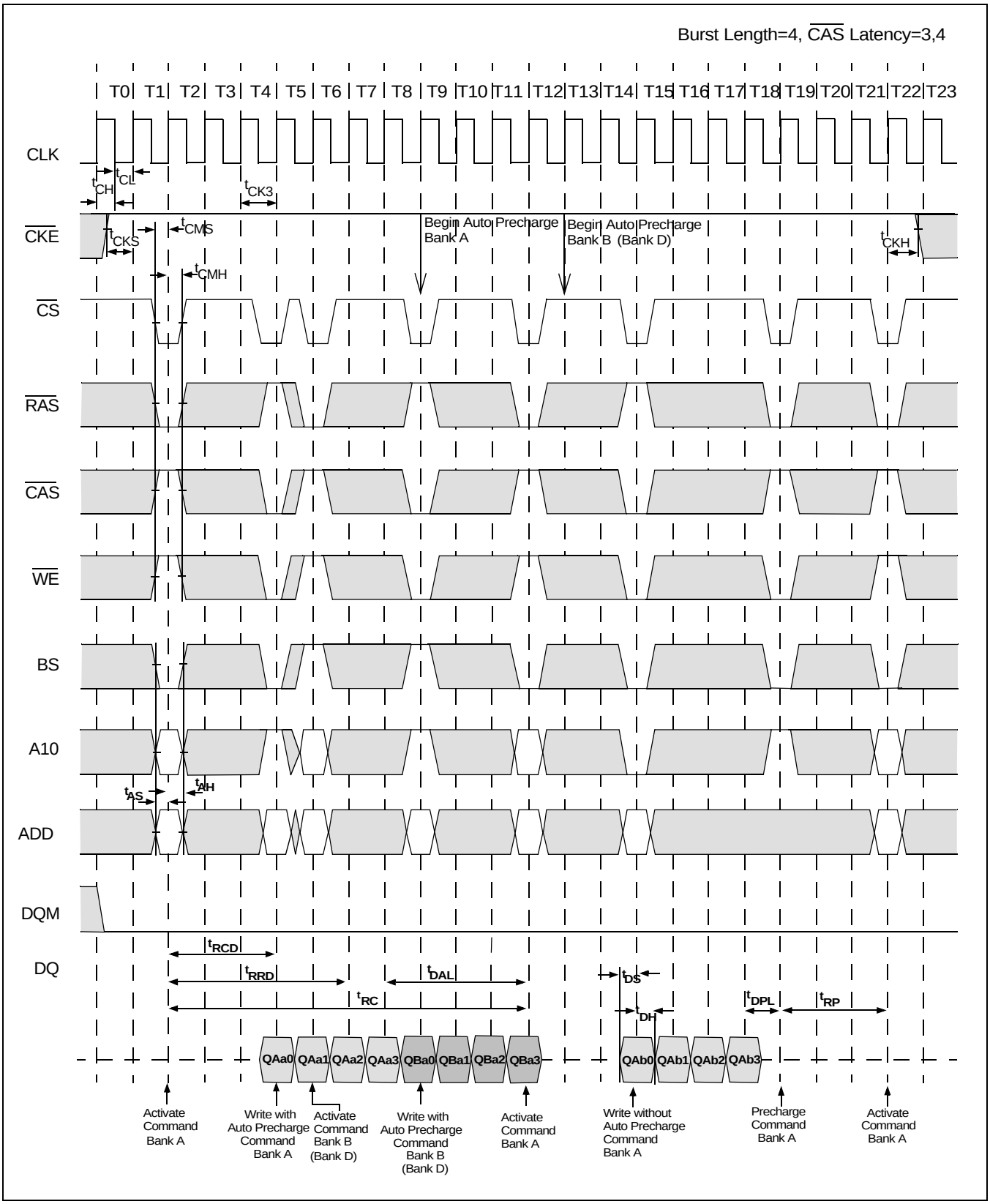
Mode Register Set



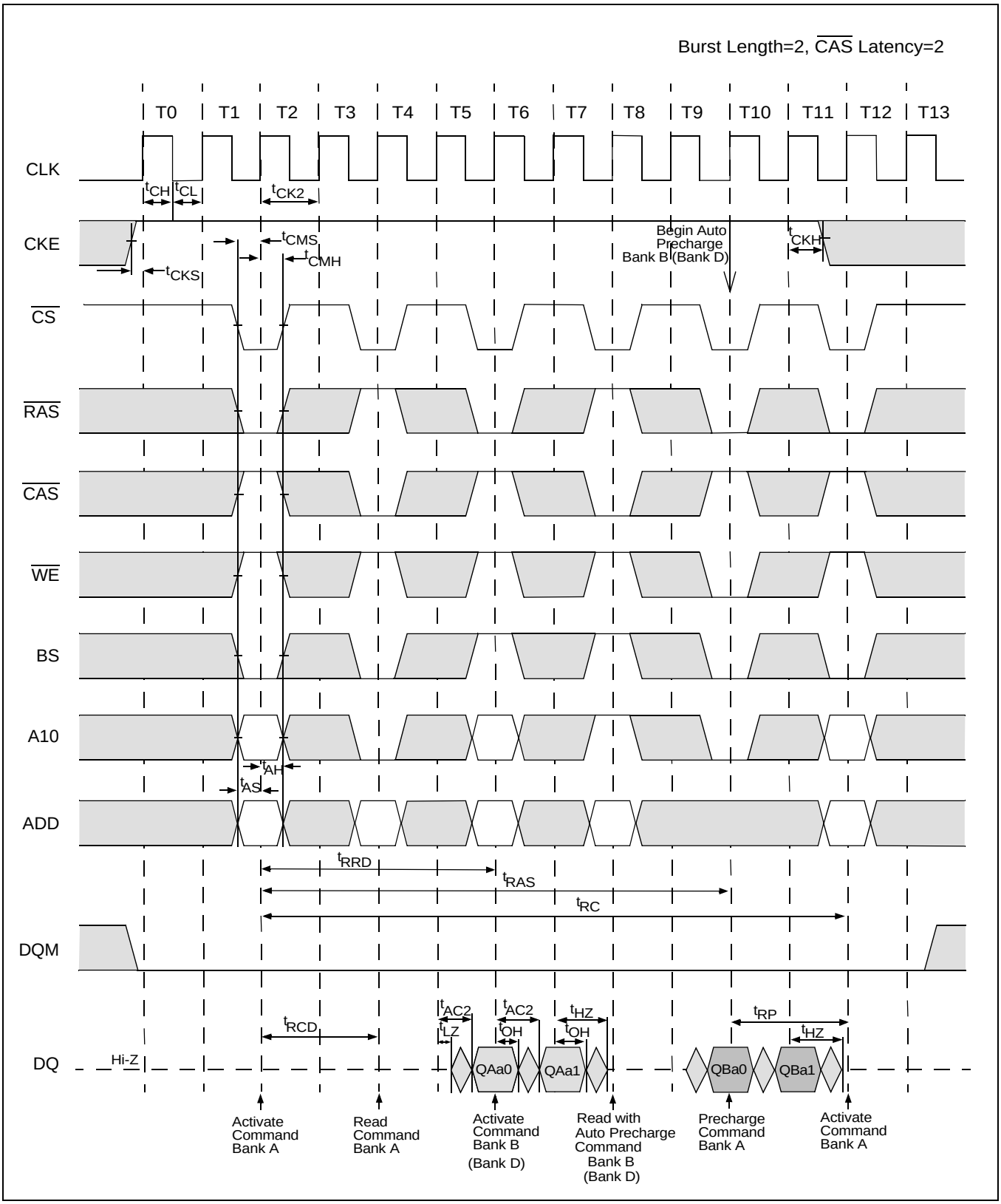
AC Parameters for Write Timing (1 of 2)



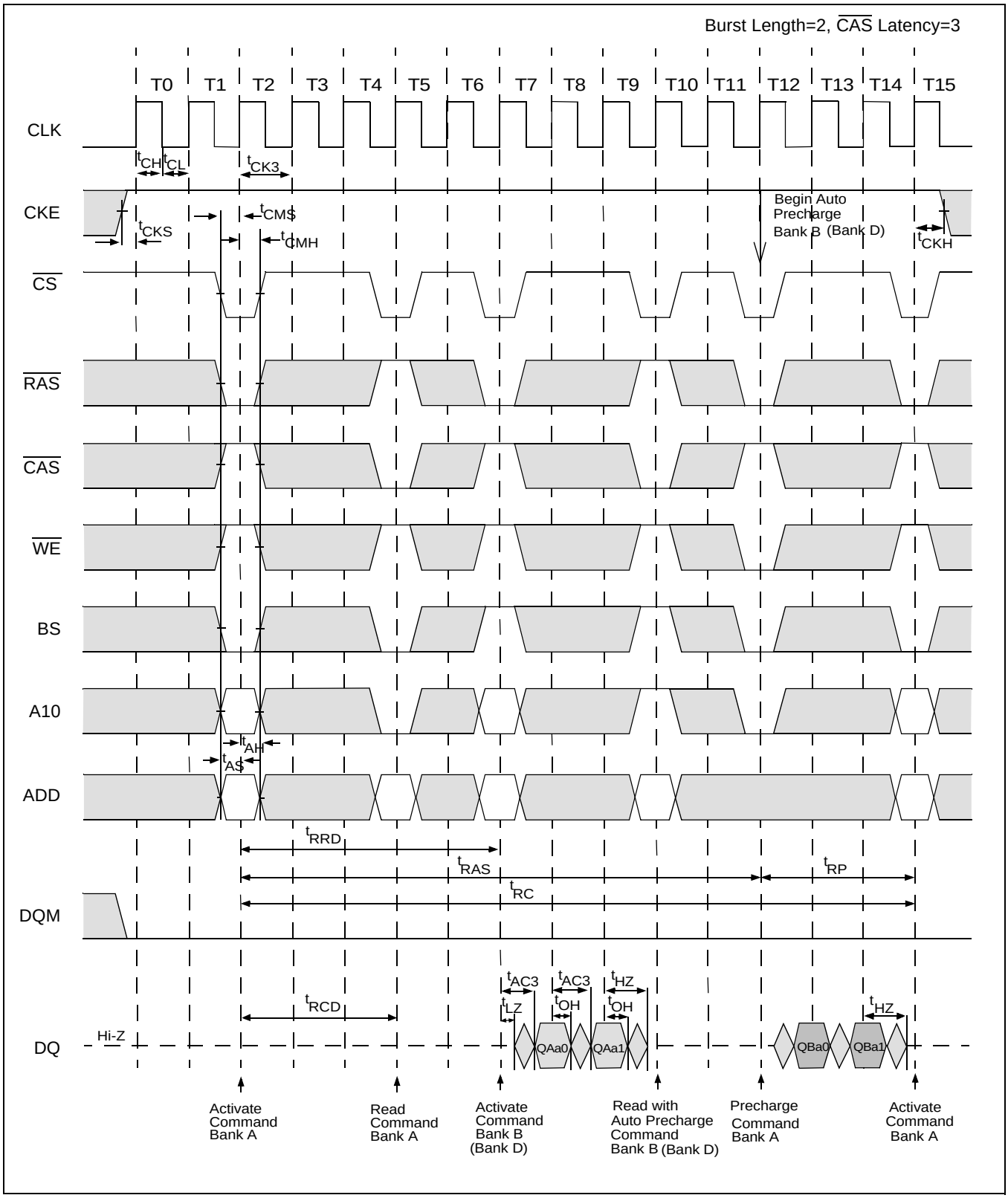
AC Parameters for Write Timing (2 of 2)



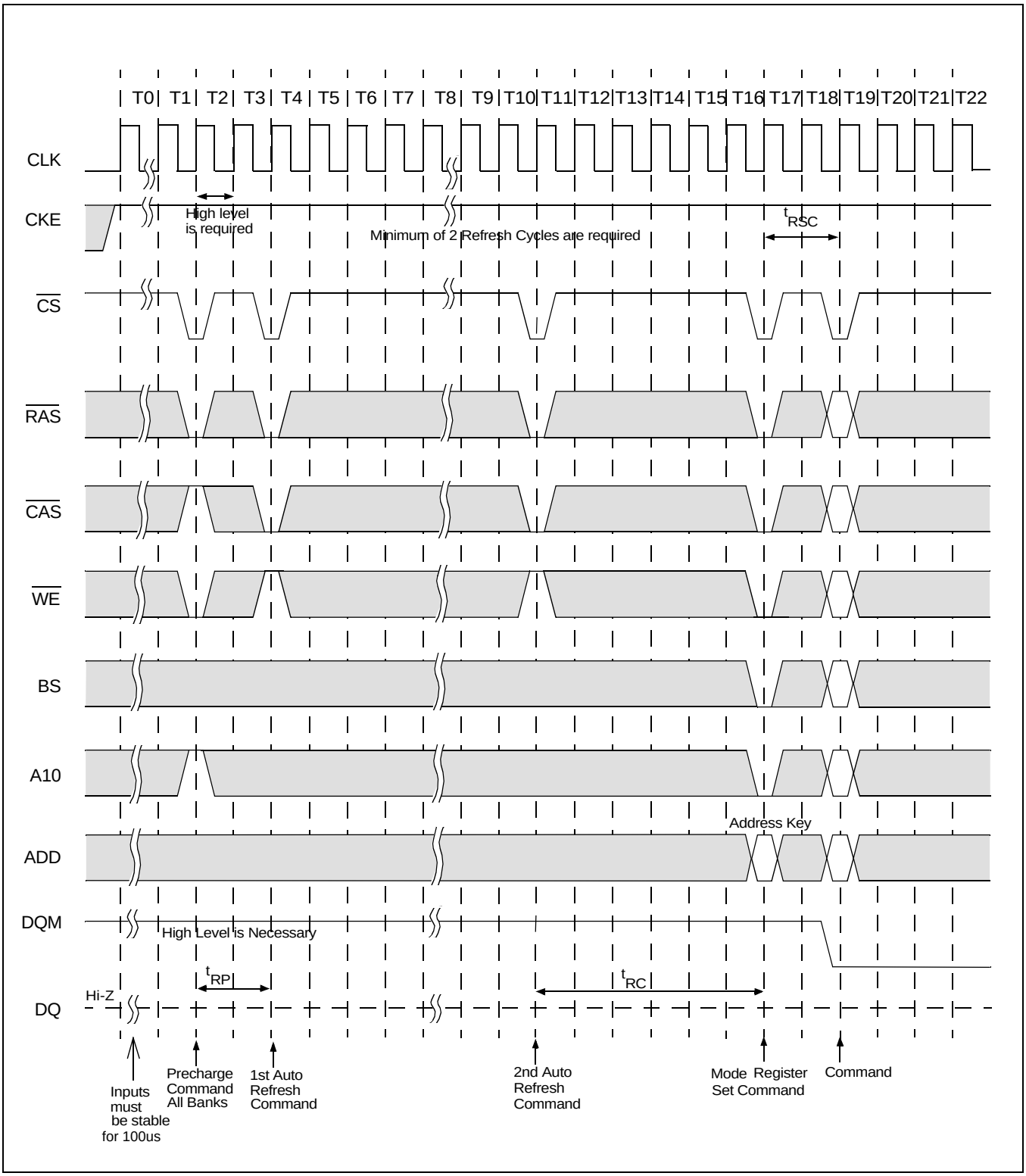
AC Parameters for Read Timing (1 of 2)



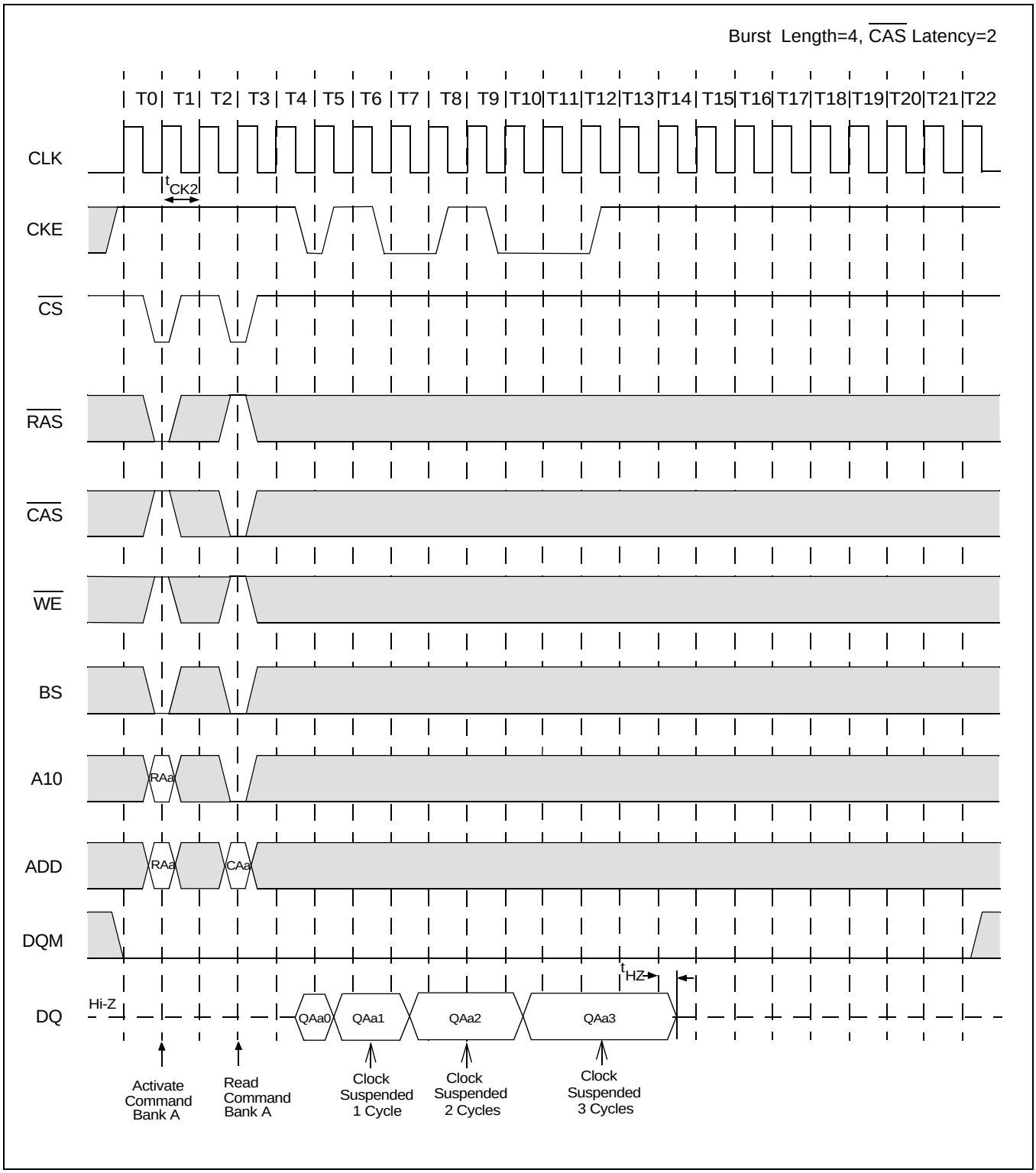
AC Parameters for Read Timing (2 of 2)



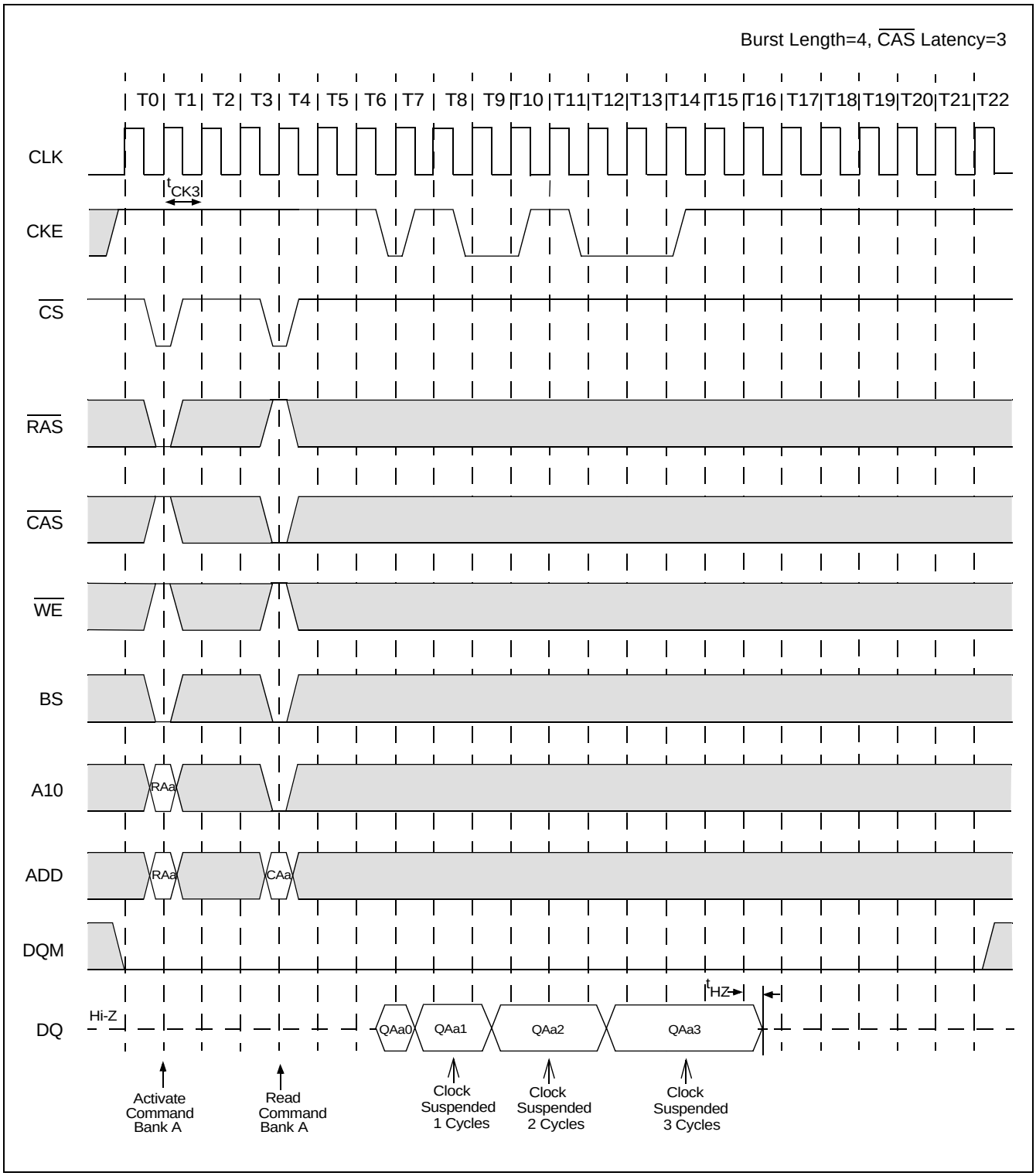
Power on Sequence and Auto Refresh (CBR)



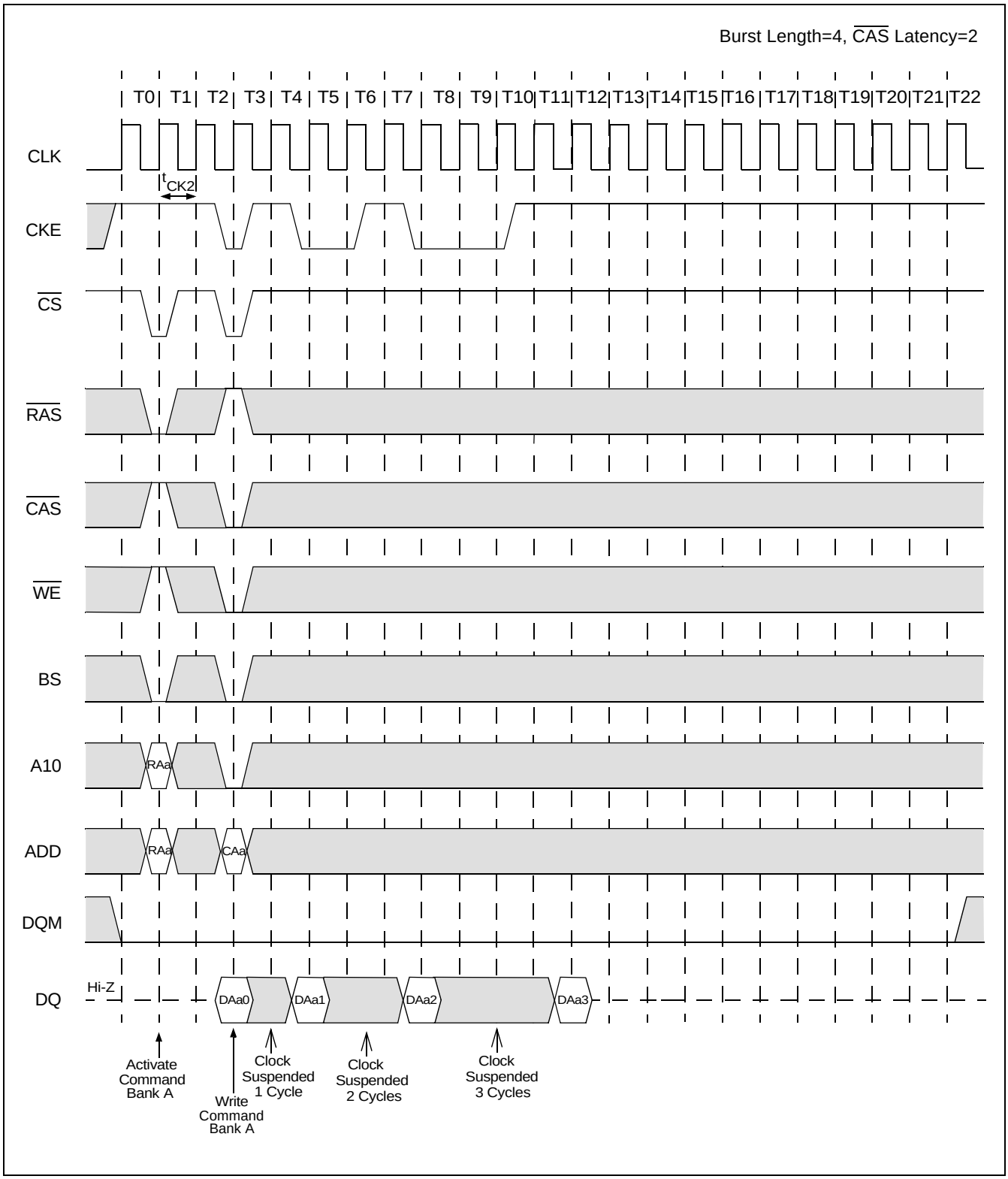
Clock Suspension During Burst Read (Using CKE) (1 of 2)



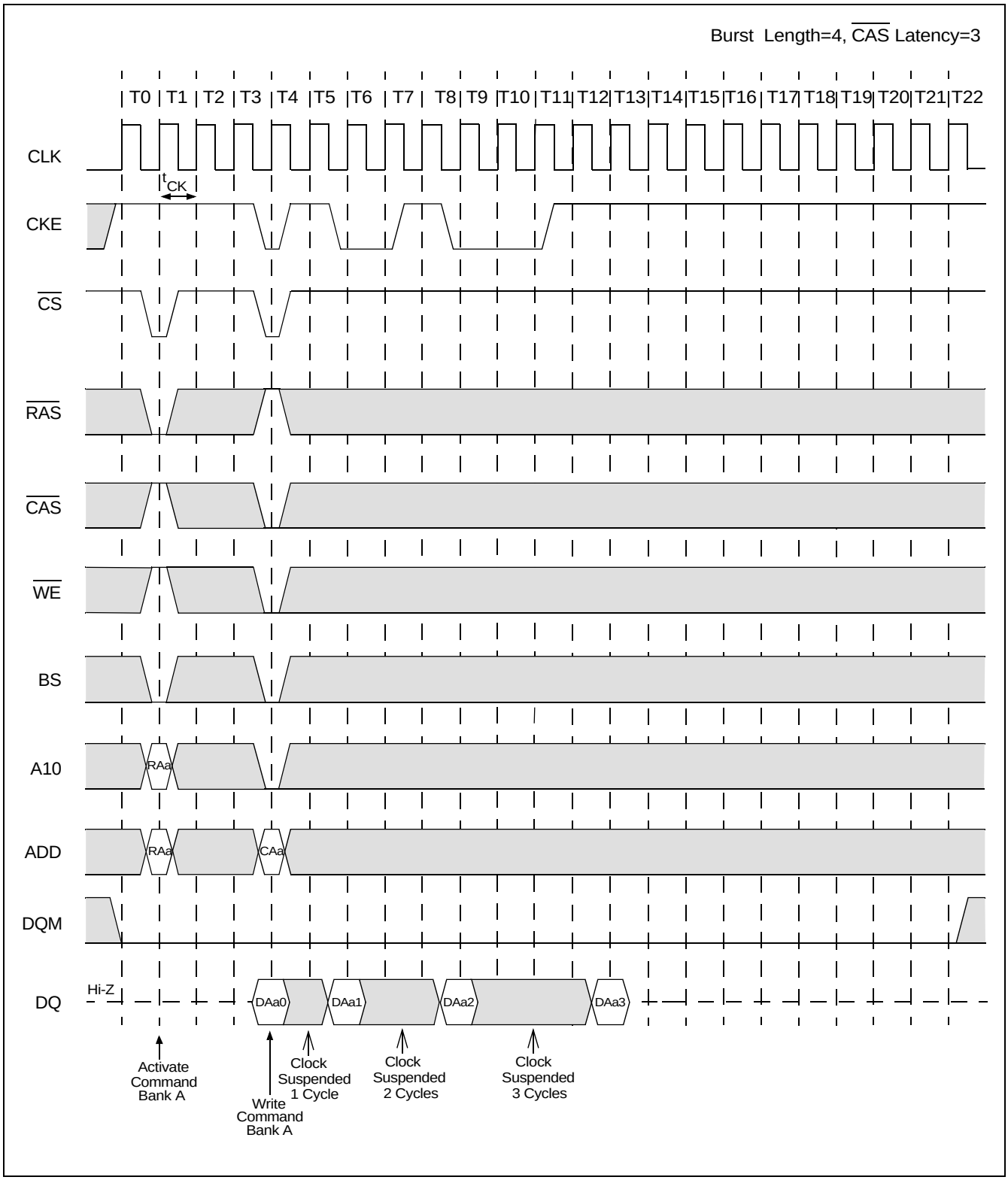
Clock Suspension During Burst Read (Using CKE) (2 of 2)



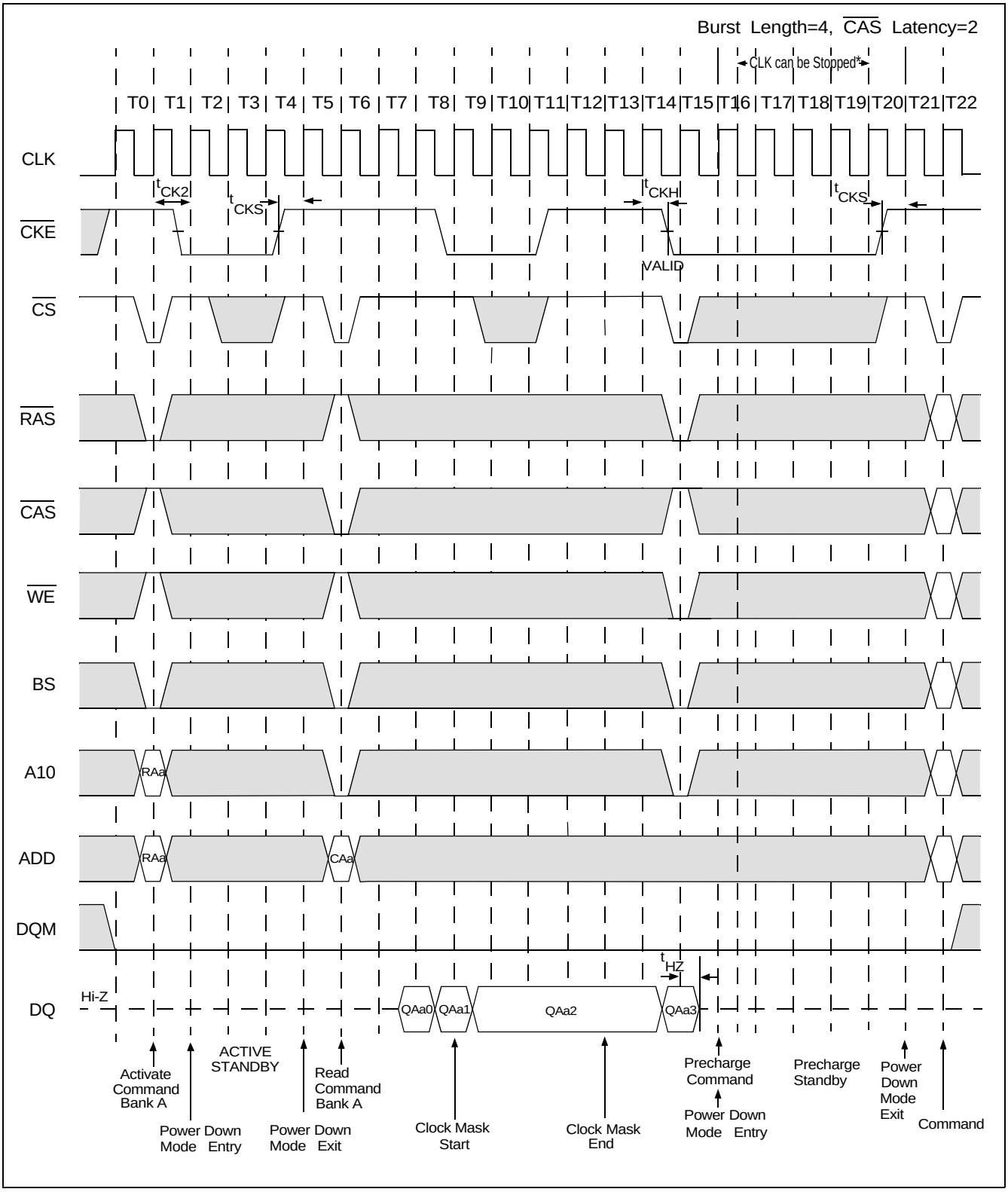
Clock Suspension During Burst Write (Using CKE) (1 of 2)



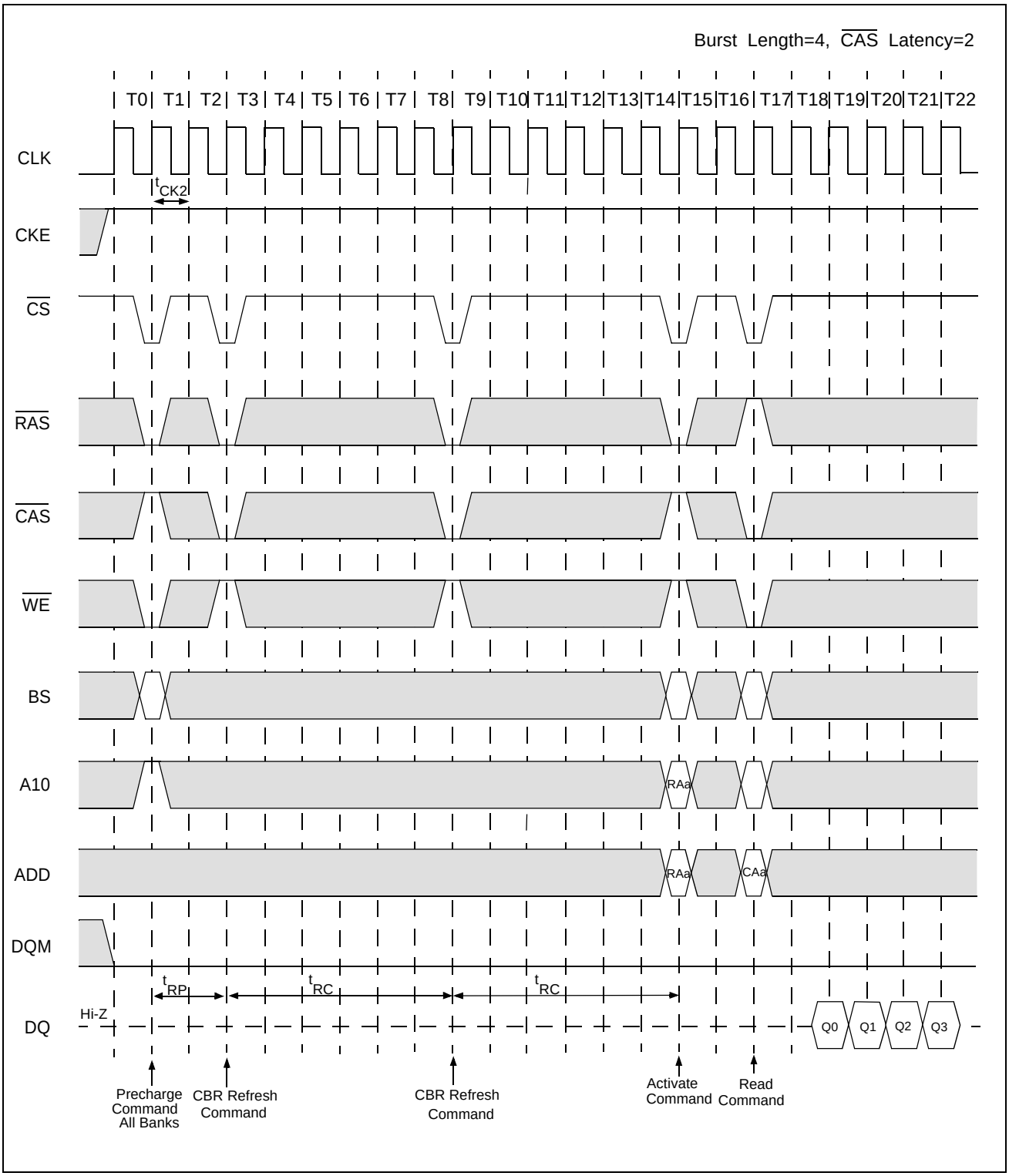
Clock Suspension During Burst Write (Using CKE) (2 of 2)



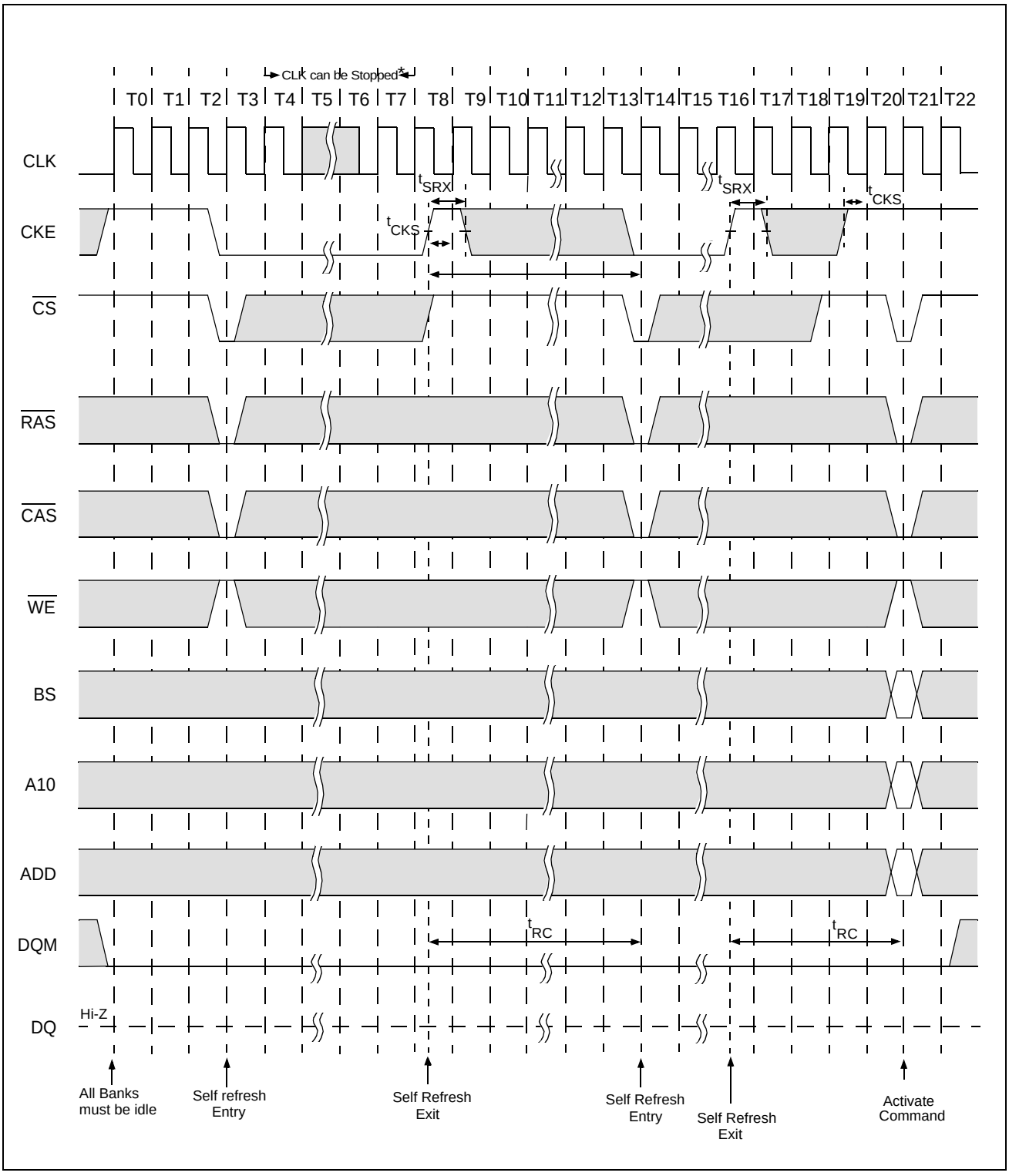
Power Down Mode and Clock Mask



Auto Refresh (CBR)

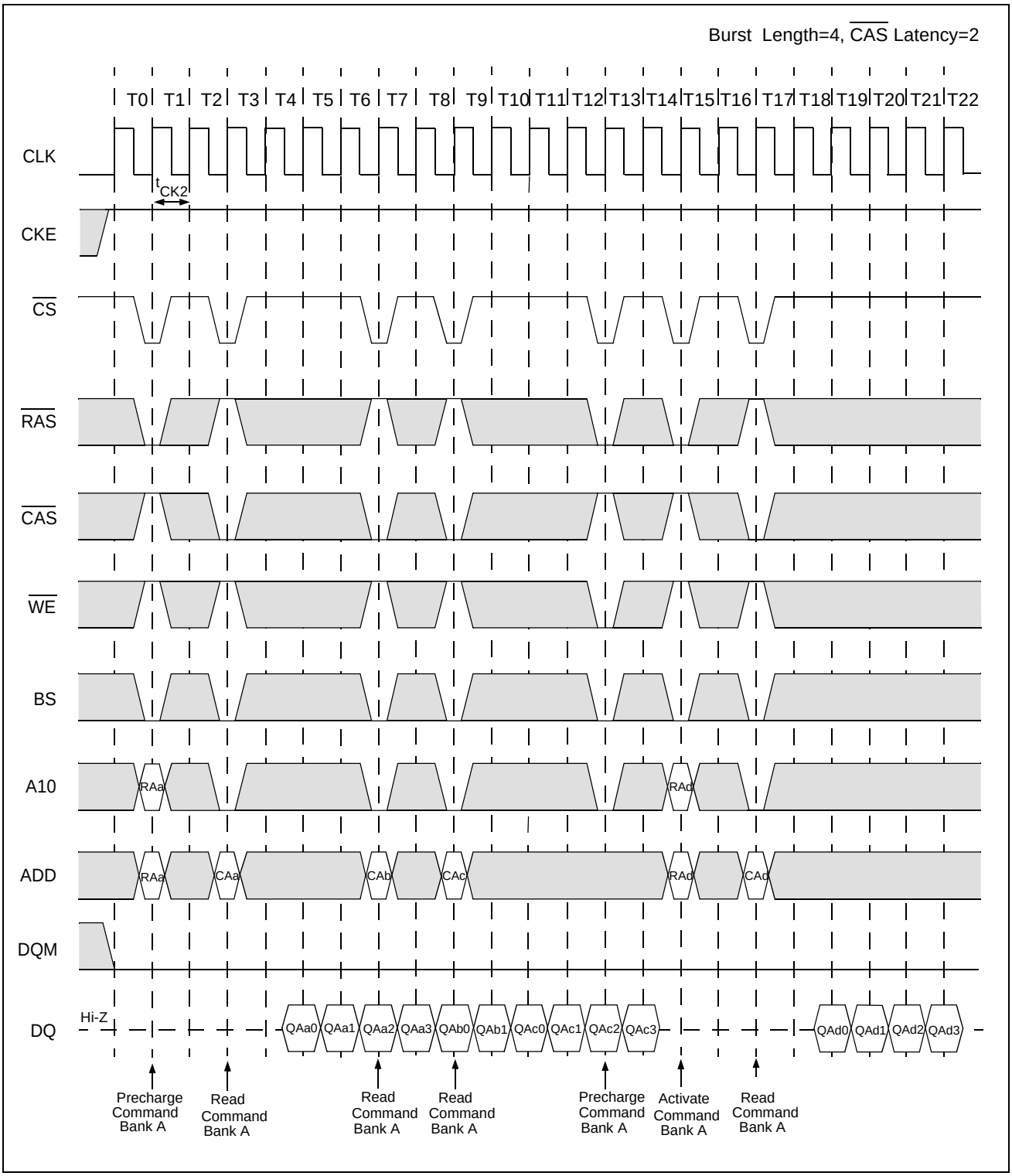


Self Refresh (Entry and Exit)

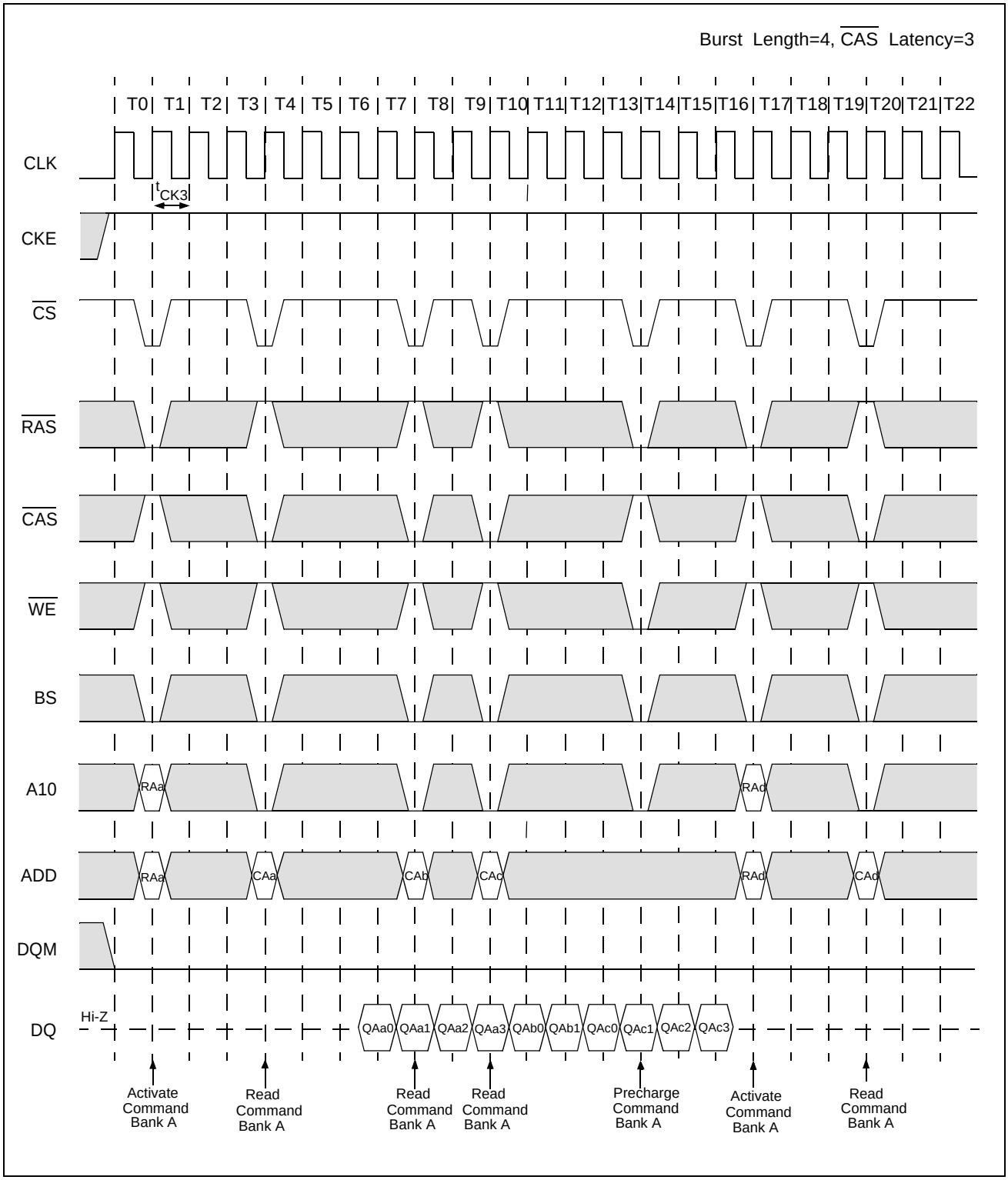


* Clock can be stopped at CKE=Low. If clock is stopped, it must be restarted/stable for 4 clock cycles before CKE=High

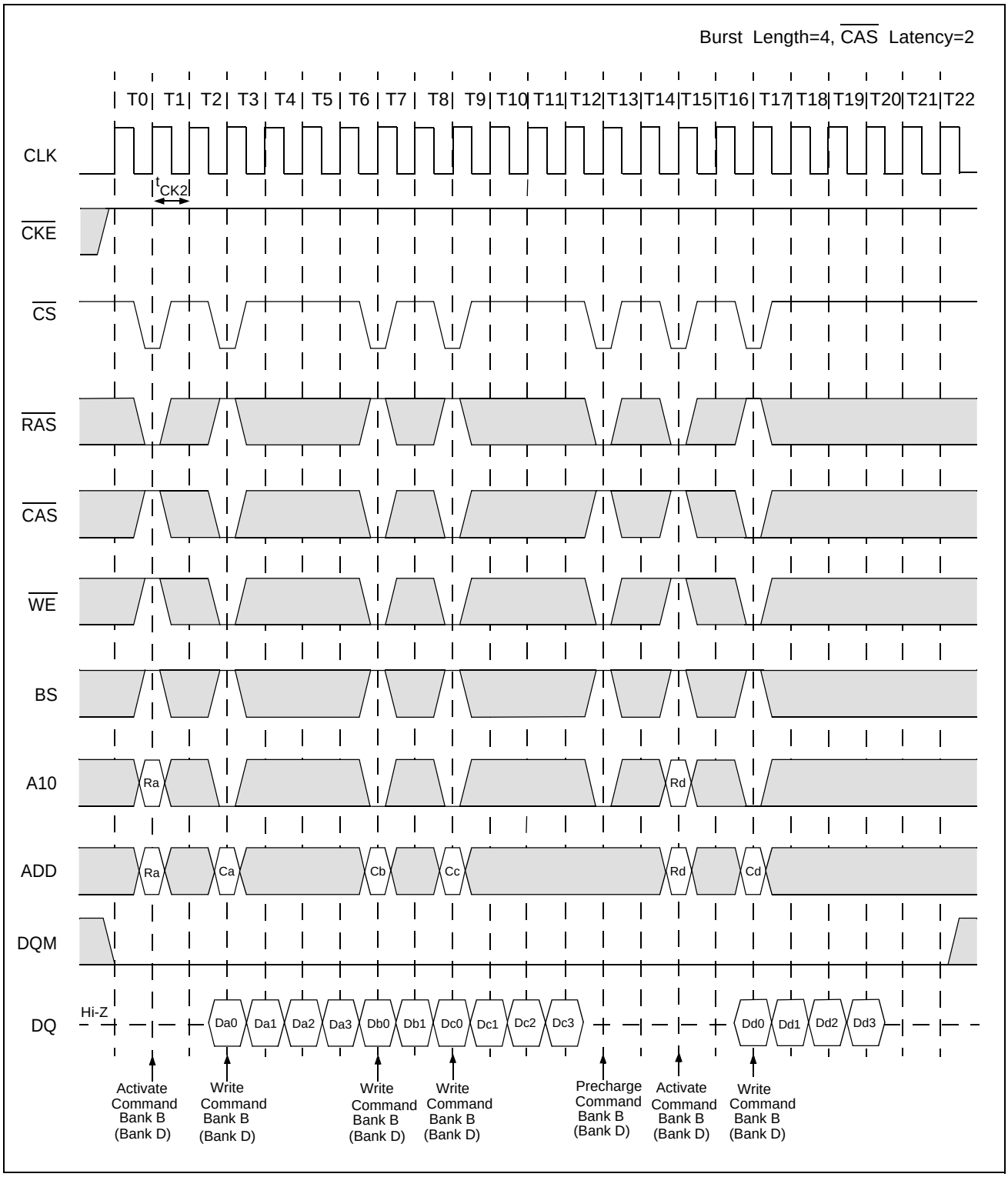
Random Column Read (Page Within same Bank)(1 of 2)



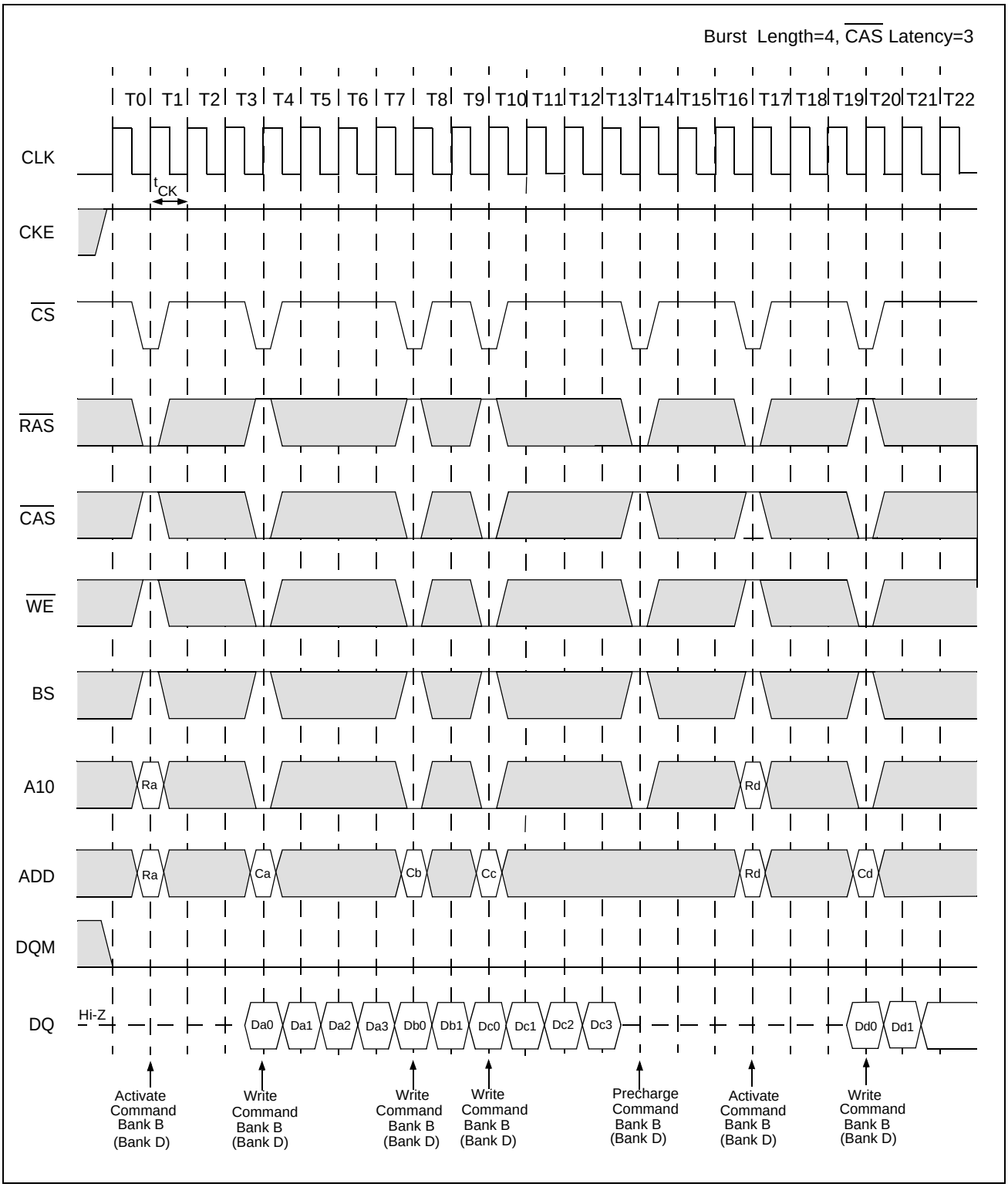
Random Column Read (Page Within same Bank)(2 of 2)



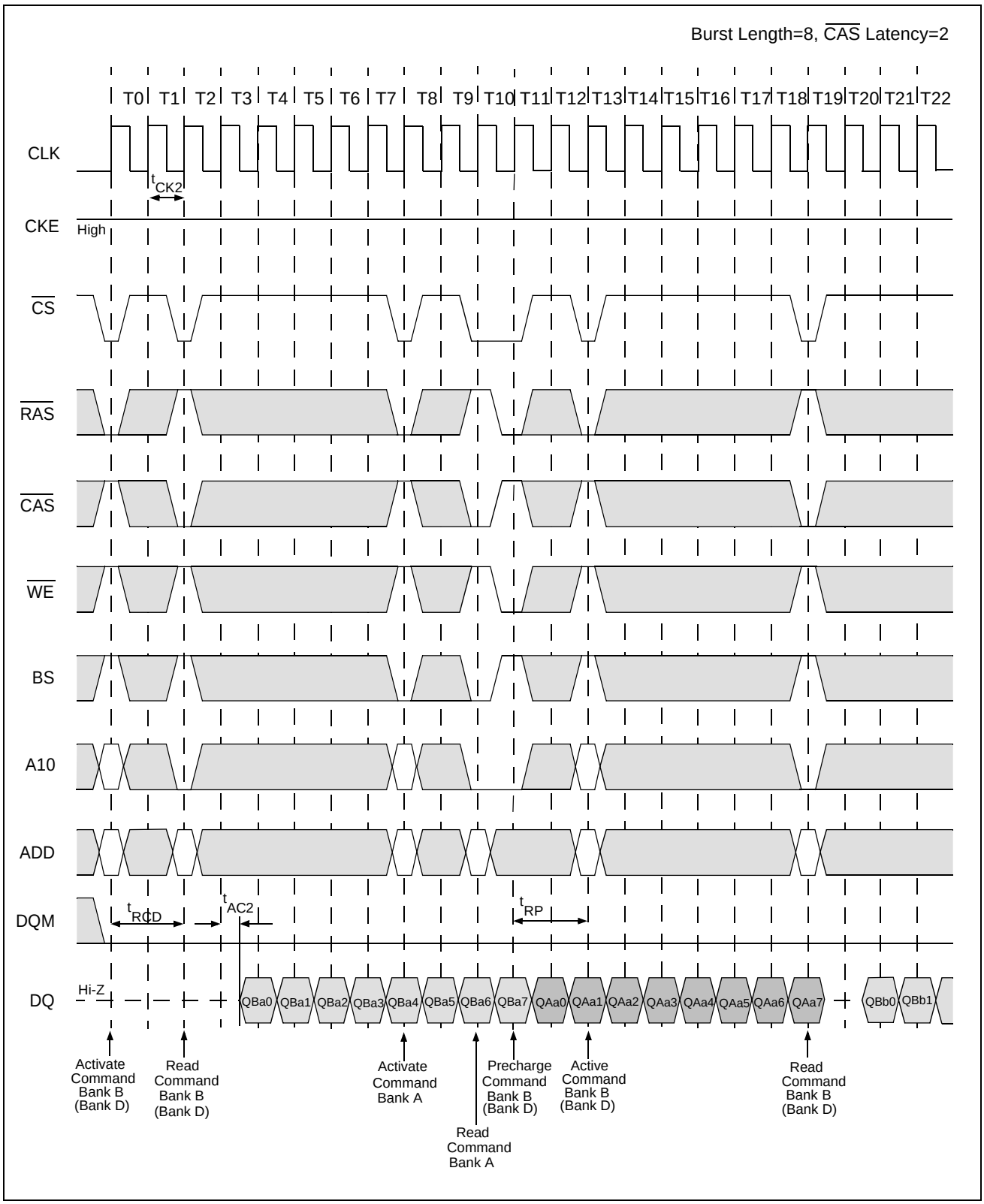
Random Column Write (Page Within same Bank) (1 of 2)



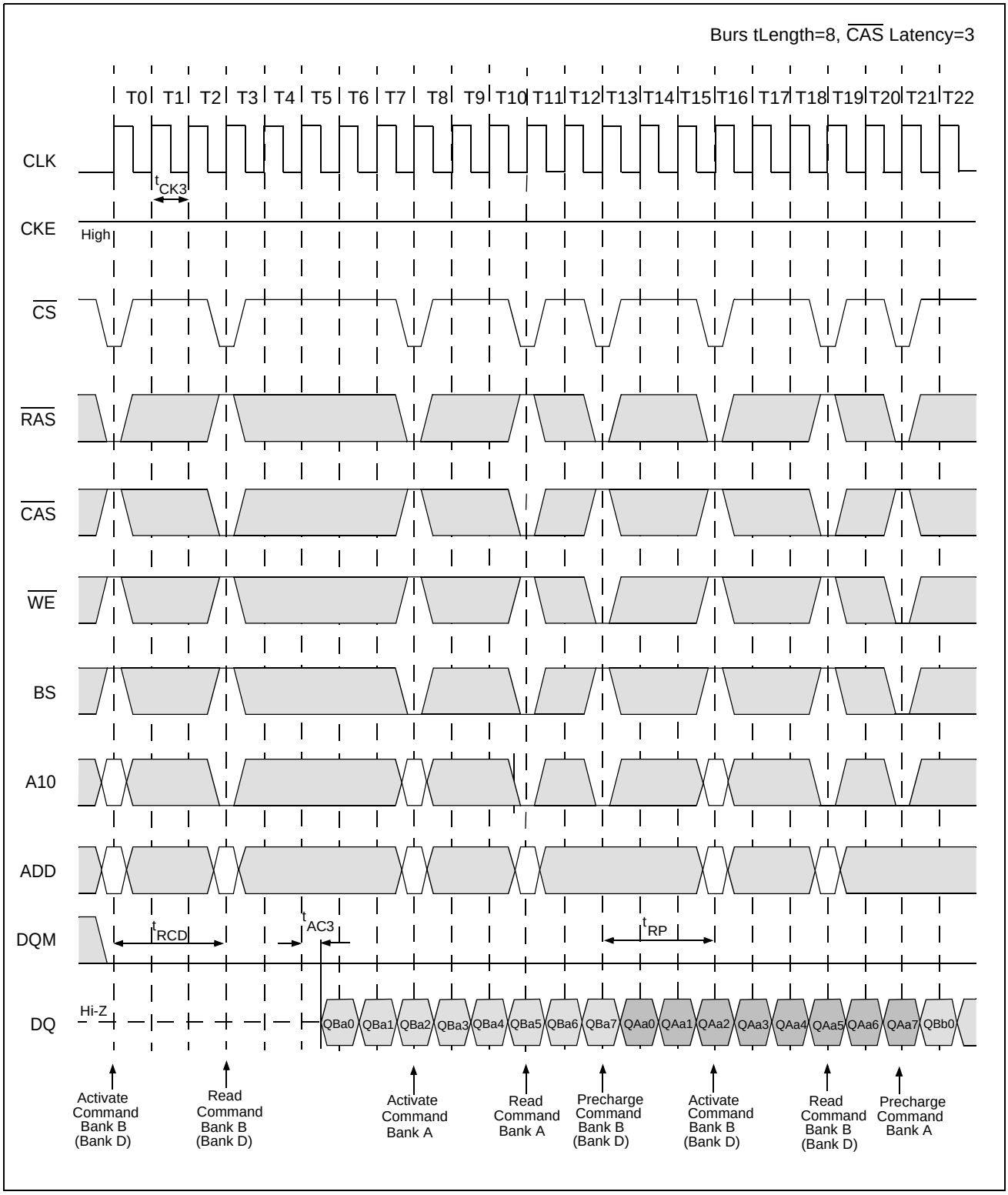
Random Column Write (Page Within same Bank) (1 of 2)



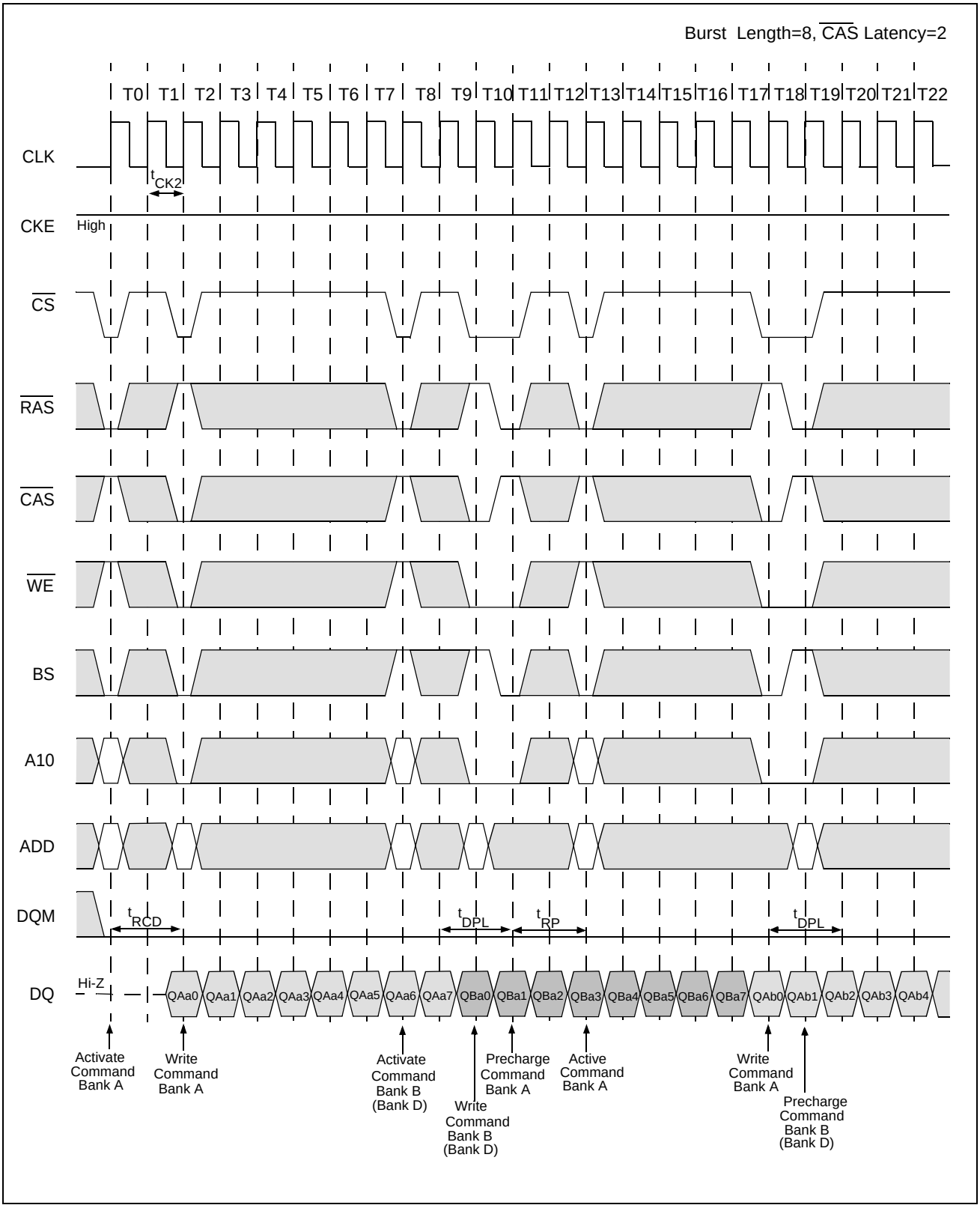
Random Row Read (Interleaving Banks)(1 of 2)



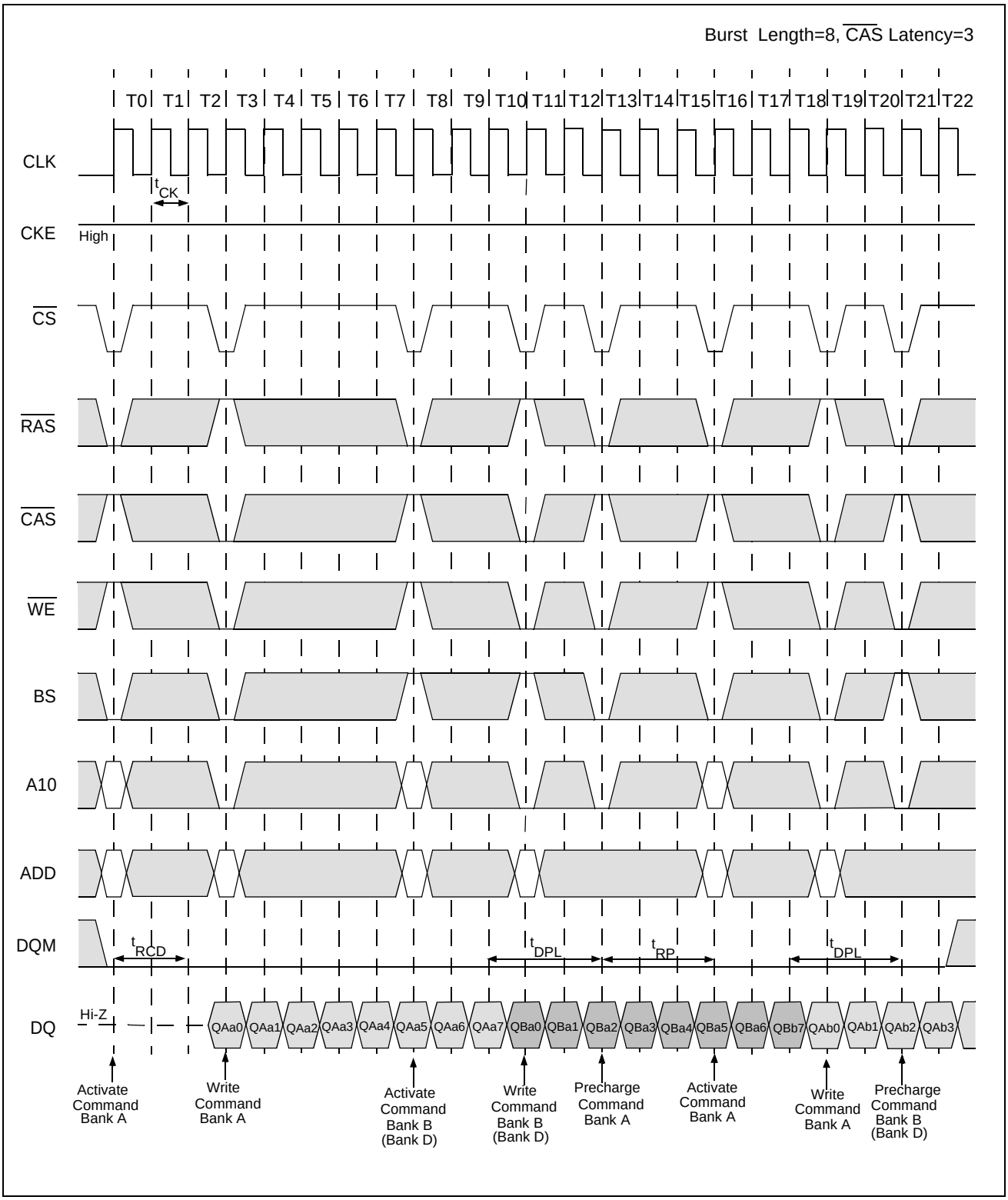
Random Row Read (Interleaving Banks) (2 of 3)



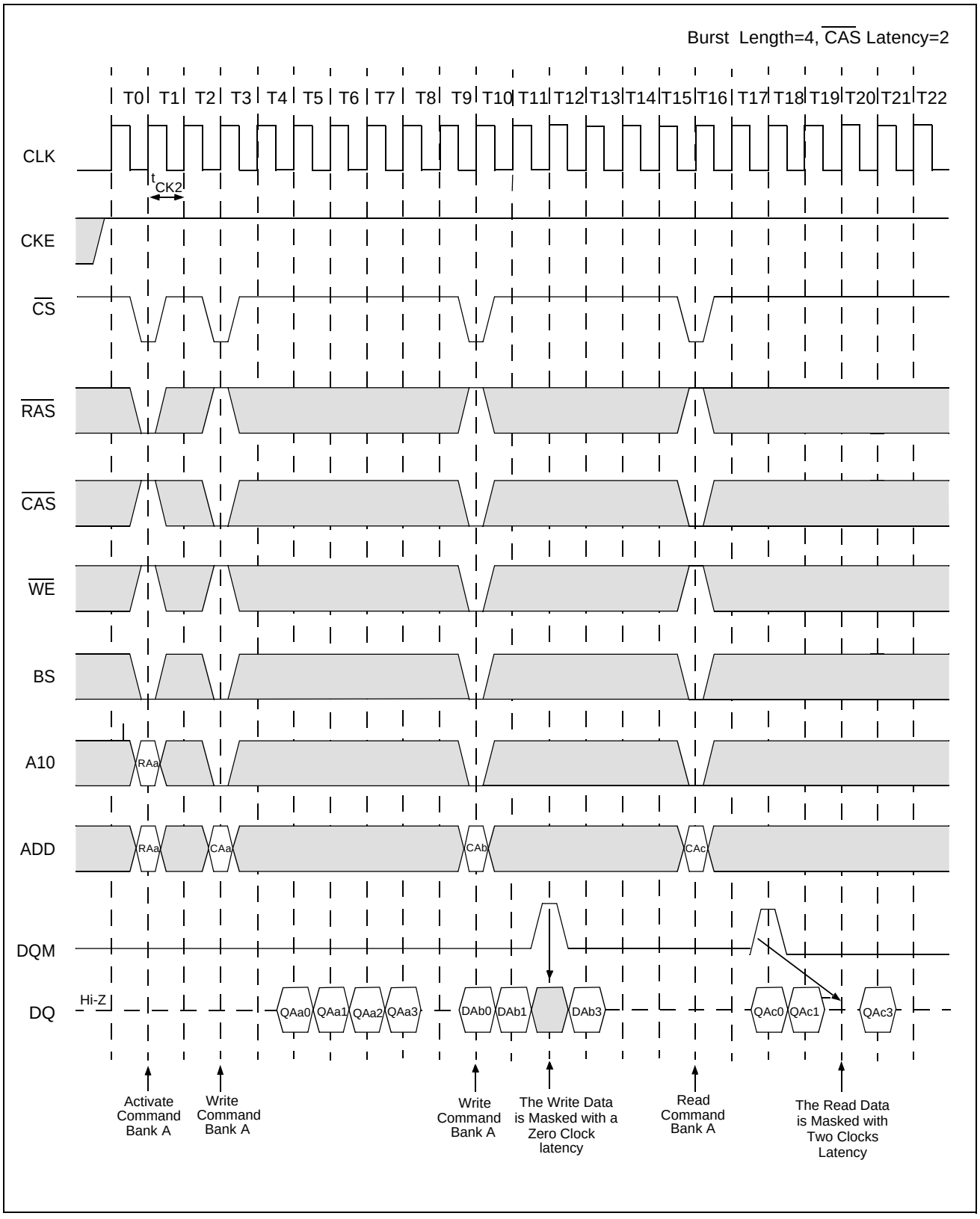
Random Row Write (Interleaving Banks) (1 of 2)



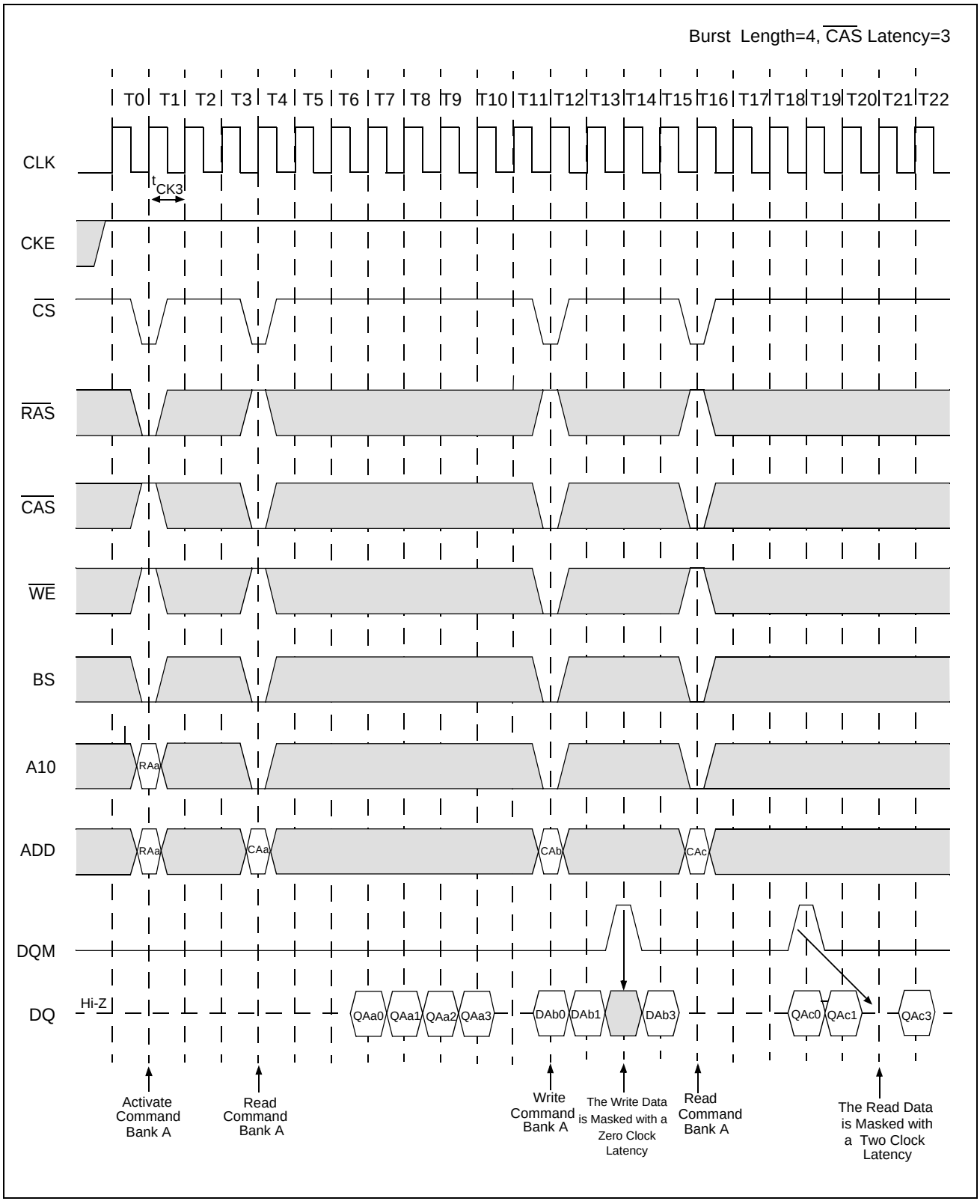
Random Row Write (Interleaving Banks) (2 of 2)



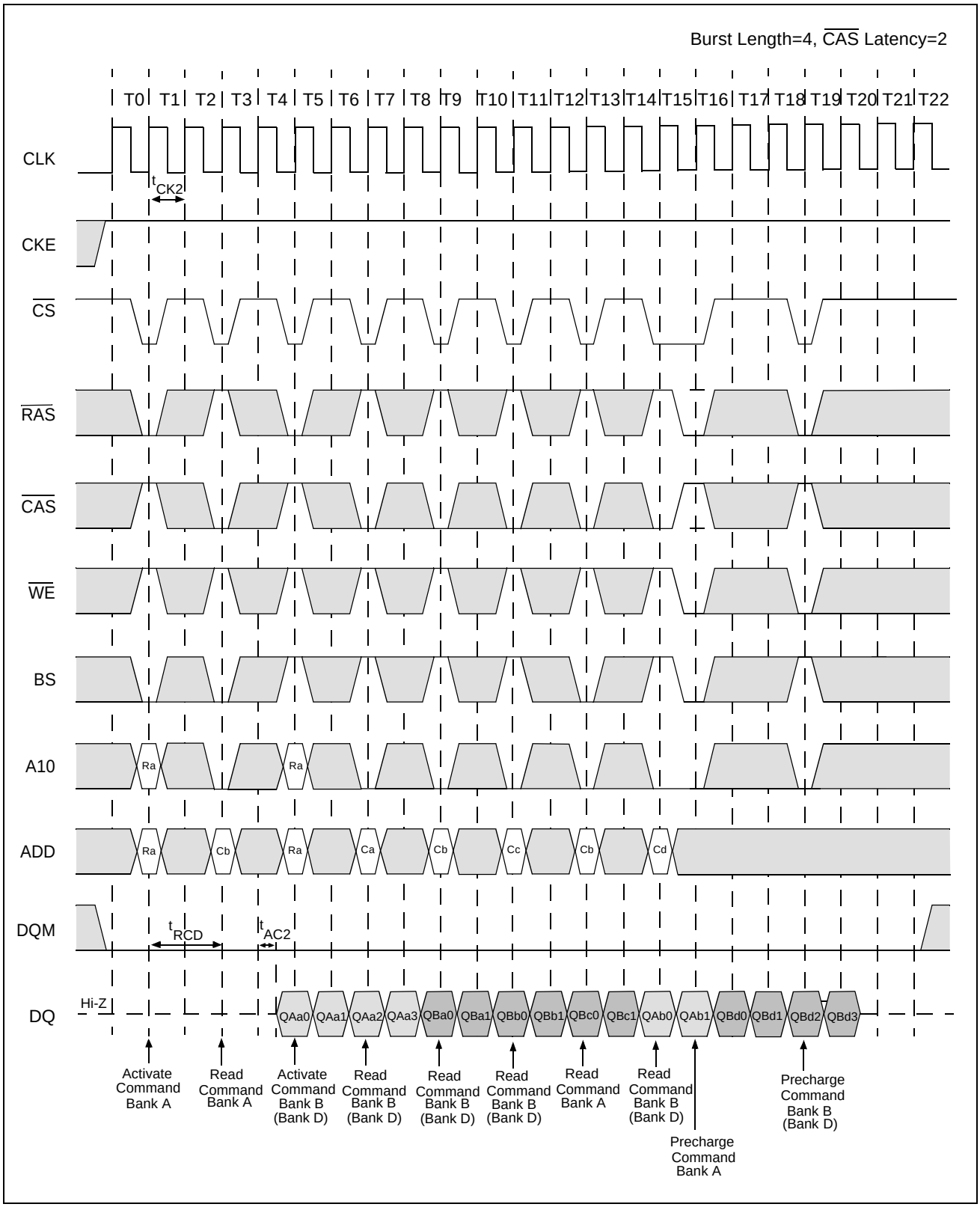
Read and Write Cycle (1 of 2)



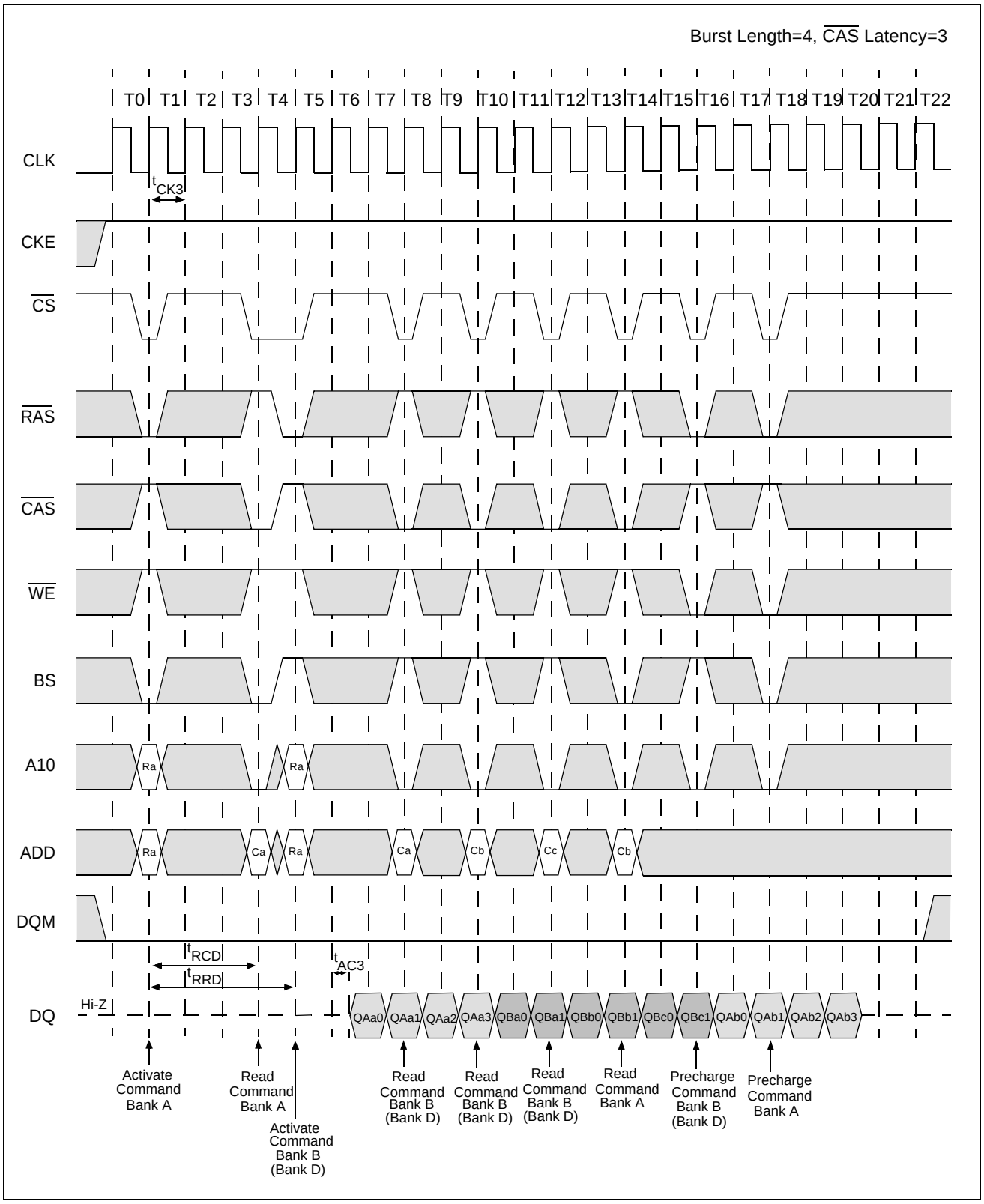
Read and Write Cycle (2 of 2)



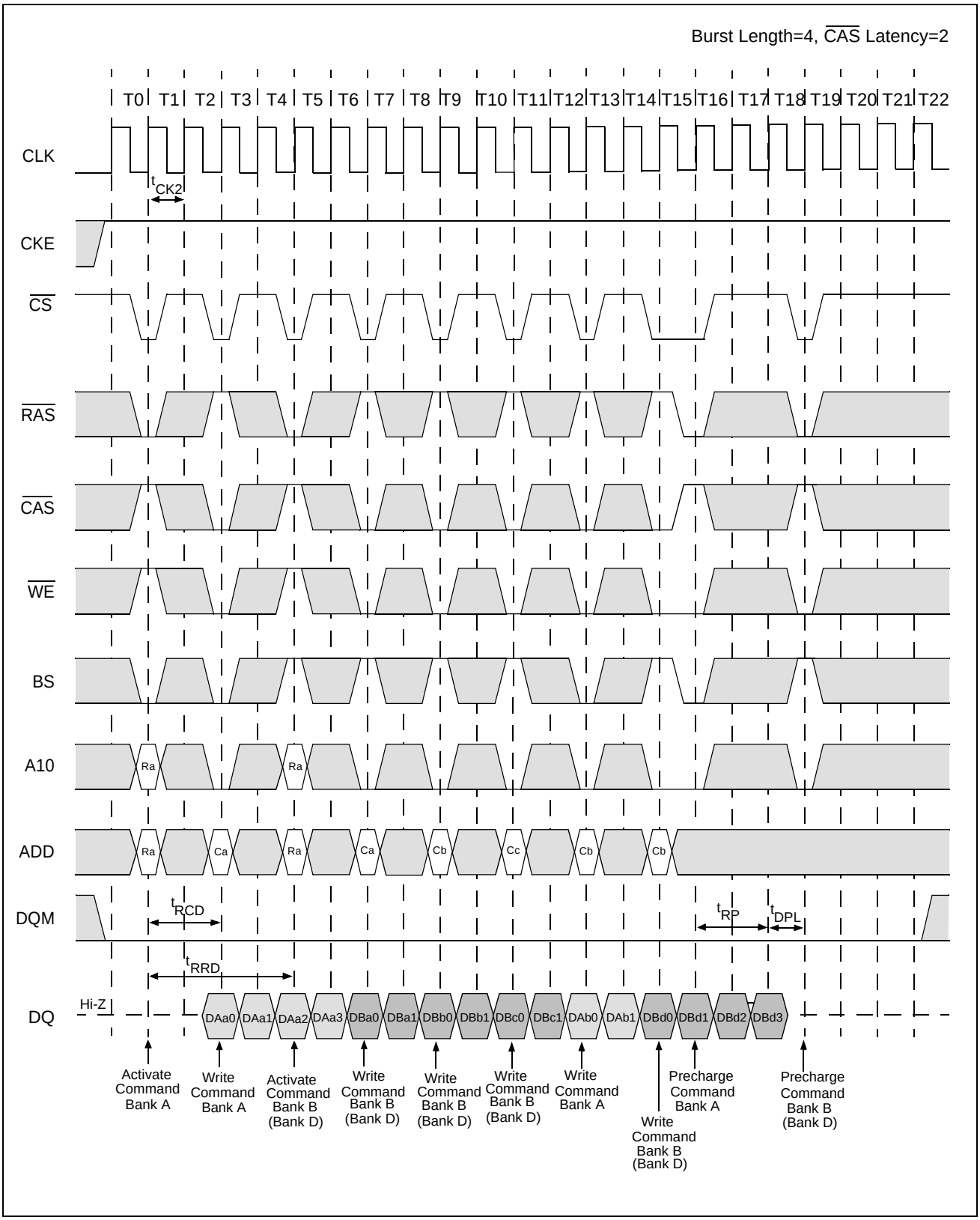
Interleaved Column Read Cycle (1 of 2)



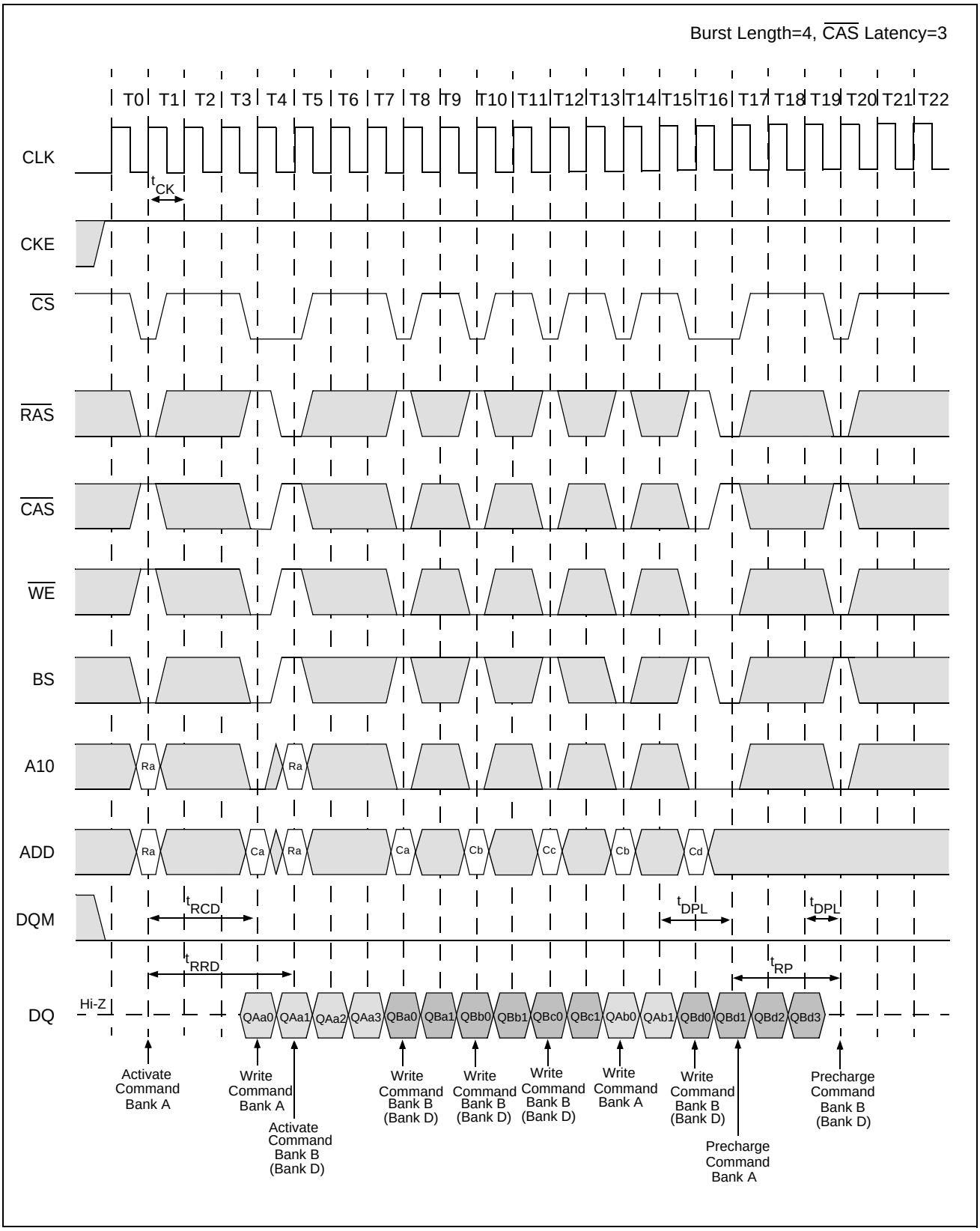
Interleaved Column Read Cycle (2 of 2)



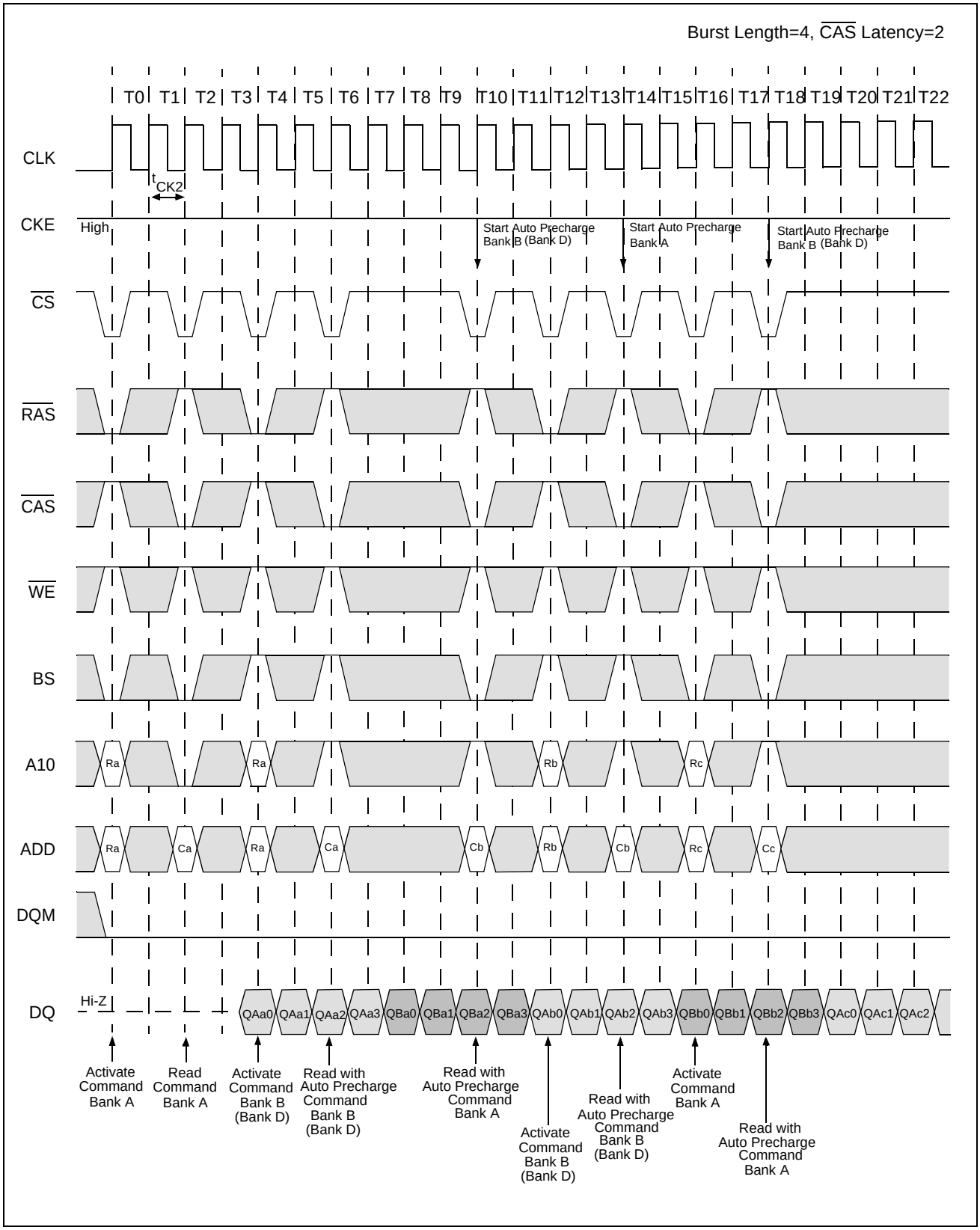
Interleaved Column Write Cycle (1 of 2)



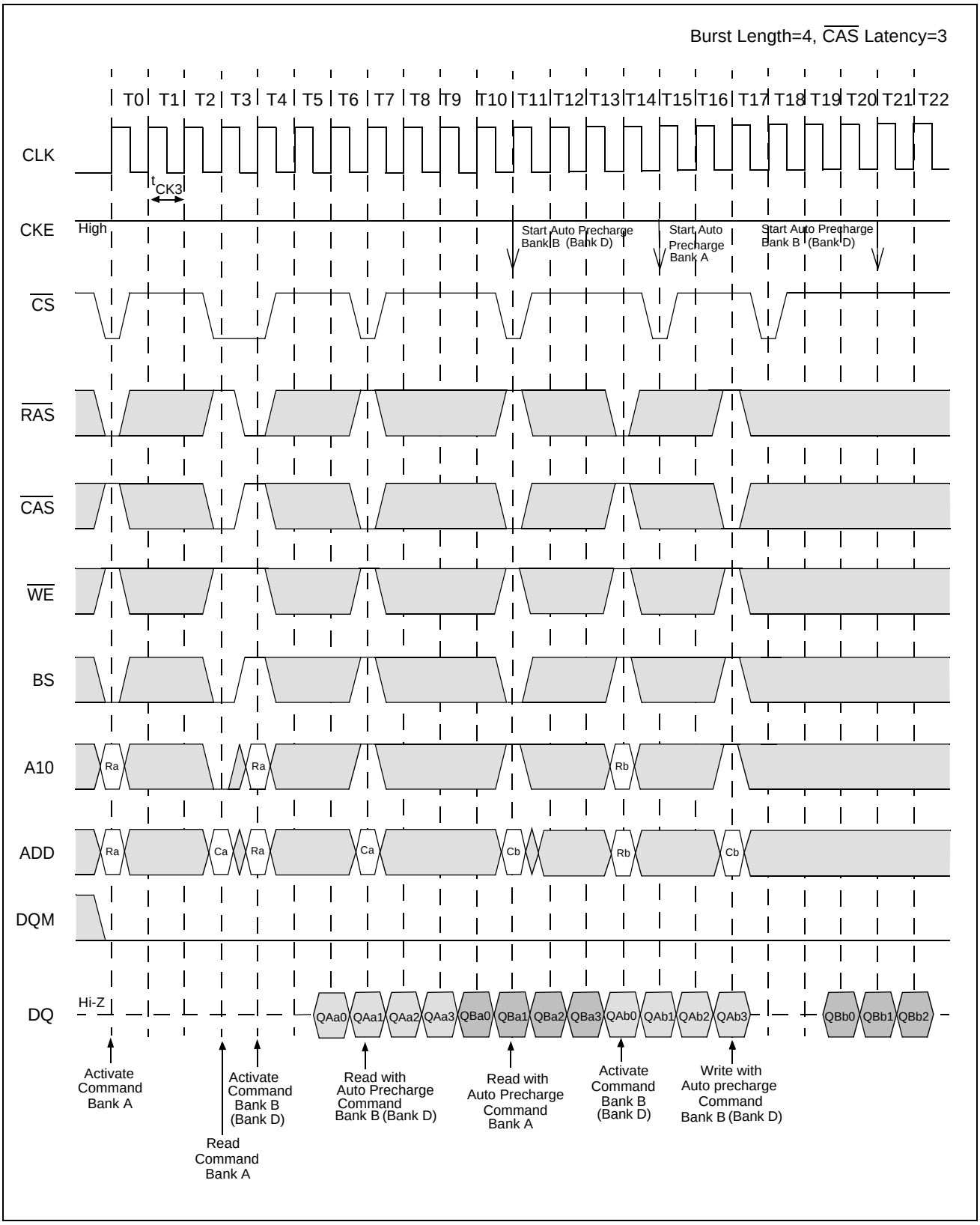
Interleaved Column Write Cycle (2 of 2)



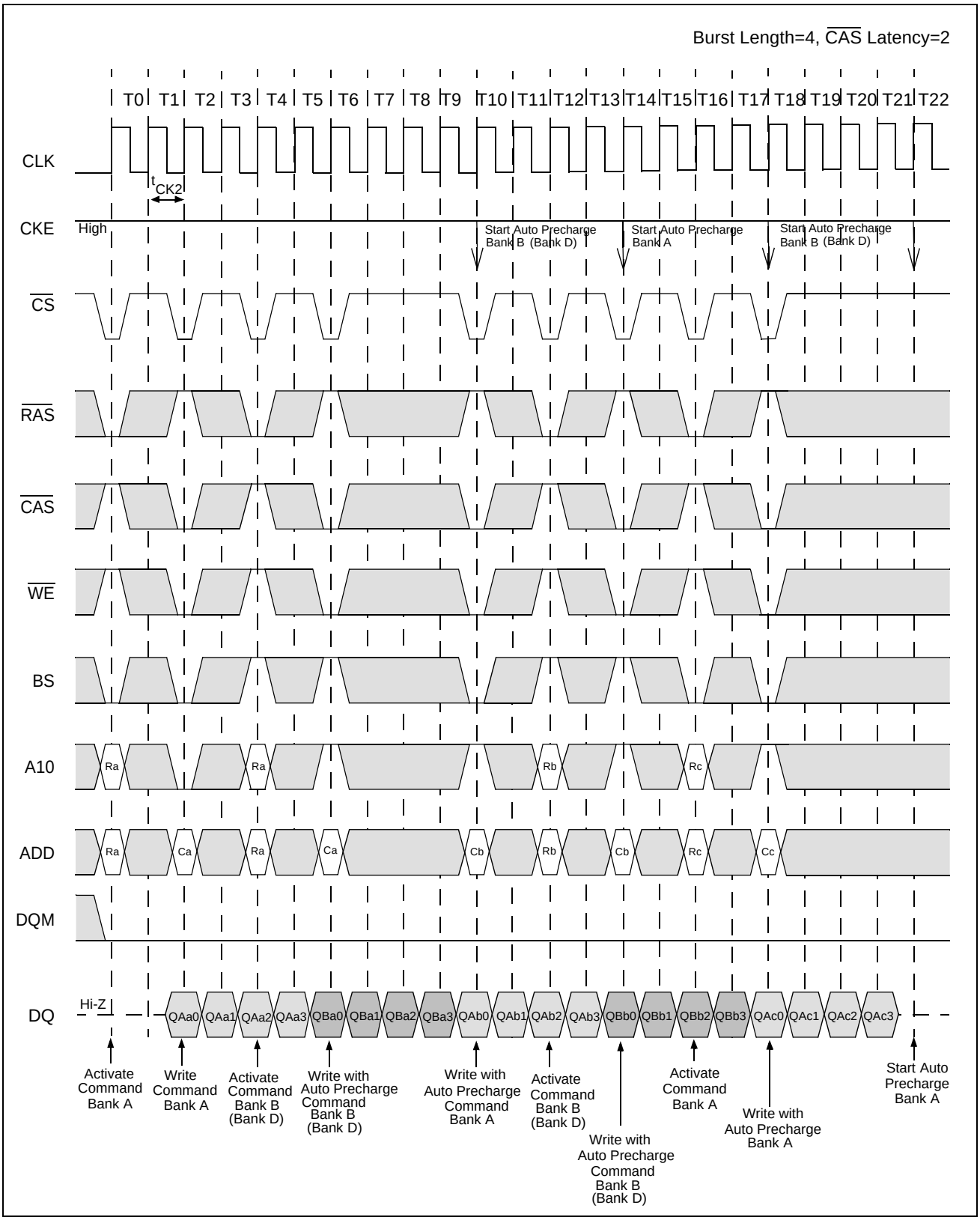
Auto Precharge after Read Burst (1 of 2)



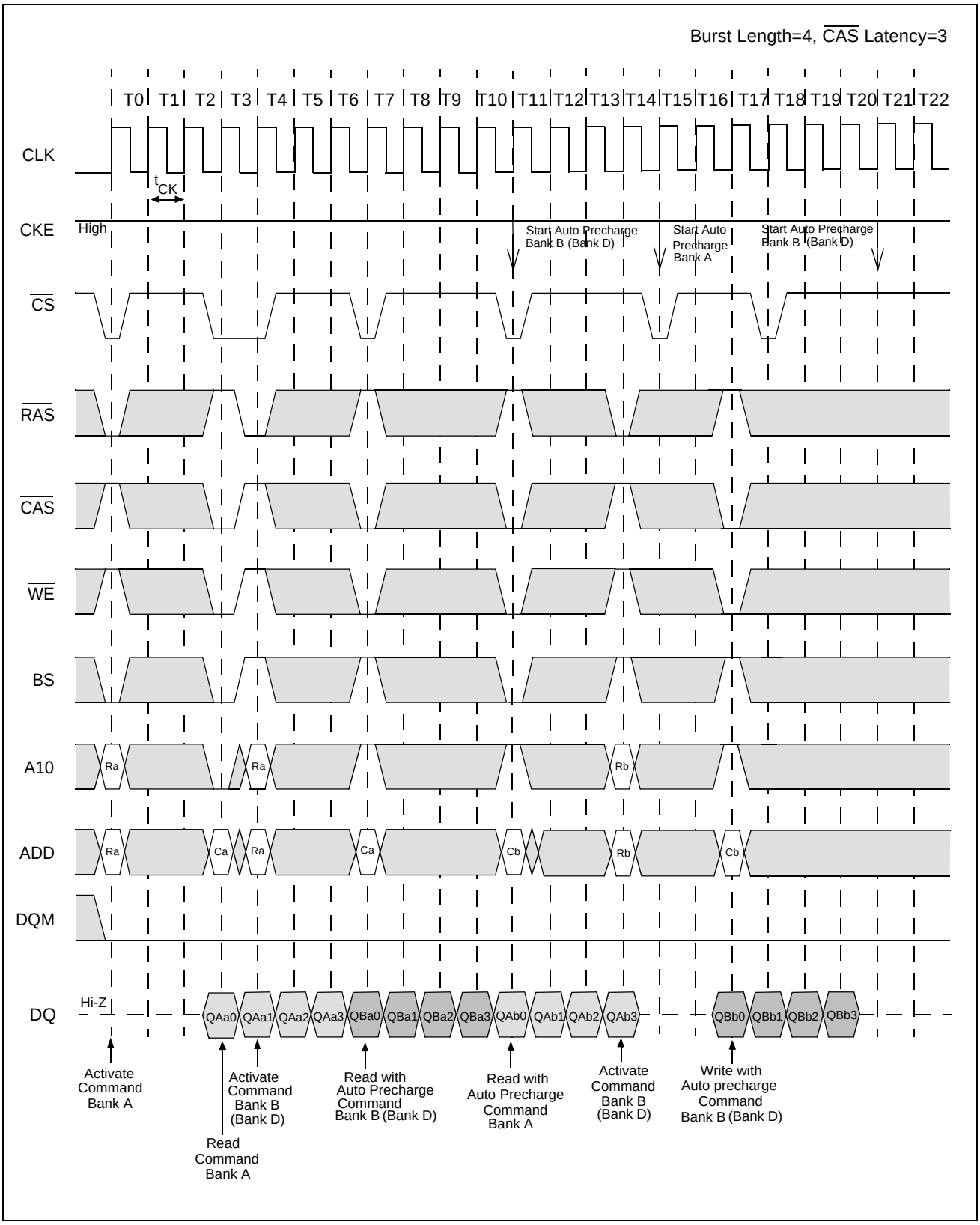
Auto Precharge after Write Burst (2 of 2)



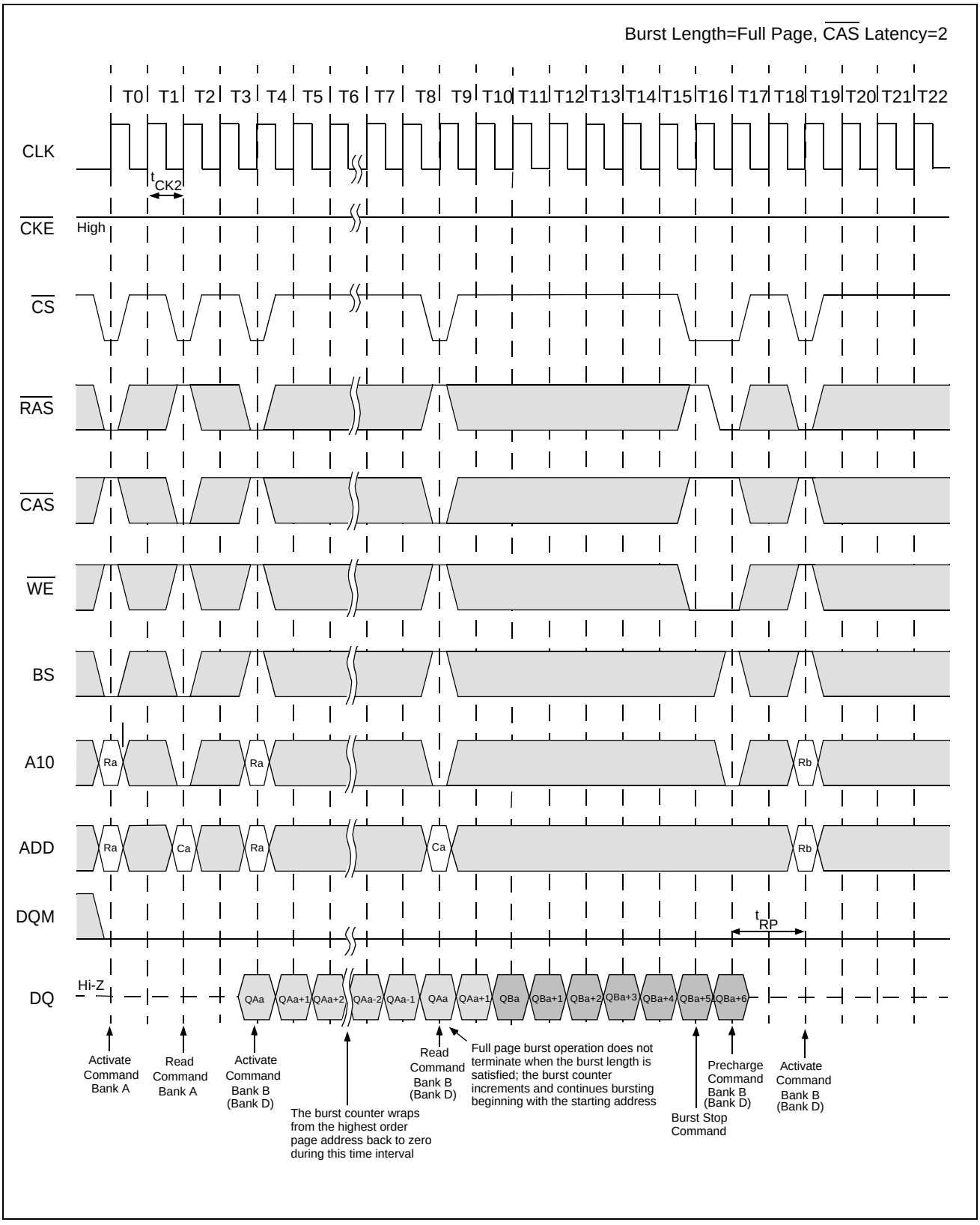
Auto Precharge after Write Burst (1 of 2)



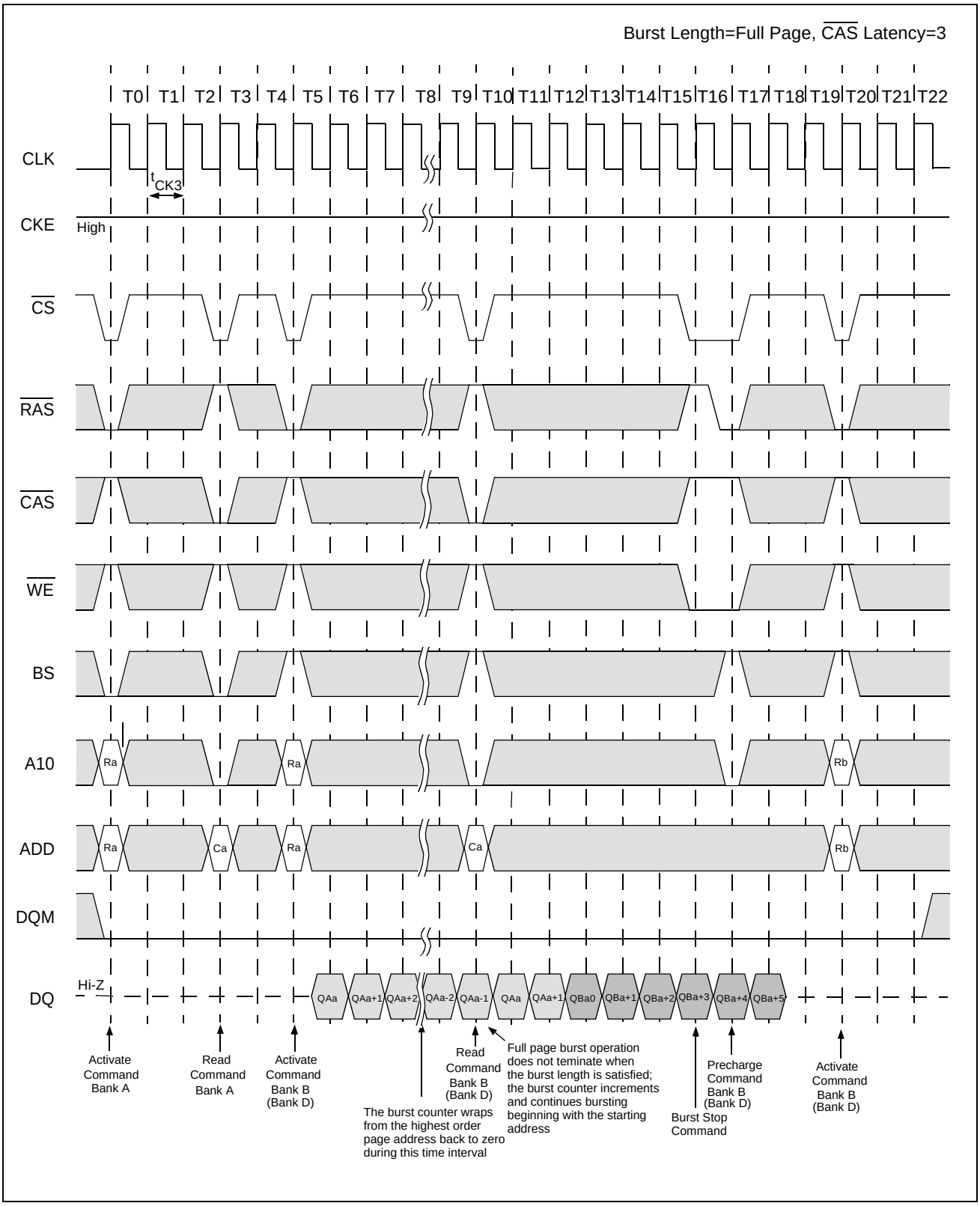
Auto Precharge after Write Burst (2 of 2)



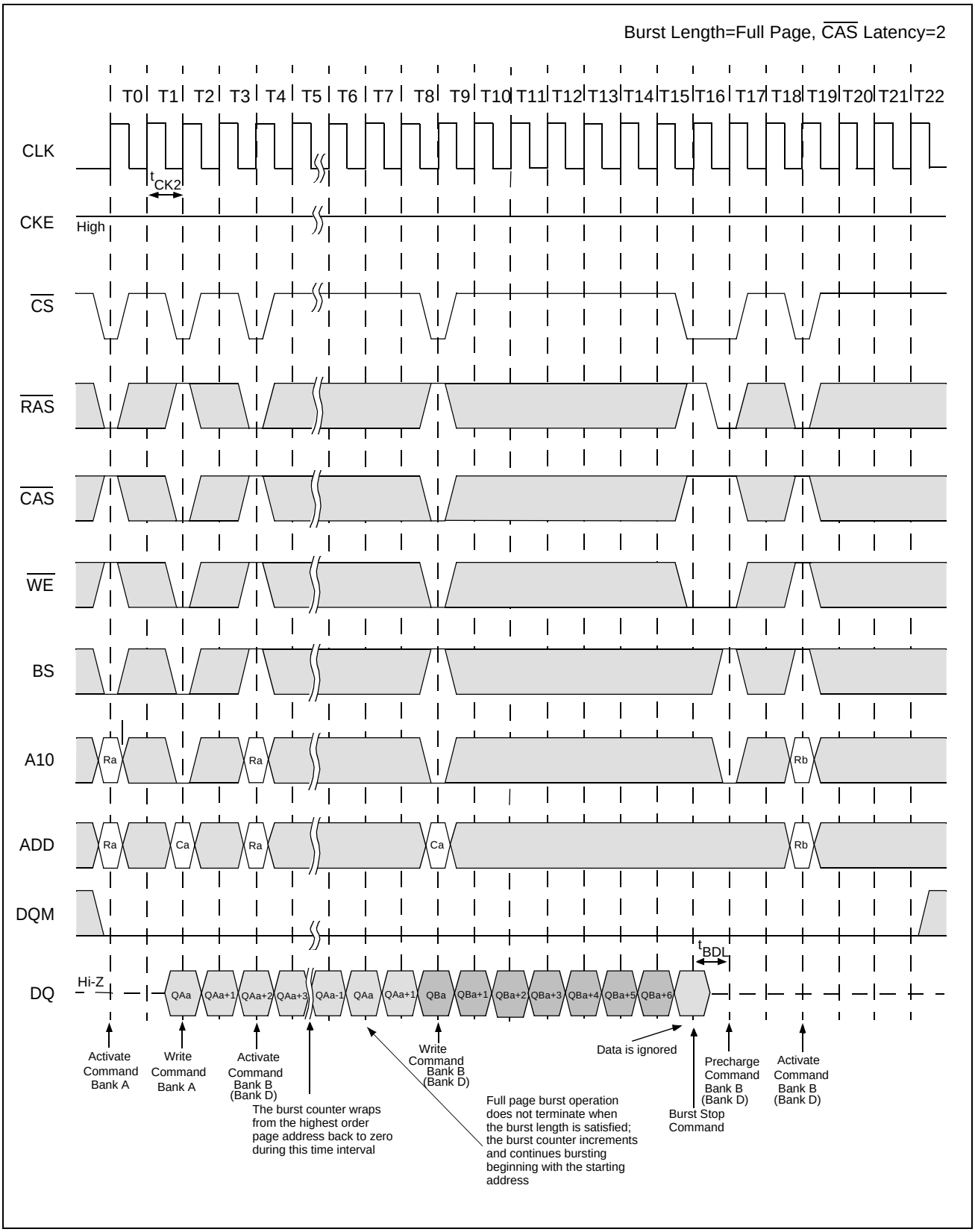
Full Page Read Cycle (1 of 2)



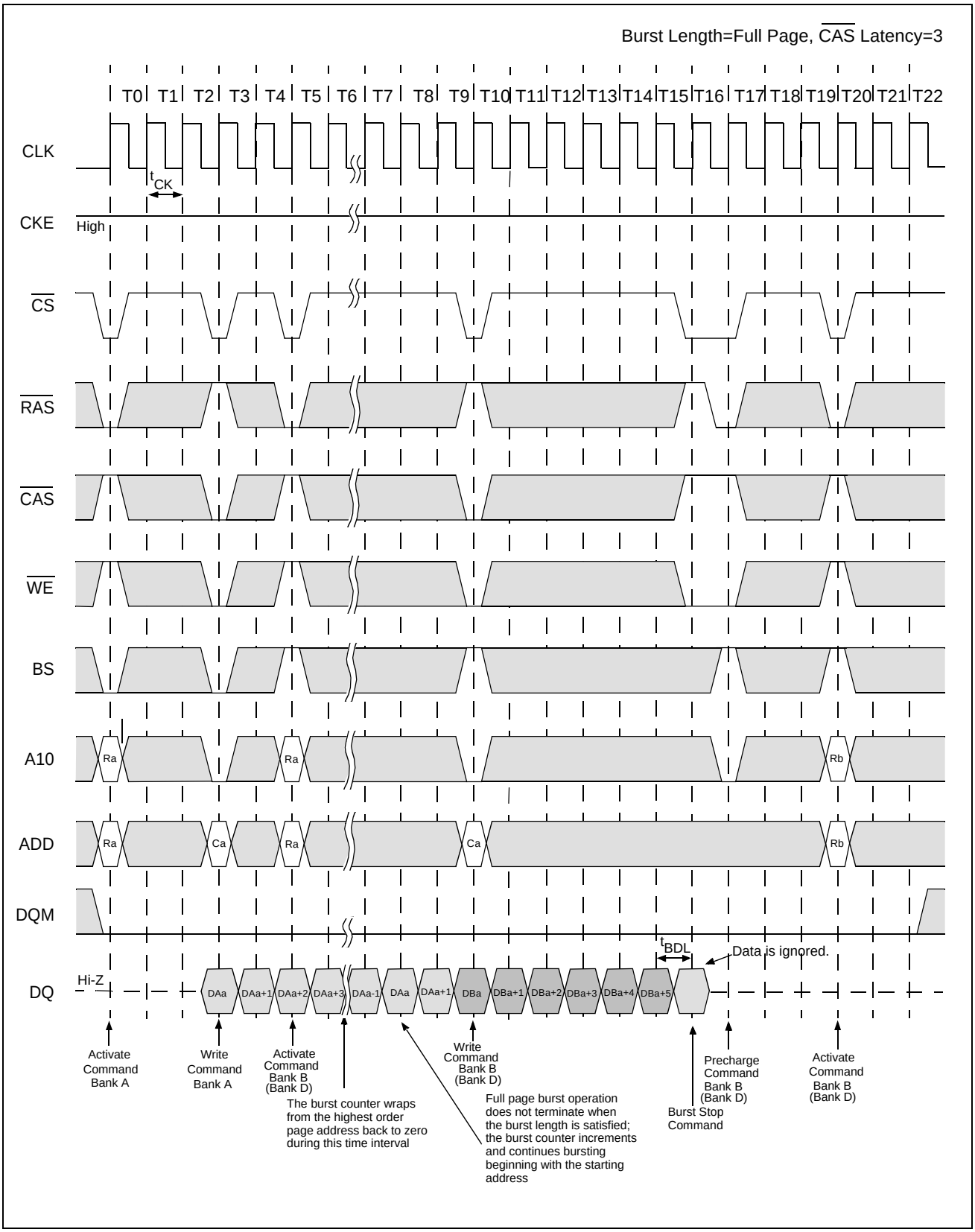
Full Page Read Cycle (2 of 2)



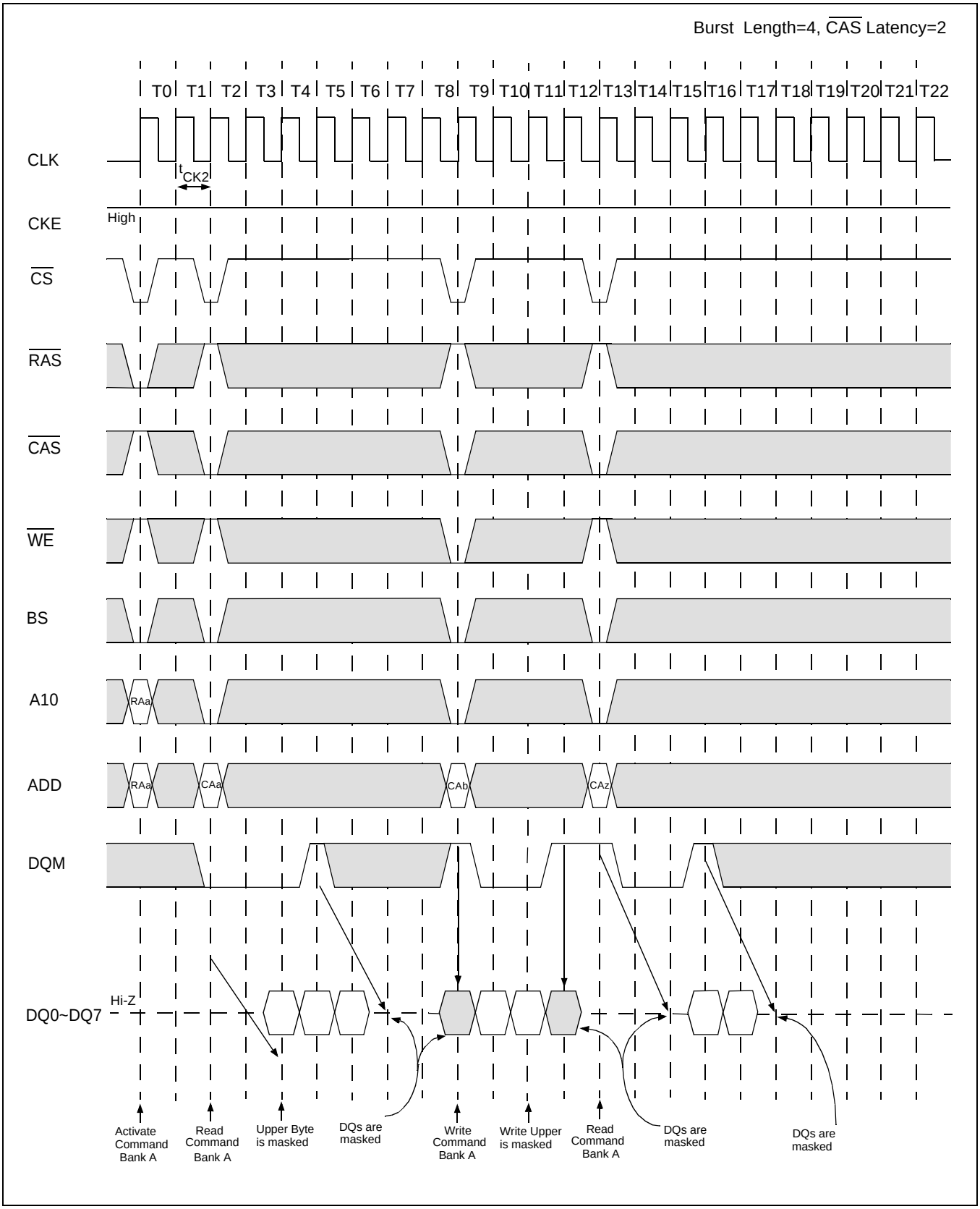
Full Page Write Cycle (1 of 2)



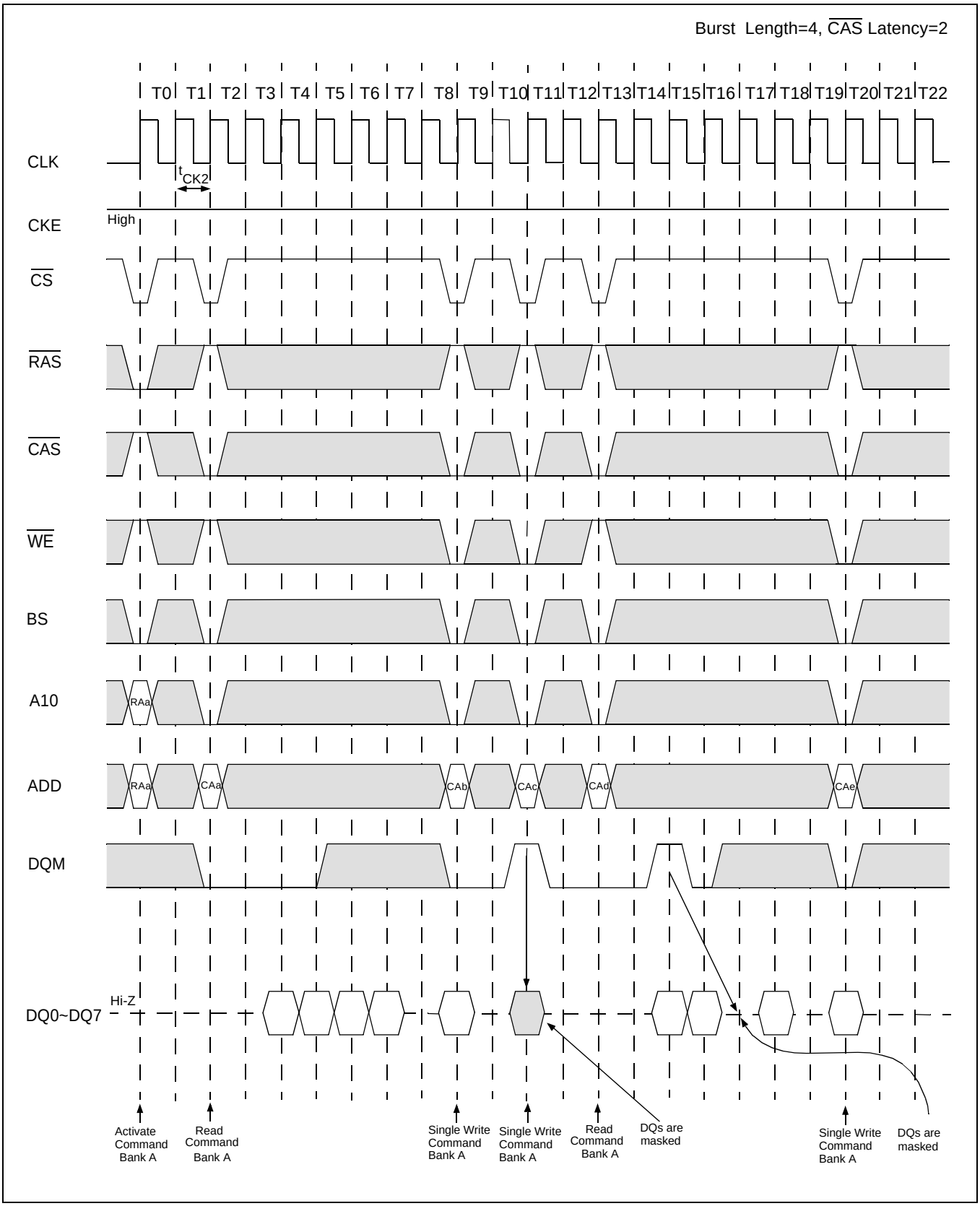
Full Page Write Cycle (2 of 2)



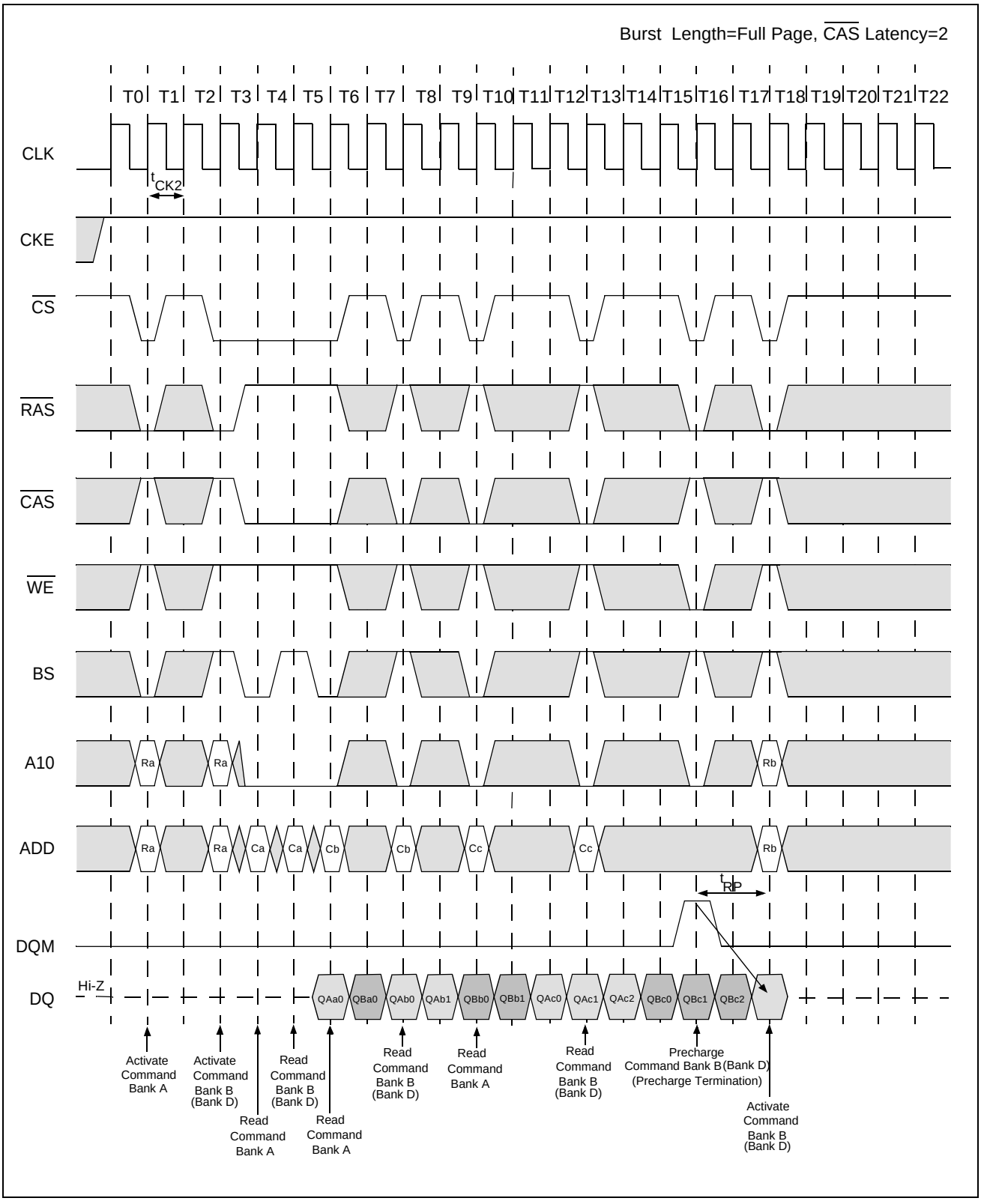
Byte Write Operation



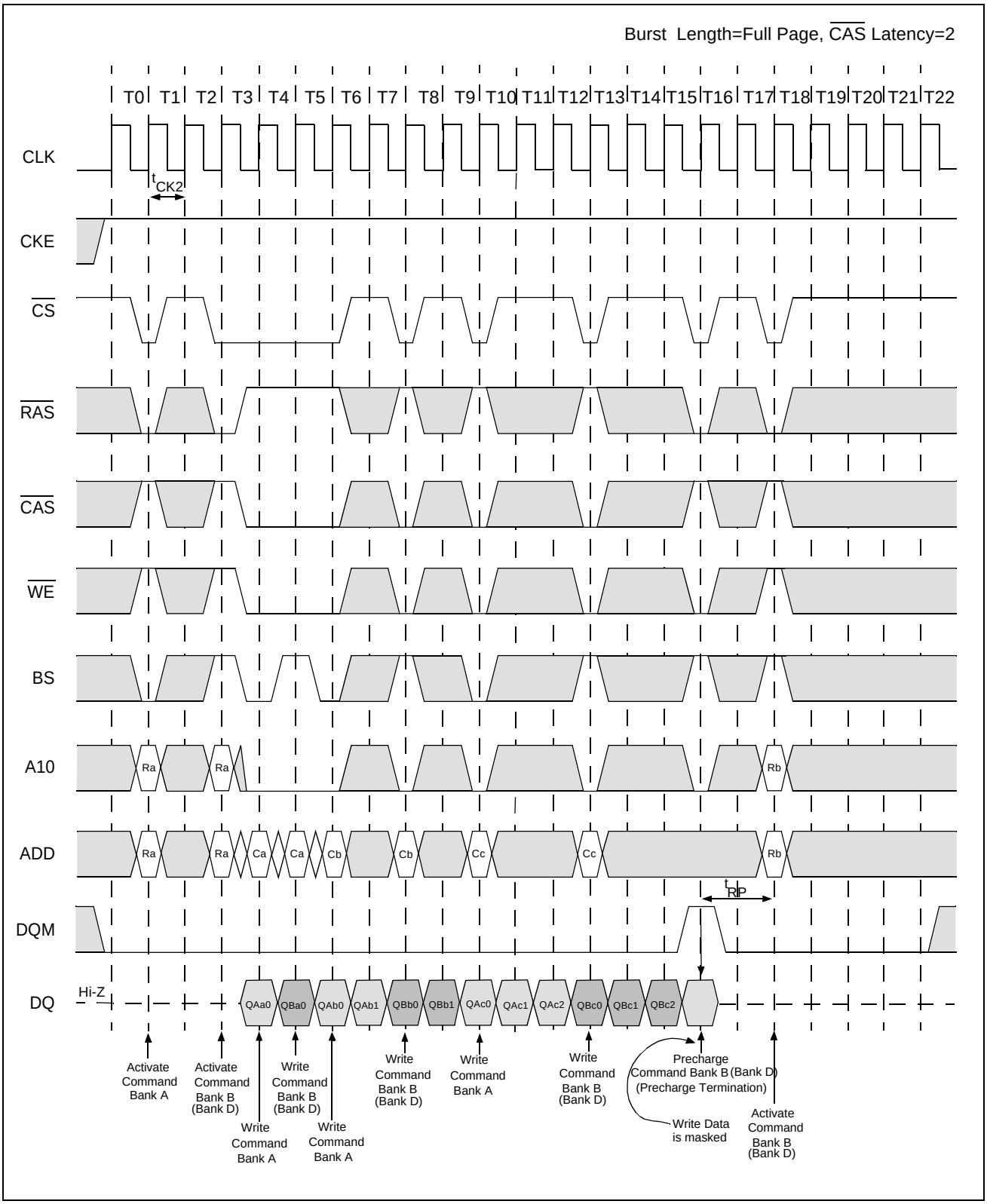
Burst Read and Single Write Operation



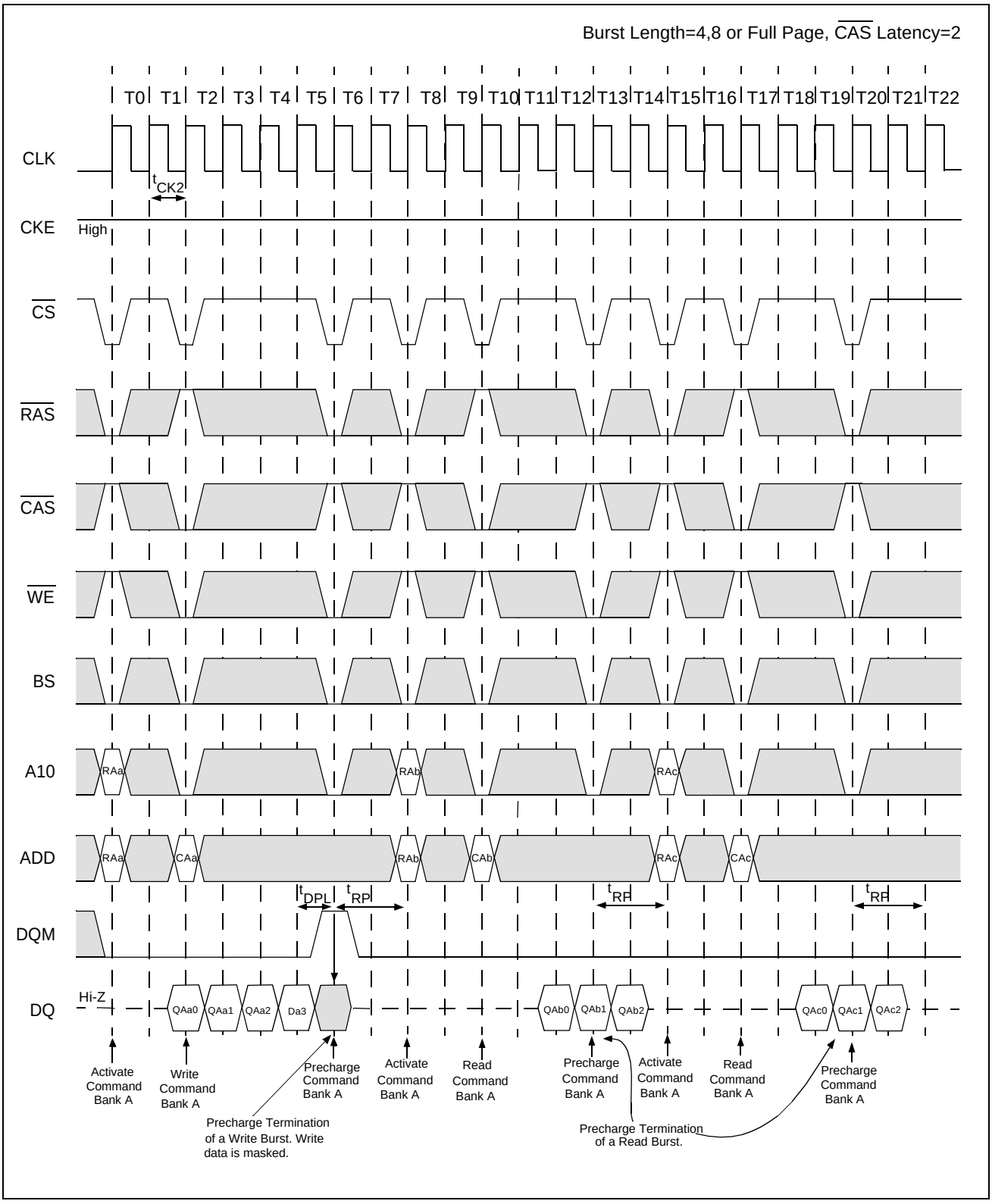
Full Page Random Column Read



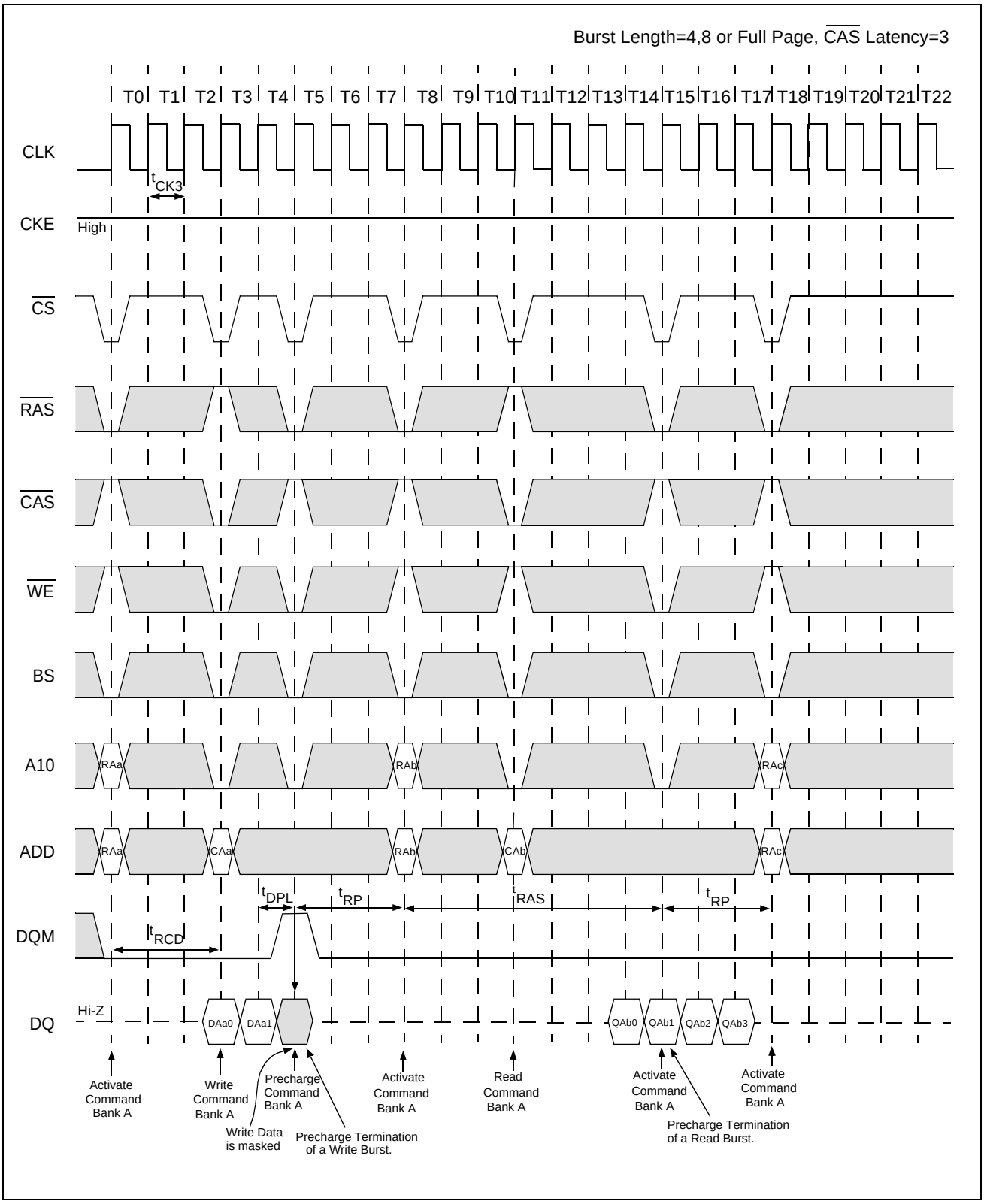
Full Page Random Column Write



Precharge Termination of a Burst (1 of 2)



Precharge Termination of a Burst (2 of 3)



Ordering information

Part Number	Cycle time	Package
VG36648041BT-7	7ns	400mil 54-Pin Plastic TSOP
VG36648041BT-8	8ns	
VG36648041BT-10	10ns	

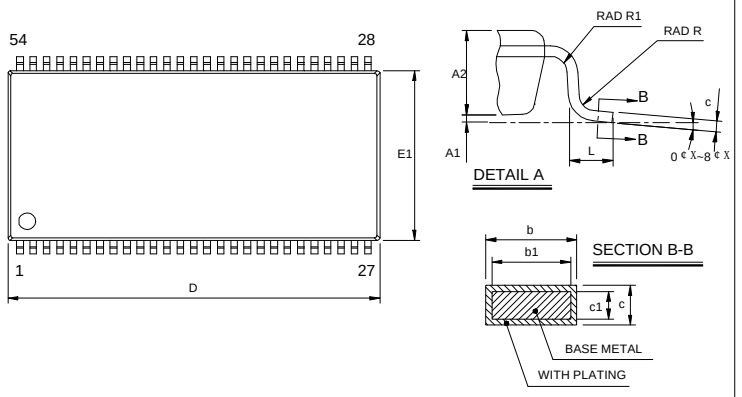
VG36648041BT-8

- VG → VIS Memory Product
- 36 → Technology/Design Rule
- 64 → 64Mb
- 80 → Device Configuration, 80: x8
- 4 → Device Infernal Banks
- 1 → Interface Type, 1: LVTTL
- B → Mask/Design Version
- T → Package Type, T: TSOP
- 8 → Cycle time, 10: 10ns, 8: 8ns, 7: 7ns

Packaging Information

•400mil, 54-Pin Plastic TSOP

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.20	---	---	0.047
A1	0.05	---	0.15	0.002	---	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	---	0.45	0.012	---	0.018
b1	0.30	---	0.40	0.012	---	0.016
c	0.12	---	0.21	0.005	---	0.008
c1	0.12	---	0.16	0.005	---	0.006
D	22.09	22.22	22.35	0.870	0.875	0.880
ZD	0.71 REF.			0.028 REF.		
e	0.80 BASIC			0.0315 BASIC		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
L	0.40	0.50	0.60	0.016	0.020	0.024
R	0.12	---	0.25	0.005	---	0.010
R1	0.12	---	---	0.005	---	---



NOTE:
1. CONTROLLING DIMENSION : MILLIMETERS
2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION.
   MOLD PROTRUSION SHALL NOT EXCEED 0.15mm(0.006") PER SIDE.
   DIMENSION E1 DOES NOT INCLUDE INTERLEAD PROTRUSION.
   INTERLEAD PROTRUSION SHALL NOT EXCEED 0.25mm(0.01") PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSIONS/INTRUSION.
   ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD TO BE WIDER THAN THE MAX b DIMENSION BY MORE THAN 0.13mm.
   DAMBAR INTRUSION SHALL NOT CAUSE THE LEAD TO BE NARROWER THAN THE MIN b DIMENSION BY MORE THAN 0.07mm.