CEL

NEC's 3 V DUAL DOWNCONVERTER AND PLL FREQUENCY SYNTHESIZER

UPB1007K

FEATURES

- **INTEGRATED RF BLOCK:** LNA, RF & IF Downconverter + PLL frequency synthesizer
- **STATE OF THE ART 25 GHz fT UHS0 BIPOLAR PROCESS**
- **DOUBLE-CONVERSION:** f_{1stIF} = 61.380 MHz, f_{2ndIF} = 4.092 MHz
- **ADJUSTABLE GAIN:** 20 dB range MIN
- **FIXED DIVISION PRESCALER**
- **LOW POWER CONSUMPTION:** 25 mA @ 3 V
- **SMALL 36 PIN QFN PACKAGE** Flat lead style for better performance
- **TAPE AND REEL PACKAGING AVAILABLE**

DESCRIPTION

NEC's UPB1007K is a Silicon RFIC designed for low cost GPS receivers. The IC combines an LNA, followed by a double-conversion RF/IF downconverter block and a PLL frequency synthesizer on one chip. The device operates on a 3V supply voltage and is housed in a small 36 pin QFN (Quad Flat No-lead) package, resulting in low power consumption and reduced board space. The device is manufactured using the state of the art UHS0 25 GHz fT silicon bipolar process.
NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

APPLICATIONS

- **LOW POWER HANDHELD GPS RECEIVER**
- **IN-VEHICLE NAVIGATION SYSTEMS**
- **PC/PDA+GPS INTEGRATION**

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.0 V, unless otherwise specified)

PART NUMBER PACKAGE OUTLINE			UPB1007K QFN-36		
SYMBOLS	**PARAMETERS AND CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
I_{CC}	Total Circuit Current, No Signals	mA		25	31
V_{CC}	Supply Voltage	V	2.7	3.0	3.3
LNA (f_{RFin} = 1575.42 MHz, Z_L = Z_S = 50 Ω)					
Z_{LNAin}	RF Input Impedance of LNA	Ω		28 - j38	
Z_{LNAop}	RF Output Impedance of LNA	Ω		85 - jx6	
P_{1dBLNA}	1 dB Compression, Input matched	dBm		-22	
PG_{LNA}	Power Gain LNA, Input matched, P_{RFin} = -60 dBm	dB	14	15	
NF_{LNA}	Noise Figure of LNA, Input matched	dB		2.8	3.2
Mixer (f_{RFin} = 1575.42 MHz, $f_{1stLOin}$ = 1636.80 MHz, P_{LO} = -10 dBm, f_{1stIF} = 61.38 MHz, Z_L = Z_S = 50 Ω)					
Z_{MIXin}	RF Input Impedance of Mixer	Ω		31 -j103	
P_{1dBMIX}	1 dB Compression (refer to input), Input matched	dBm		-25	
PCG_{MIX}	Power Conversion Gain	dB		21	
NF_{MIX}	Noise Figure of Mixer (SSB), Input matched	dB		9.5	10
A_{LO-IF}	LO Leakage to IF Pins, P_{LO} = -10 dBm	dBm		-40	
A_{LO-RF}	LO Leakage to RF Input Pins, P_{LO} = -10 dBm	dBm		-48	
Z_{MIXout}	RF Output Impedance of Mixer			+152 - j9	
PLL					
I_{CPOH}	PLL Charge Pump High Side Current @ V_{CPout} = V_{CC}/2	mA		1	
I_{CPOL}	PLL Charge Pump Low Side Current @ V_{CPout} = V_{CC}/2	mA		-1	
f_{PD}	Phase Comparison Frequency	MHz		8.184	
IF Downconverter Block ($f_{1stIFin}$ = 61.38 MHz, $f_{2ndLOin}$ = 65.472 MHz, f_{2ndIF} output = 4.092 MHz, Z_S = 2kΩ, Z_L = 2 kΩ)					
NF_{2ndMIX}	Noise Figure of 2nd IF Mixer (SSB), (Z_S = 50Ω)	dB		12	
GV_{2ndMIX}	Voltage Gain of 2nd Mixer/Amplifier, P_{1stIF} = -50 dBm	dB		47	
V_{GC}	Gain Control Voltage (Voltage at maximum gain)	V		0.5	
D_{GC}	Gain Control Range, P_{1stIF} = -50 dBm (Voltage at maximum gain)	dB	20		
$A_{2ndLO1stIF}$	2nd LO Isolation to 1st IF Input Pins, V_{AGC} = 0 V	dB		-70	
$A_{2ndLO2ndIF}$	2nd LO Isolation to 2nd IF Output Pins, V_{AGC} = 0 V	dB		-70	

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3 V, unless otherwise specified)

PART NUMBER PACKAGE OUTLINE			UPB1007K QFN-36		
SYMBOLS	**PARAMETERS AND CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
2nd IF Amplifier Block (f_{2ndIF} = 4.096 MHz, Z_S = 2kΩ, Z_L = 2 kΩ)					
GV_{LIM}	Voltage Gain of Limiter Amplifier, P_{IN} = -60 dBm	dB		48	
f_{BB}	Roll-off Frequency	MHz		110	
Reference Amplifier Block					
V_{REFin}	Reference Input Minimum Level	mVpp	400	400	
V_{REFout}	Reference Output Swing (open collector output), C_L = 2 pF//R_L = 10 kΩ	Vpp	1.1	1.2	1.3
Power Down Control Pins					
VIH	Digital Control Input High	V	1.83	1.86	2.15
VIL	Digital Control Input Low	V		0.5	0.6

ABSOLUTE MAXIMUM RATINGS[1,2] (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CC}	Supply Voltage	V	3.6
P_T	Total Power Dissipation[3]	mW	433
T_{OP}	Operating Temperature	°C	-40 to +85
T_{STG}	Storage Temperature	°C	-55 to +150

Notes:
1. Operation in excess of any one of these parameters may result in permanent damage.
2. More than two items must not be reached simultaneously.
3. T_A = +85°C, mounted on a 50 x 50 x 1.6 mm double-sided copper clad epoxy glass PWB.

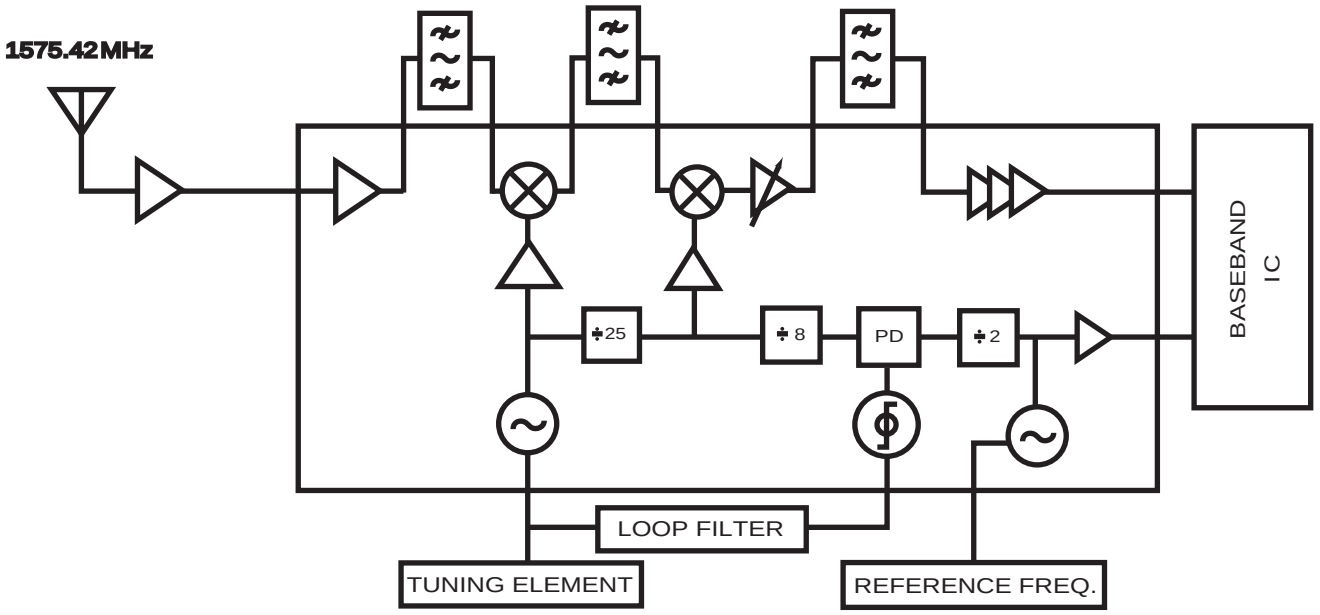
RECOMMENDED OPERATING CONDITIONS

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{CC}	Supply Voltage	V	2.7	3.0	3.3
T_{OP}	Operating Temperature	°C	-40	+25	+85
f_{RFin}	RF Input Frequency	MHz		1575.42	
f_{REFin} f_{REFout}	Reference Frequency	MHz		16.368	
f_{1stLO}	1st LO Oscillating Frequency	MHz		1636.8	
$f_{1stIFin}$	1st IF Input Frequency	MHz		61.38	
$f_{2ndLOin}$	2nd LO Input Frequency	MHz		65.472	
$f_{2ndIFin}$ $f_{2ndIFout}$	2nd IF Input/Output Frequency	MHz		4.092	
VIH	Power Down Control Voltage "High"	V	1.8		3
VIL	Power Down Control Voltage "Low"	V			0.6

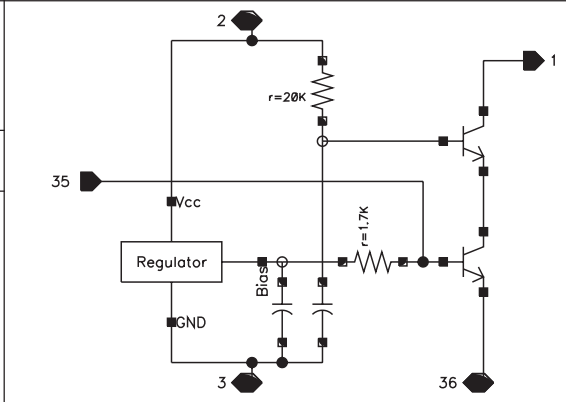
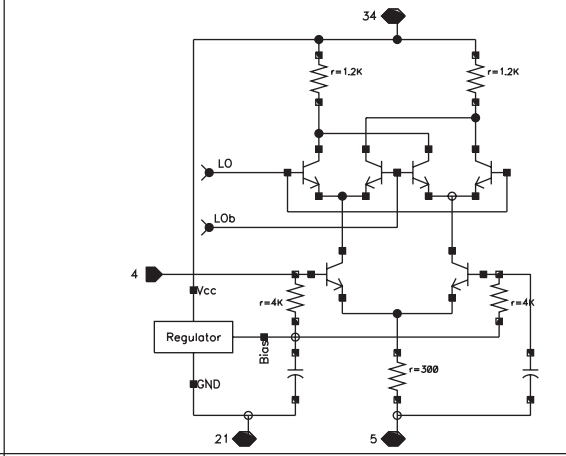
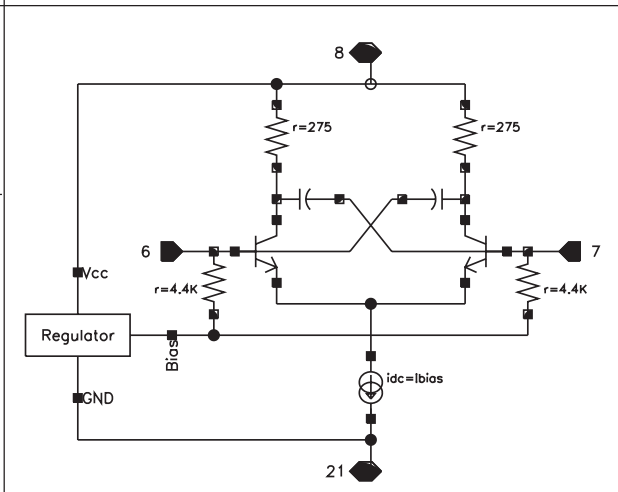
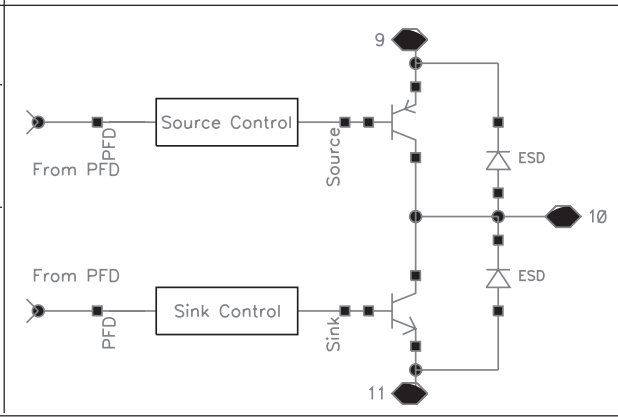
CURRENT BUDGET

SYMBOL	PARAMETER AND CONDITIONS	UNITS	MIN	TYP	MAX
IC Performance Parameters					
V_{CC}	Supply Voltage	V	2.7	3.0	3.3
I_{CC}	Total Circuit Current, V_{CC} = 3.0 V, no signal	mA		25	31
I_{CC_PL}	Power Down Node Current	mA		0.15	
I_{CC_XO}	Oscillator Supply Current, (Pin 15 = 0 V, Pin 16 = 3 V)	mA		2.7	
I_{CC_RX}	Receiver Supply Current, (Pin 15 = 0 V, Pin 16 = 3 V)	mA		22.3	
Functional Blocks Current Details					
I_{CC_LNA}	Supply Current of LNA, RF off	mA		2.6	
I_{CC_MIX1}	Supply Current of RF Mixer, RF off	mA		6.7	
I_{CC_MIX2}	Supply Current of IF Mixer, RF off	mA		3.5	
I_{CC_IFAMP}	Supply Current of IF Amplifier, RF off	mA		1.1	
I_{CC_XO}	Crystal Oscillator Supply Current	mA		2.7	
$I_{CC}9$	PLL Supply Current	mA		6.3	
I_{CC_CF}	Control Functions Supply Current	μA		2.1	
V_{IL}	Power Down Pin Logic LOW Level	V			0.6
V_{IH}	Power Down Pin Logic HIGH Level	V	1.8		
τ_{d_PON}	Power-on Response Time	ms		3	

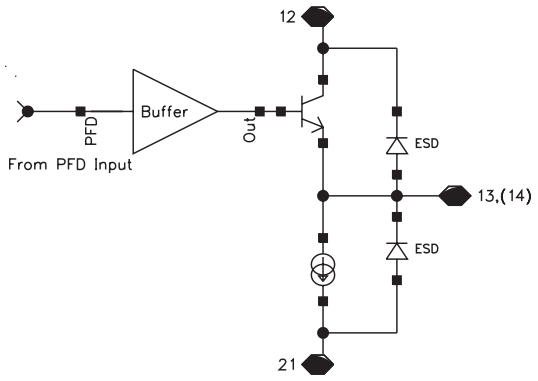
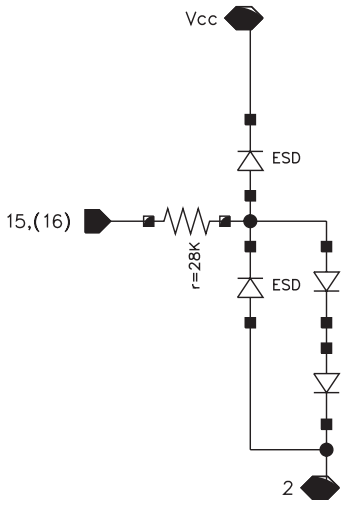
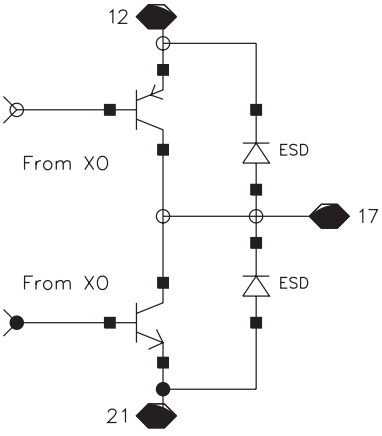
APPLICATION EXAMPLE



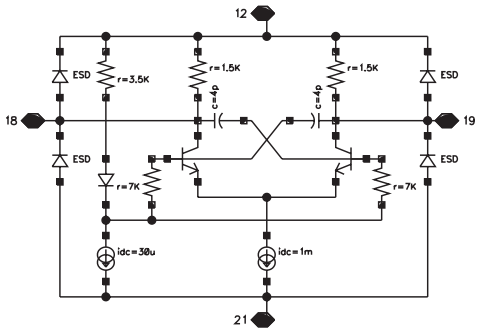
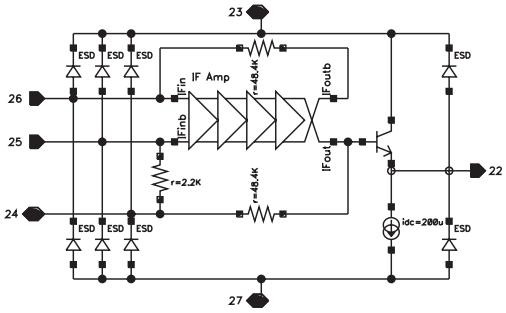
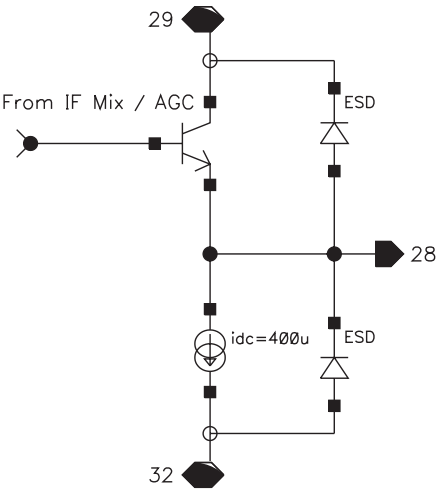
PIN FUNCTIONS

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
1	LNAout	Output pin of LNA. Output biasing and matching required as it is an open collector output.	
2	V_{CC} (V_{reg})	Supply voltage pin of regulator mixer block.	
3	GND (V_{reg})	Ground pin of regulator reference cell.	
4	RF MIXin	Input pin of RF mixer. 1575.42 MHz band pass filter can be inserted between pin 1 and mixer input.	
5	GND (MIX)	Ground pin of RF mixer cell.	
6	1stLO-OSC1	Pins 6 & 7 are base pins of the differential amplifier for 1st LO oscillator. These pins should be equipped with LC and varactor circuits to oscillate at 1636.8 MHz.	
7	1stLO-OSC2		
8	V_{CC} (1stLO-OSC)	Supply voltage pin of differential amplifier for 1st LO oscillator circuit (VCO).	
9	V_{CC} (Charge Pump)	Supply voltage pin of the phase detector charge pump.	
10	PD-out	This is a current mode charge pump output for connection to a passive RC loop filter for driving the external varactor diode of 1stLO-OSC.	
11	GND (Charge Pump)	Ground pin of phase detector charge pump.	

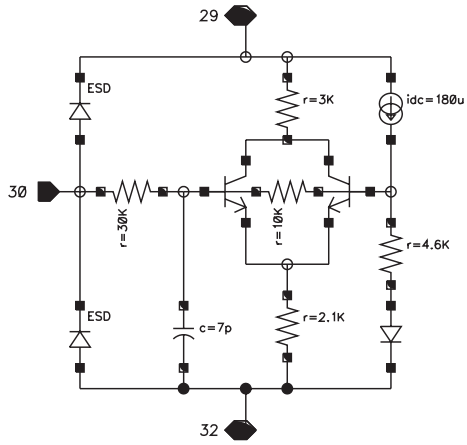
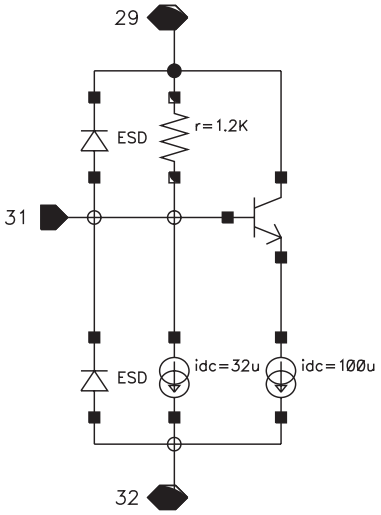
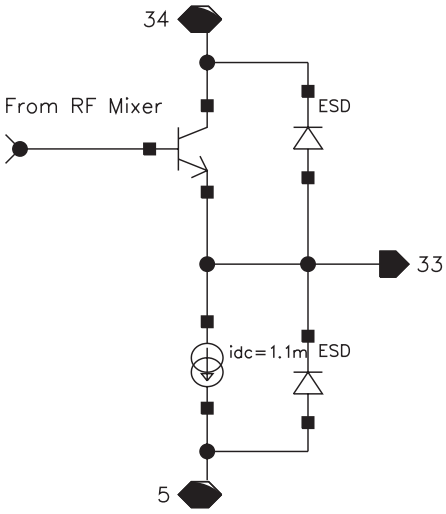
PIN FUNCTIONS

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
12	Vcc (Divider Block)	Supply voltage pin of prescaler, phase detector, crystal oscillator, VCO buffer.	
13	LO_out	Monitor pin of frequency at phase detector.	
14	XO_out	Monitor pin of oscillator ÷2 output at phase detector.	
15	PD1	Power down control pin Low = Whole chip off except XTAL osc. High = Whole chip on except XTAL osc.	
16	PD2	Reference block standby mode. Low = Reference block disabled. High = Reference block enabled.	
17	REFout	Output pin of reference frequency. The frequency from pin 17 can be taken out as 1Vp-p swing.	

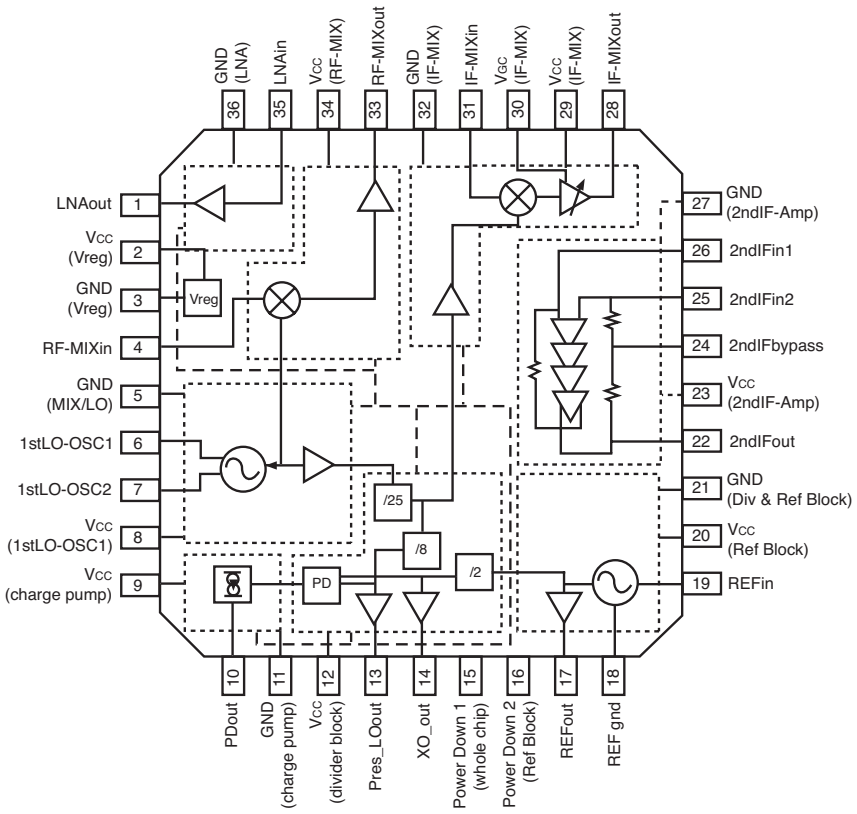
PIN FUNCTIONS

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
18	REF gnd	Differential oscillator input. This pin should be grounded via a capacitor.	
19	REF_{in}	Input pin of the reference frequency buffer. This pin should be equipped with an external 16.368 MHz oscillator (e.g. TCXO).	
20	V_{CC} (Ref Block)	Supply voltage pin of output charge pump of the oscillator.	
21	GND (Ref Block)	Ground pin of the oscillator, prescaler, phase detector and VCO.	
22	2nd IF_{out}	Output pin of 2nd IF amplifier. This pin output 4.092 MHz clipped sinewave. This pin should be equipped with external inverter to adjust level to next stage on user's system.	
23	V_{CC} 2ndIFAMP	Supply voltage pin of 2ndIF amplifier	
24	2ndIF bypass	Bypass pin of 2nd IF amplifier input. This pin should be grounded via a capacitor.	
25	2ndIFin1	Pin 1 of 2nd IF amplifier input . 2nd IF filter can be inserted between 25 & 28.	
26	2ndIFin2	Pin 2 of 2nd IF amplifier input. This pin should be grounded via a capacitor.	
27	GND (2ndIF AMP)	Ground pin of 2nd IF amplifier.	
28	IF MIXout	Output pin from IF mixer. IF mixer output signal goes through gain control amplifier before this emitter follower output port.	
29	V_{CC} (IF MIX)	Supply voltage pin of IF mixer, gain control amplifier.	

PIN FUNCTIONS

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
30	V_{GC} (IF MIX)	Gain control voltage pin of IF mixer output amplifier. This voltage performs forward control, i.e., (V_{GC} up→Gain down).	
31	IF-MIXin	Input pin of IF mixer and IF VAGC.	
32	GND (IF-MIX)	Ground pin of IF mixer and IF VAGC.	
33	RF-MIXout	Output pin of RF mixer . 1st IF filter must be inserted between pins 31 and 33.	
34	V_{CC} (RF-MIX)	Supply voltage pin of RF mixer block. This pin must be decoupled with capacitor (e.g. 1000 pF).	
35	LNAin	Input pin of low noise amplifier. Optimal input matching required for low noise performance.	See Pins 1-3
36	GND (LNA)	Ground pin of LNA.	

INTERNAL BLOCK DIAGRAM



ORDERING INFORMATION

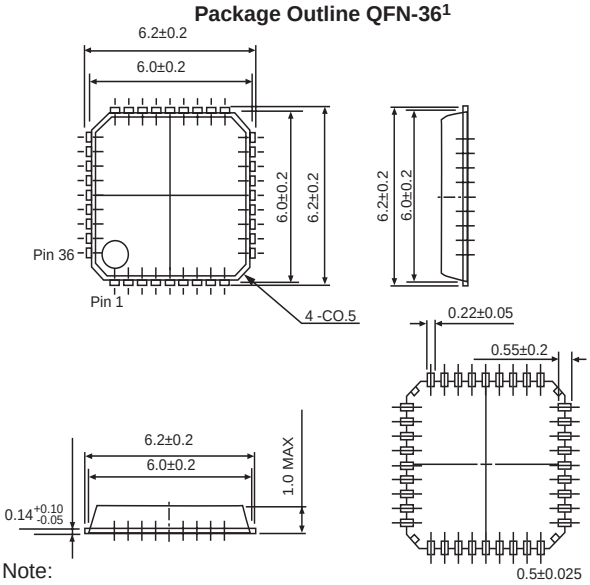
Part Number	Package
UPB1007K	36 Pin plastic QFN

ACTUAL SIZE (Units in mm)

Package Outline QFN-36

OUTLINE DIMENSIONS (Units in mm)

Package Outline QFN-36[1]



Note:
1. The solder pads on each corner should be grounded.