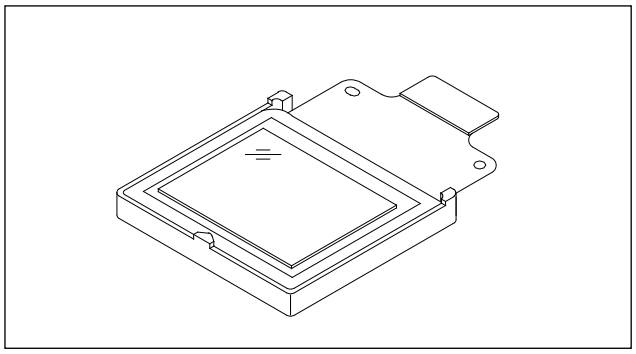
SONY

LCX009AK

1.8cm (0.7-inch) NTSC/PAL Color LCD Panel

Description

The LCX009AK is a 1.8cm diagonal active matrix TFT-LCD panel addressed by the polycrystalline silicon super thin film transistors with built-in peripheral driving circuit. This panel provides full-color representation in NTSC/PAL mode. RGB dots are arranged in a delta pattern featuring high picture quality of no fixed color patterns, which is inherent in vertical stripes and mosaic pattern arrangements.



Features

- The number of active dots: 180,000 (0.7-inch; 1.8cm in diagonal)
- Horizontal resolution: 400 TV lines
- High optical transmittance: 3.5% (typ.)
- High contrast ratio with normally white mode: 200 (typ.)
- Built-in H and V driving circuit (built-in input level conversion circuit, TTL drive possible)
- High quality picture representation with RGB delta arranged color filters
- Full-color representation
- NTSC/PAL compatible
- Right/left inverse display function

Element Structure

- Dots

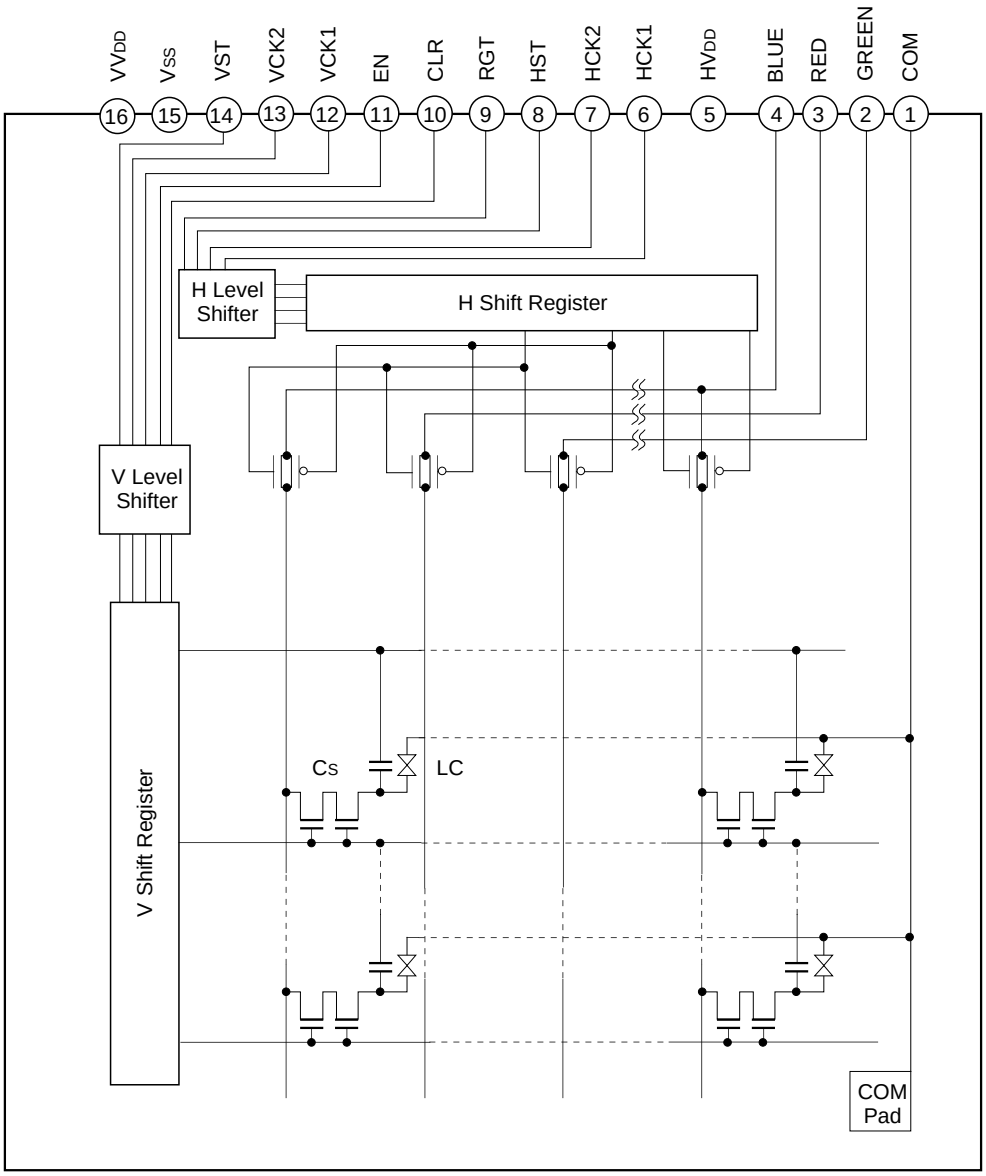
  Total dots : 827 (H) × 228 (V) = 188,556

  Active dots : 800 (H) × 225 (V) = 180,000

- Built-in peripheral driving circuit using the polycrystalline silicon super thin film transistors.

E94212C64-PS

Block Diagram



Absolute Maximum Ratings (Vss = 0V)

• H driver supply voltage	HV_{DD}	–1.0 to +17	V
• V driver supply voltage	VV_{DD}	–1.0 to +17	V
• H driver input pin voltage	HST, HCK1, HCK2 RGT	–1.0 to +17	V
• V driver input pin voltage	VST, VCK1, VCK2 CLR, EN	–1.0 to +17	V
• Video signal input pin voltage	GREEN, RED, BLUE	–1.0 to +15	V
• Operating temperature	Topr	–10 to +70	°C
• Storage temperature	Tstg	–30 to +85	°C

Operating Conditions (Vss = 0V)

Supply voltage

HV_{DD}	13.5 ± 0.5	V
VV_{DD}	13.5 ± 0.5	V

Input pulse voltage (Vp-p of all input pins except video signal input pins)

Vin	3.0V or more

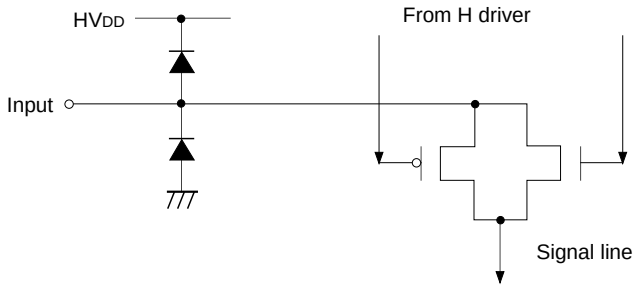
Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	COM	Common voltage of panel	9	RGT	Drive direction pulse for H shift register (H: normal, L: reverse)
2	GREEN	Video signal (G) to panel	10	CLR	Improvement pulse for uniformity
3	RED	Video signal (R) to panel	11	EN	Enable pulse for gate selection
4	BLUE	Video signal (B) to panel	12	VCK1	Clock pulse for V shift register drive
5	HV_{DD}	Power supply for H driver	13	VCK2	Clock pulse for V shift register drive
6	HCK1	Clock pulse for H shift register drive	14	VST	Start pulse for V shift register drive
7	HCK2	Clock pulse for H shift register drive	15	Vss	GND (H, V drivers)
8	HST	Start pulse for H shift register drive	16	VV_{DD}	Power supply for V driver

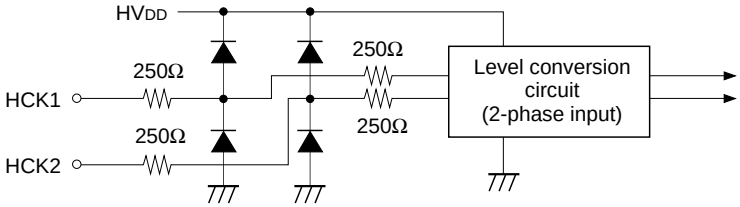
Input Equivalent Circuit

To prevent static charges, protective diodes are provided for each pin except the power supply. In addition, protective resistors are added to all pins except video signal input. The equivalent circuit of each input pin is shown below. (The resistor value: typ.)

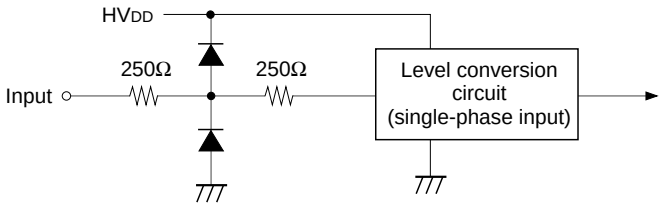
(1) Video signal input



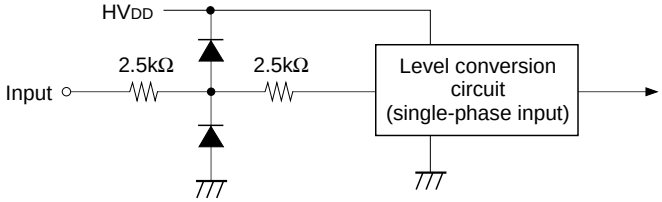
(2) HCK1, HCK2



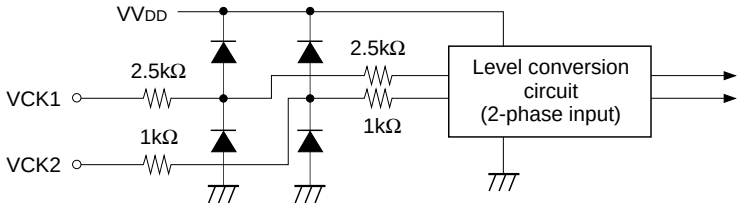
(3) HST



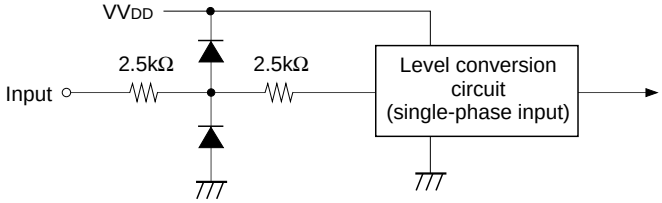
(4) RGT



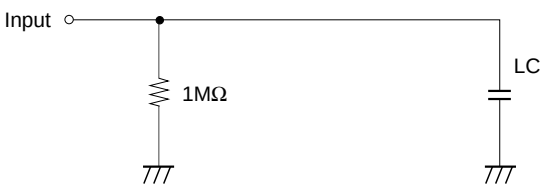
(5) VCK1, VCK2



(6) VST, CLR, EN



(7) COM



Level Conversion Circuit

The LCX009AK has a built-in level conversion circuit in the clock input unit located inside the panel. The circuit voltage is stepped up to 13.5V. This level conversion circuit meets the specifications of a 3.0V to 5.0V power supply of the externally-driven IC mainly. However, this circuit can operate even with a 12V power supply of the IC.

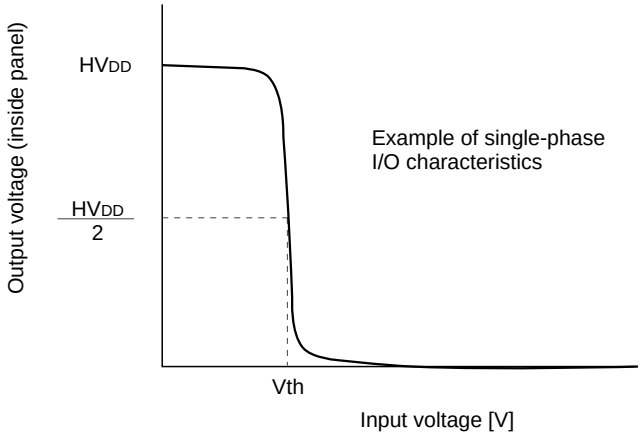
1. I/O characteristics of level conversion circuit

(For a single-phase input unit)

An example of the I/O voltage characteristics of a level conversion circuit is shown in the figure to the right. The input voltage value that becomes half the output voltage (after voltage conversion) is defined as Vth.

The Vth value varies depending on the HV_{DD} and VV_{DD} voltages.

The Vth values under standard conditions are indicated in the table below. (HST, VST, EN, CLR, and RGT in the case of a single-phase input)

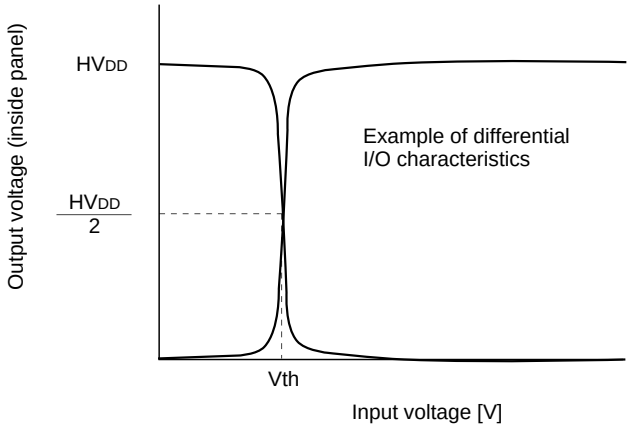


$HV_{DD} = VV_{DD} = 13.5V$

Item	Symbol	Min.	Typ.	Max.	Unit
Vth voltage of circuit	Vth	0.35	1.50	2.70	V

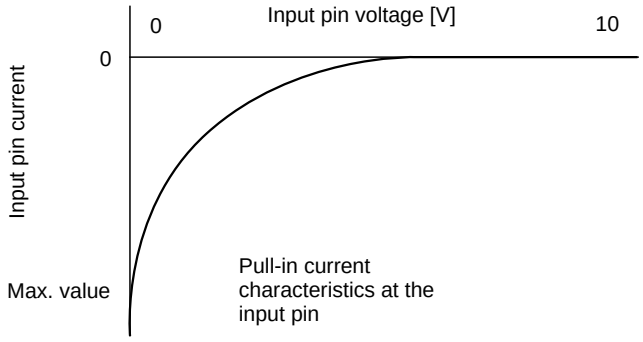
(For a differential input unit)

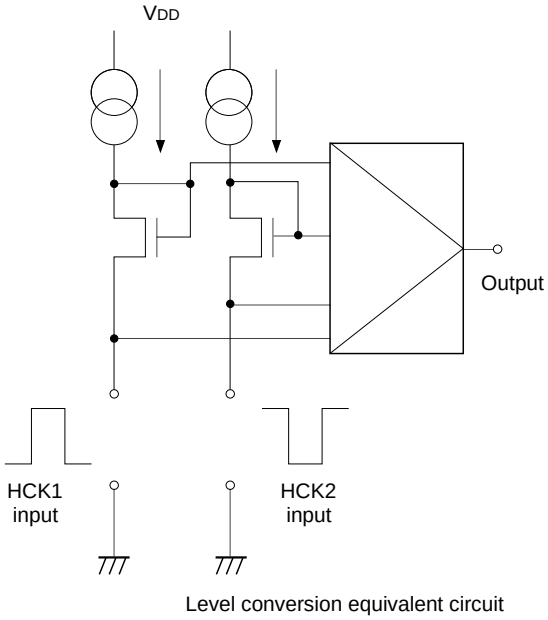
An example of I/O voltage characteristics of a level conversion circuit for a differential input is shown in the figure to the right. Although the characteristics, including those of the Vth voltage, are basically the same as those for a single-phased input, the two-phased input phase is defined. (Refer to clock timing conditions.)



2. Current characteristics at the input pin of level conversion circuit

A slight pull-in current is generated at the input pin of the level conversion circuit. (The equivalent circuit diagram is shown to the right.) The current volume increases as the voltage at the input pin decreases, and is maximized when the pin is grounded.) (Electrical characteristics are defined by the grounded input.)





Level conversion equivalent circuit

Input Signals

1. Input signal voltage conditions (Vss = 0V)

Item		Symbol	Min.	Typ.	Max.	Unit
H driver input voltage	(Low)	VHIL	–0.3	0.0	0.3	V
	(High)	VHIH	3.0	5.0	5.5	V
V driver input voltage	(Low)	VVIL	–0.3	0.0	0.3	V
	(High)	VVIH	3.0	5.0	5.5	V
Video signal center voltage		VVC	5.8	6.0	6.2	V
Video signal input range*1		Vsig	VVC – 4.5		VVC + 4.5	V
Common voltage of panel		Vcom	VVC – 0.55	VVC – 0.40	VVC – 0.25	V

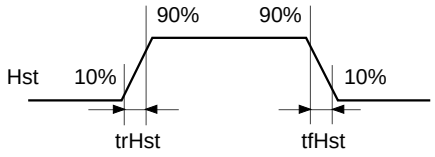
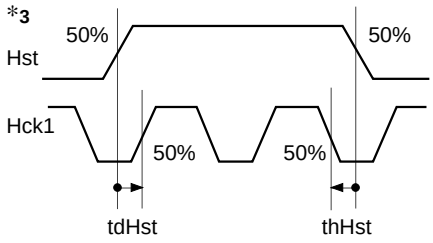
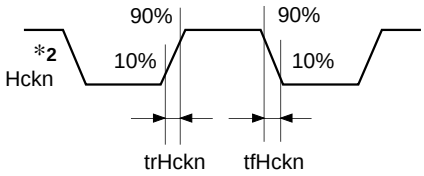
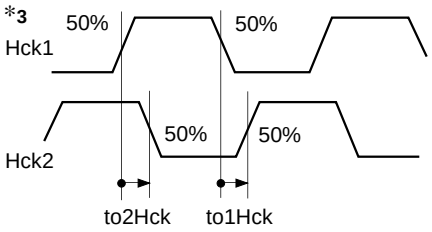
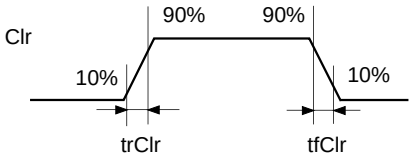
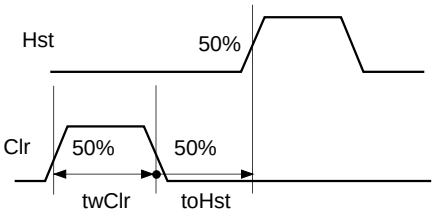
*1 Video input signal should be symmetrical to VVC.

2. Clock timing conditions (Ta = 25°C)

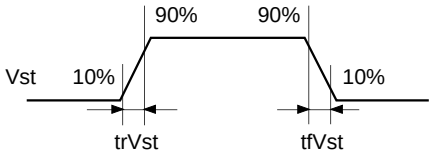
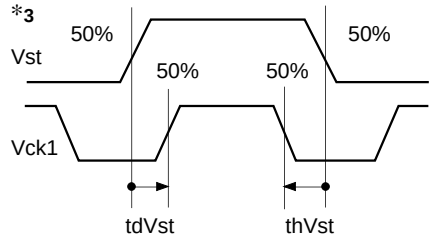
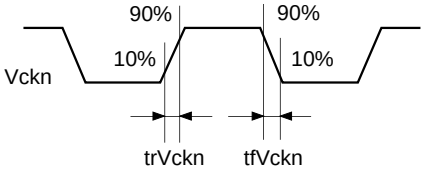
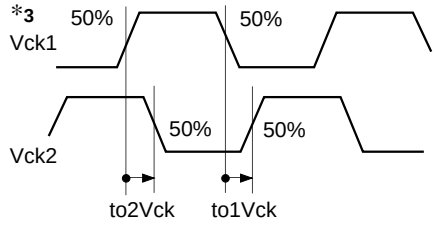
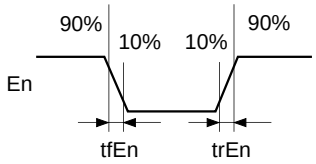
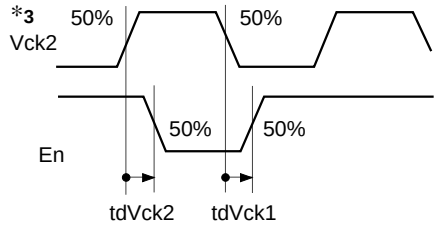
	Item	Symbol	Min.	Typ.	Max.	Unit
HST	Hst rise time	trHst			30	ns
	Hst fall time	tfHst			30	
	Hst data set-up time	tdHst	–100	60	100	
	Hst data hold time	thHst	–200	–120	–50	
HCK	Hckn*2 rise time	trHckn			30	
	Hckn*2 fall time	tfHckn			30	
	Hck1 fall to Hck2 rise time	to1Hck	–15	0	15	
	Hck1 rise to Hck2 fall time	to2Hck	–15	0	15	
CLR	Clr rise time	trClr			100	
	Clr fall time	tfClr			100	
	Clr pulse width	twClr	3400	3500	3600	
	Clr fall to Hst rise time	toHst	1850	1950	2050	
VST	Vst rise time	trVst			100	
	Vst fall time	tfVst			100	
	Vst data set-up time	tdVst	–50	32	50	µs
	Vst data hold time	thVst	–50	–32	–20	
VCK	Vckn*2 rise time	trVckn			100	ns
	Vckn*2 fall time	tfVckn			100	
	Vck1 fall to Vck2 rise time	to1Vck	–20	0	20	
	Vck1 rise to Vck2 fall time	to2Vck	–20	0	20	
EN	En rise time	trEn			100	
	En fall time	tfEn			100	
	Vck2 rise to En fall time	tdVck2	–20	0	20	
	Vck1 rise to En rise time	tdVck1	–20	0	20	

*2 Hckn and Vckn mean Hck1, Hck2 and Vck1, Vck2. (fHckn = 2.75MHz, fVckn = 7.81kHz)

<Horizontal Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
HST	Hst rise time	trHst		○ Hckn*2 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hst fall time	tfHst		
	Hst data set-up time	tdHst		○ Hckn*2 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hst data hold time	thHst		
HCK	Hckn*2 rise time	trHckn		○ Hckn*2 duty cycle 50% to1Hck = 0ns to2Hck = 0ns tdHst = 60ns thHst = –120ns
	Hckn*2 fall time	tfHckn		
	Hck1 fall to Hck2 rise time	to1Hck		○ tdHst = 60ns thHst = –120ns
	Hck1 rise to Hck2 fall time	to2Hck		
CLR	Clr rise time	trClr		○ Hckn*2 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Clr fall time	tfClr		
	Clr pulse width	twClr		○ Hckn*2 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Clr fall to Hst rise time	toHst		

<Vertical Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
VST	Vst rise time	trVst		○ Vckn*2 duty cycle 50% to1Vck = 0ns to2Vck = 0ns
	Vst fall time	tfVst		
	Vst data set-up time	tdVst		○ Vckn*2 duty cycle 50% to1Vck = 0ns to2Vck = 0ns
	Vst data hold time	thVst		
VCK	Vckn*2 rise time	trVckn		○ Vckn*2 duty cycle 50% to1Vck = 0ns to2Vck = 0ns tdVst = 32µs thVst = –32µs
	Vckn*2 fall time	tfVckn		
	Vck1 fall to Vck2 rise time	to1Vck		○ tdVst = 32µs thVst = –32µs
	Vck1 rise to Vck2 fall time	to2Vck		
EN	En rise time	trEn		○ Vckn*2 duty cycle 50% to1Vck = 0ns to2Vck = 0ns
	En fall time	tfEn		
	Vck2 rise to En fall time	tdVck2		○ Vckn*2 duty cycle 50% to1Vck = 0ns to2Vck = 0ns
	Vck1 rise to En rise time	tdVck1		

*3 Definitions: The right-pointing arrow (•►) means +.
The left-pointing arrow (◄•) means –.
The black dot at an arrow (•) indicates the start of measurement.

Electrical Characteristics (Ta = 25°C, HV_{DD} = 13.5V, VV_{DD} = 13.5V)

1. Horizontal drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Input pin capacitance	Hckn	CHckn		5	10	pF	
	Hst	CHst		5	10	pF	
Input pin current	Hck1	IHck1	–200	–60		µA	Hck1 = GND
	Hck2	IHck2	–500	–260		µA	Hck2 = GND
	Hst	IHst	–300	–100		µA	Hst = GND
	Rgt	IRgt	–100	–15		µA	Rgt = GND
Video signal input pin capacitance		Csig		45	60	pF	
Current consumption		IH		3	4	mA	Hckn: Hck1, Hck2 (2.75MHz)

2. Vertical drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Input pin capacitance	Vckn	CVckn		5	10	pF	
	Vst	CVst		5	10	pF	
Input pin current	Vck1	IVck1	–100	–30		µA	Vck1 = GND
	Vck2	IVck2	–400	–200		µA	Vck2 = GND
	Vst En Clr	IVst, IEn, IClr	–100	–15		µA	Vst, En, Clr=GND
Current consumption		IV		400	1000	µA	Vckn: Vck1, Vck2 (7.87kHz)

3. Total power consumption of the panel

Item	Symbol	Min.	Typ.	Max.	Unit
Total power consumption of the panel (NTSC)	PWR		45	70	mW

4. COM input resistance

Item	Symbol	Min.	Typ.	Max.	Unit
COM – Vss input resistance	Rcom	0.5	1		MΩ

Electro-optical Characteristics (Ta = 25°C, NTSC mode)

Item			Symbol	Measurement method	Min.	Typ.	Max.	Unit
Contrast ratio		25°C	CR_{25}	1	80	200	—	—
		60°C	CR_{60}		80	200	—	
Optical transmittance			T	2	2.7	3.5	—	%
Chromaticity	R	X	Rx	3	0.560	0.630	0.670	CIE standards
		Y	Ry		0.300	0.345	0.390	
	G	X	Gx		0.275	0.310	0.347	
		Y	Gy		0.541	0.595	0.650	
	B	X	Bx		0.120	0.148	0.187	
		Y	By		0.040	0.088	0.122	
V – T characteristics	V_{90}	25°C	$V_{90\text{-}25}$	4	1.1	1.6	2.2	V
		60°C	$V_{90\text{-}60}$		1.0	1.3	2.1	
	V_{50}	25°C	$V_{50\text{-}25}$		1.5	2.0	2.5	
		60°C	$V_{50\text{-}60}$		1.4	1.8	2.4	
	V_{10}	25°C	$V_{10\text{-}25}$		2.2	2.7	3.2	
		60°C	$V_{10\text{-}60}$		2.1	2.5	3.1	
Half tone color reproduction range		R vs. G	V_{50RG}	5	—	–0.10	–0.25	V
		B vs. G	V_{50BG}		—	0.10	0.45	
Response time	ON time	0°C	ton0	6	—	25	100	ms
		25°C	ton25		—	8	40	
	OFF time	0°C	toff0		—	65	150	
		25°C	toff25		—	20	60	
Flicker		60°C	F	7	—	—	–40	dB
Image retention time		60min.	YT60	8	—	—	20	s
Optimum Vcom voltage			Vcomopt	9	5.45	5.60	5.75	V

<Electro-optical Characteristics Measurement>

Basic measurement conditions

(1) Driving voltage

HV_{DD} = 13.5V, VV_{DD} = 13.5V

VVC = 6.0V, Vcom = 5.6V

(2) Measurement temperature

25°C unless otherwise specified.

(3) Measurement point

One point in the center of screen unless otherwise specified.

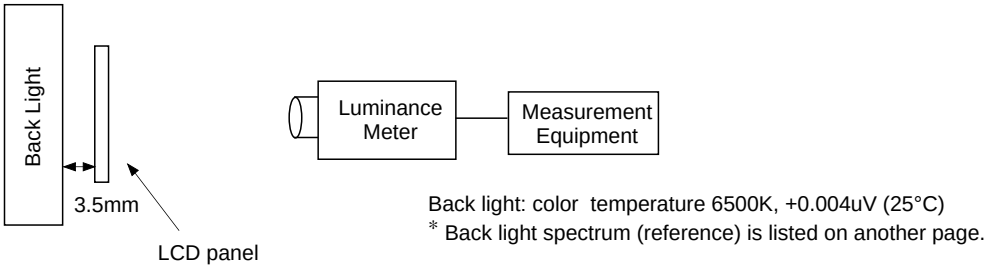
(4) Measurement systems

Two types of measurement system are used as shown below.

(5) RGB input signal voltage (Vsig)

Vsig = 6 ± V_{AC} (V) (V_{AC}: signal amplitude)

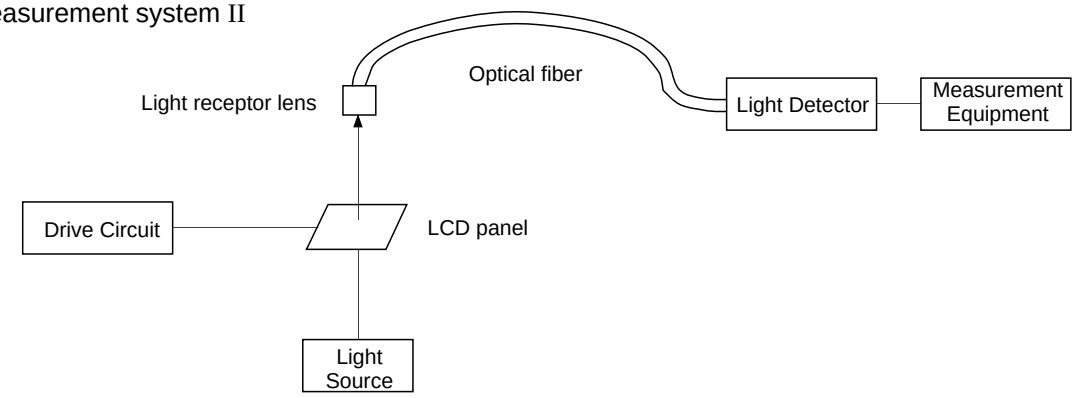
* Measurement system I



Back light: color temperature 6500K, +0.004uV (25°C)

* Back light spectrum (reference) is listed on another page.

* Measurement system II



1. Contrast Ratio

Contrast Ratio (CR) is given by the following formula (1).

$$CR = \frac{L\ (White)}{L\ (Black)} \quad \ldots (1)$$

L (White): Surface luminance of the TFT-LCD panel at the RGB signal amplitude V_{AC} = 0.5V.

L (Black): Surface luminance of the panel at V_{AC} = 4.5V

Both luminosities are measured by System I.

2. Optical Transmittance

Optical Transmittance (T) is given by the following formula (2).

$$T = \frac{L\ (White)}{Luminance\ of\ Back\ Light} \times 100\ (\%) \quad ... (2)$$

L (White) is the same expression as defined in the 'Contrast Ratio' section.

3. Chromaticity

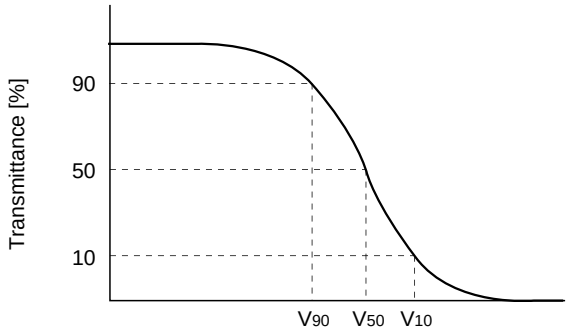
Chromaticity of the panels are measured by System I. Raster modes of each color are defined by the representations at the input signal amplitude conditions shown in the table below. System I uses Chromaticity of x and y on the CIE standards here.

		Signal amplitudes (V_{AC}) supplied to each input		
		R input	G input	B input
Raster	R	0.5	4.5	4.5
	G	4.5	0.5	4.5
	B	4.5	4.5	0.5

(Unit: V)

4. V – T Characteristics

V – T characteristics, the relationship between signal amplitude and the transmittance of the panels, are measured by System II. V90, V50 and V10 correspond to the each voltage which defines 90%, 50% and 10% of transmittance respectively.

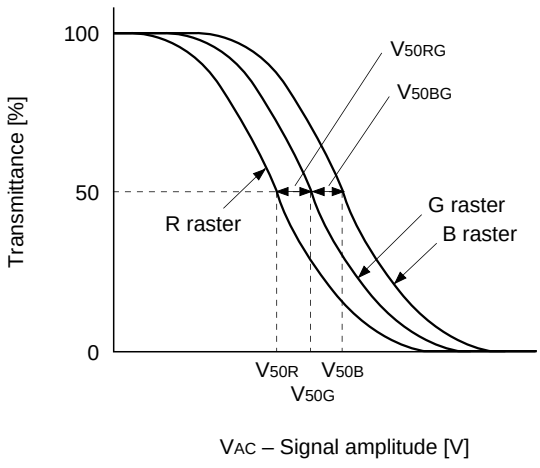


5. Half Tone Color Reproduction Range

Half tone color reproduction range of the LCD panels is characterized by the differences between the V – T characteristics of R, G and B. The differences of these V – T characteristics are measured by System II. System II defines signal voltages of each R, G, B raster modes which correspond to 50% of transmittance, V_{50R}, V_{50G} and V_{50B} respectively. V_{50RG} and V_{50BG}, the voltage differences between V_{50R} and V_{50G}, V_{50B} and V_{50G}, are simply given by the following formula (3) and (4) respectively.

$V_{50RG} = V_{50R} – V_{50G}$ ... (3)

$V_{50BG} = V_{50B} – V_{50G}$ ... (4)



6. Response Time

Response time t_{on} and t_{off} are defined by the formula (5) and (6) respectively.

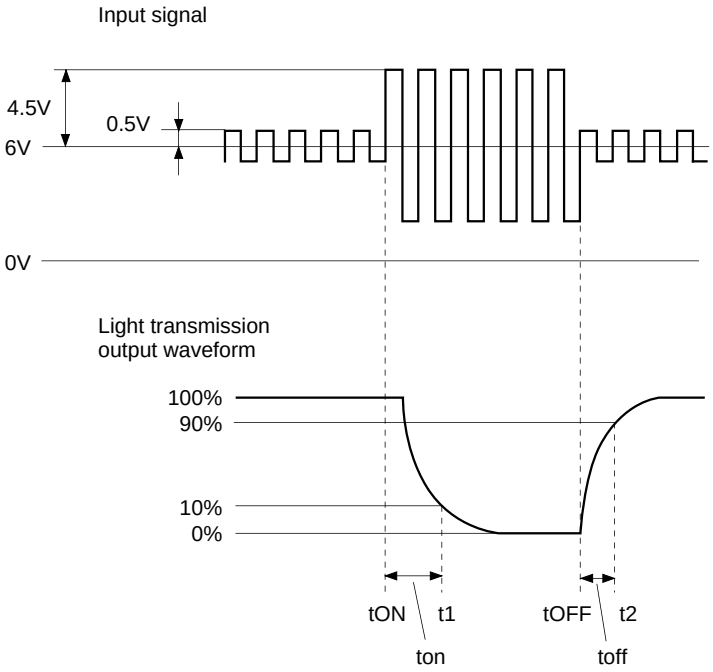
$t_{on} = t1 - tON$ ... (5)

$t_{off} = t2 - tOFF$ ... (6)

t1: time which gives 10% transmittance of the panel.

t2: time which gives 90% transmittance of the panel.

The relationships between t1, t2, tON and tOFF are shown in the right figure.



7. Flicker

Flicker (F) is given by the formula (7). DC and AC (NTSC: 30Hz, rms, PAL: 25Hz, rms) components of the panel output signal for gray raster* mode are measured by a DC voltmeter and a spectrum analyzer in System II.

$$F\ (dB) = 20\log\left\{\frac{\text{AC component}}{\text{DC component}}\right\} \quad \text{... (7)}$$

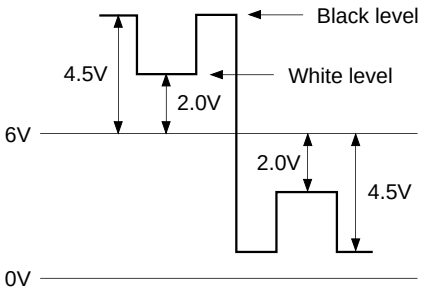
* R, G, B input signal condition for gray raster mode is given by
Vsig = 6 ± V_{50} (V)
where: V_{50} is the signal amplitude which gives 50% of transmittance in V – T curve.

8. Image Retention Time

Image retention time is given by the following procedures:

Apply monoscope signal to the LCD panel for 60 minutes and then change monoscope signal* to gray scale signal (Vsig = 6 ± V_{AC} (V); V_{AC} = 3 to 4V) so as to give the maximum image retention. Hold input signal V_{AC}. The time of the residual image to disappear gives the image retention time.

* Monoscope signal conditions:
Vsig = 6 ± 4.5 or 6 ± 2.0 (V)
(shown in the right figure)
Vcom = 5.6V



Vsig waveform

9. Method of Measuring the Optimum Vcom

There are two methods of measuring the optimum Vcom using the photoelectric element.

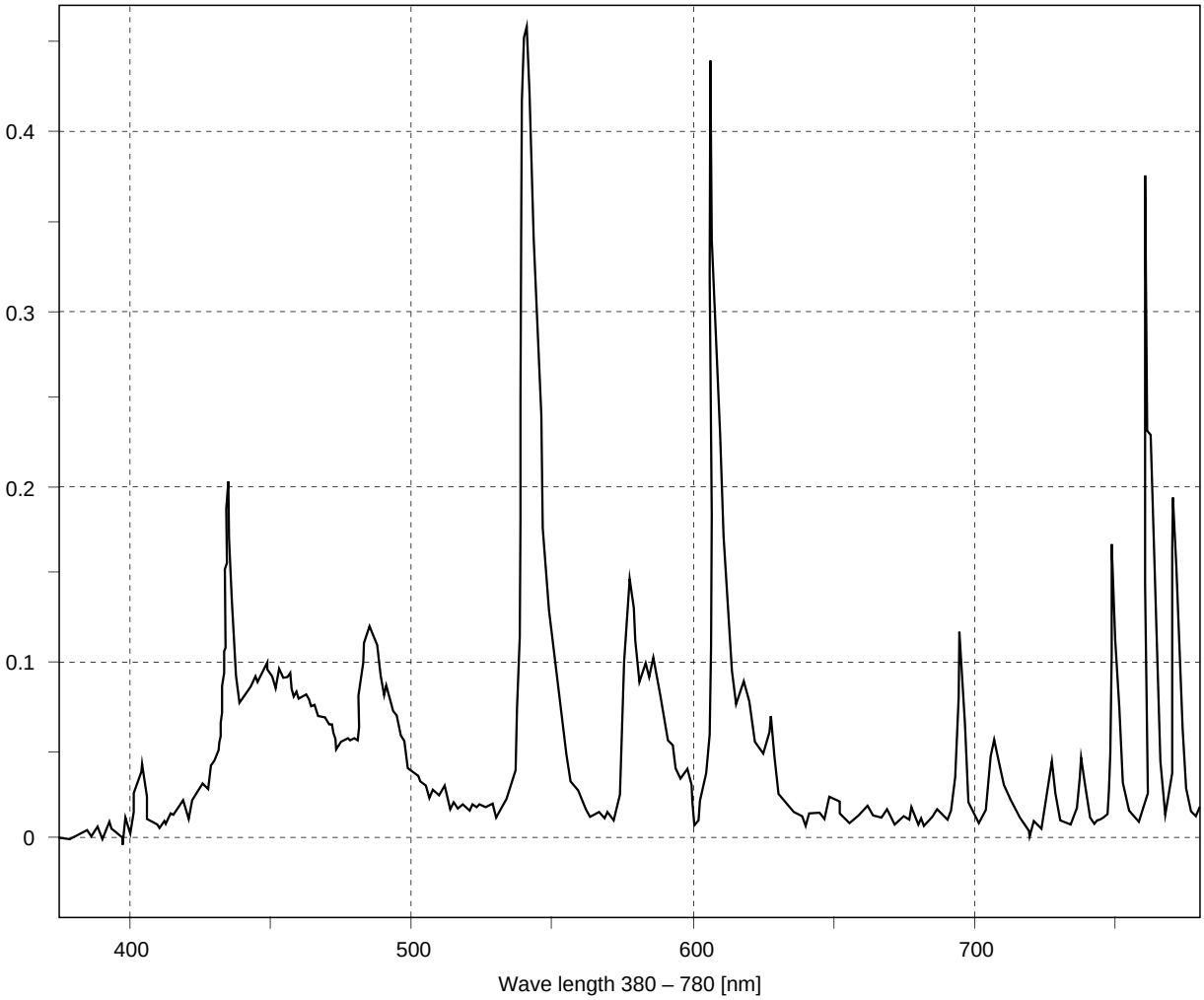
9-1. Method of Measuring Flicker

In the field invert drive mode, adjust the flicker level of the half tone (Vsig = 1.5 to 2.5V) using the photoelectric element and oscilloscope so that its 30Hz component becomes minimum. The Vcom value at this time is taken to be the optimum Vcom.

9-2. Method of Measuring Contrast

In the normal 1H invert drive mode, adjust the optical output voltage of the half tone (Vsig = 1.5 to 2.5V) so that it becomes minimum. The Vcom value at this time is taken to be the optimum Vcom.

Example of Back Light Spectrum (Reference)

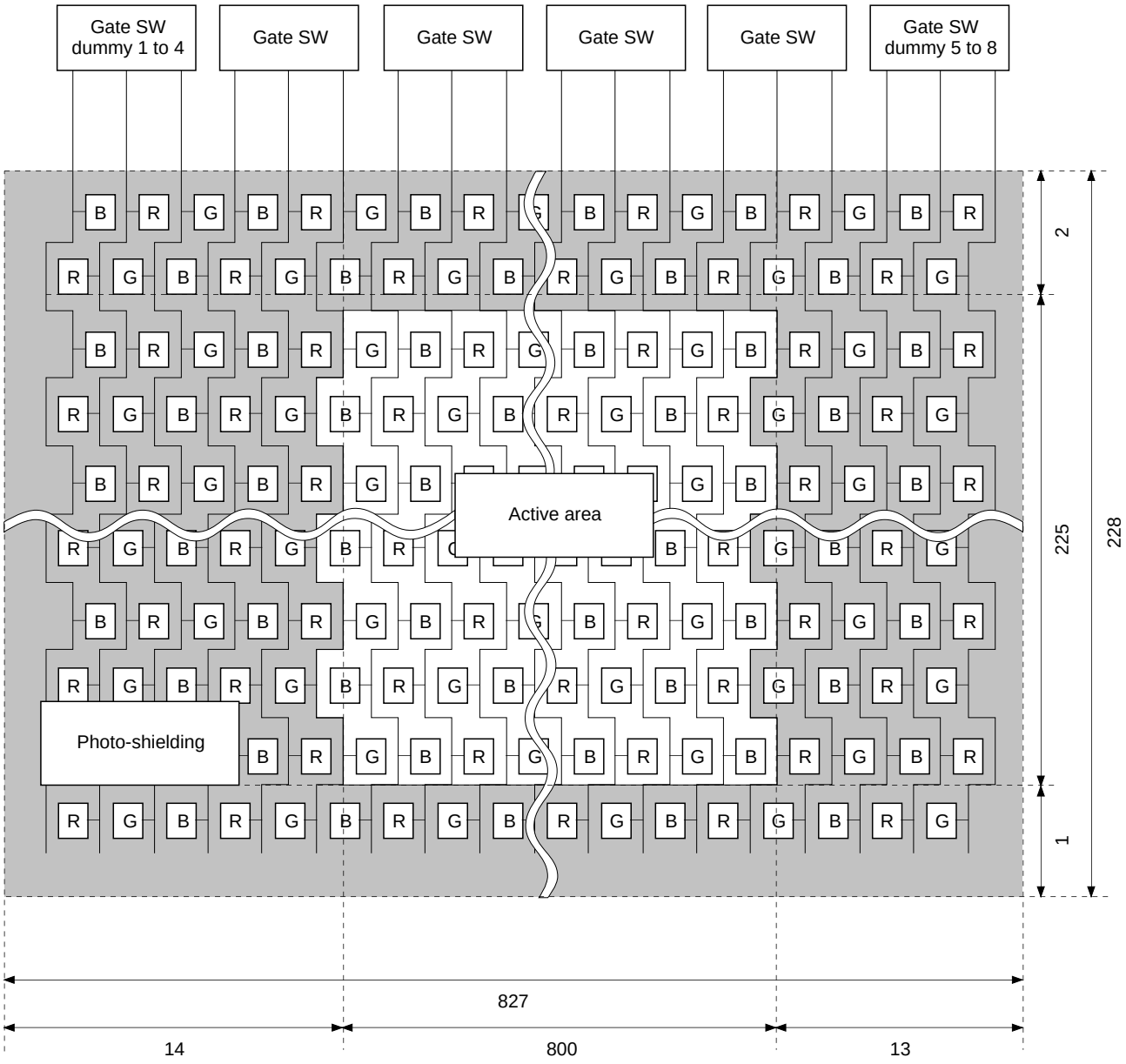


Description of Operation

1. Color Coding

Color filters are coded in a delta arrangement.

The shaded area is used for the dark border around the display.



2. LCD Panel Operations

- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to every 225 gate lines sequentially in every single horizontal scanning period. A vertical shift register scans the gate lines from the top to bottom of the panel.

- The selected pulse is delivered when the enable pin turns to High level. PAL mode images are displayed by controlling the enable and VCK1, VCK2 pins. The enable pin should be High when not in use.

- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuit, applies selected pulses to every 800 signal electrodes sequentially in a single horizontal scanning period.

- Scanning direction of horizontal shift register can be switched with RGT pin.Scanning direction is left to right for RGT pin at High level; and right to left for RGT pin at Low level.(These scanning directions are from a front view.) Normally, set to High level.

- Vertical and horizontal drivers address one pixel, and then dot Thin Film Transistors (TFTs; two TFTs for one dot) turn on to apply a video signal to the dot. The same procedures lead to the entire 225 × 800 dots to display a picture in a single vertical scanning period.

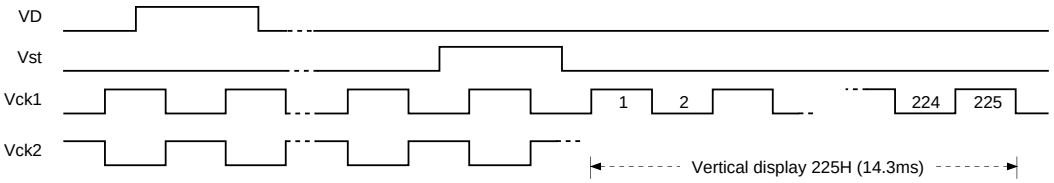
- Pixels are arranged in a delta pattern, where sets of RGB pixels are positioned with 1.5-dot offset against juxtaposed horizontal line. For this reason, 1.5-dot offset of a horizontal driver output pulse against horizontal synchronized pulse is required to apply a video signal to each dot properly. 1 H reversed displaying mode is required to apply video signal to the panel.

- The CLR pin is provided to eliminate the shading effect caused by the coupling of selected pulses. While maintaining the CLR at High level, the VV_{DD} potential drops to approximately 8.5V. This pin should be grounded when not in use.

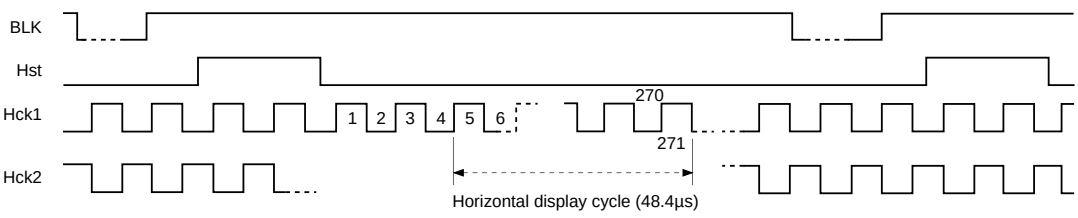
- The video signal must be input with polarity-inverted system in every horizontal cycle.

- Timing diagrams of the vertical and the horizontal right-direction scanning (RGT = High level) display cycle are shown below.
  Hck1 and Hck2 should be exchanged to display the left-direction horizontal scanning (RGT = Low level). This exchange enables the center of the image to be fixed by eliminating offsets.

(1) Vertical display cycle



(2) Horizontal display cycle (right-direction scanning)



The horizontal display cycle consists of 800/3 = 267 clock pulses because of RGB simultaneous sampling*.

* Refer to Description of Operation "3. RGB Simultaneous Sampling"

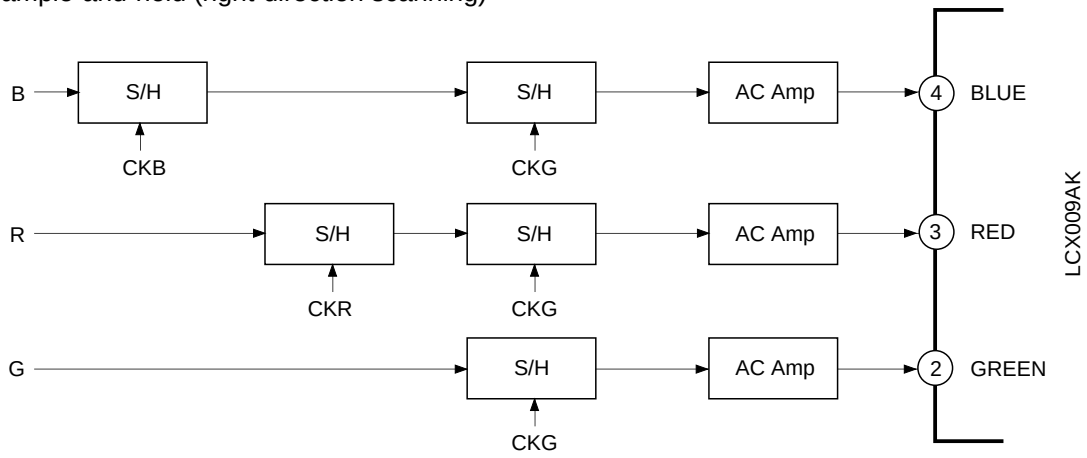
3. RGB Simultaneous Sampling

Horizontal driver performs R, G and B signal sampling simultaneously, which requires the phase matching between R, G, B signals to prevent horizontal resolution from deteriorating. The phase matching by an external signal delaying circuit is needed before applying video signal to the LCD panel.

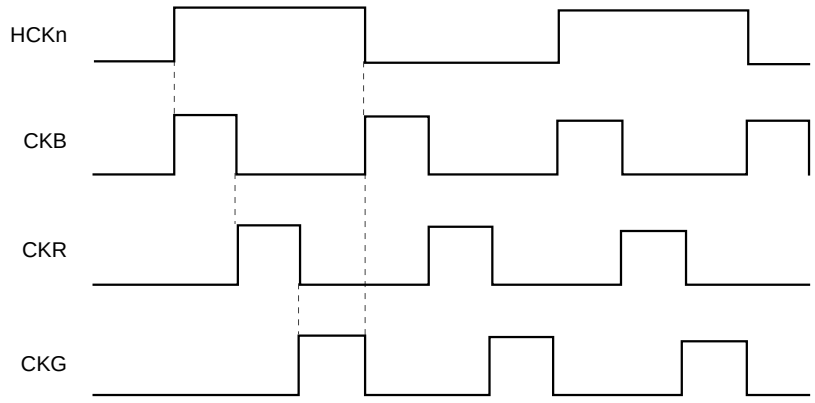
Two methods are applied for the delaying procedure: Sample-and-hold and Delay circuit. These two block diagrams are as follows.

The LCX009 has a right/left inverse function. The following phase relationship diagram indicates the phase setting for the right-direction scanning (RGT = High level). For the left-direction scanning (RGT = Low level), the phase setting should be inverted for B and G signals.

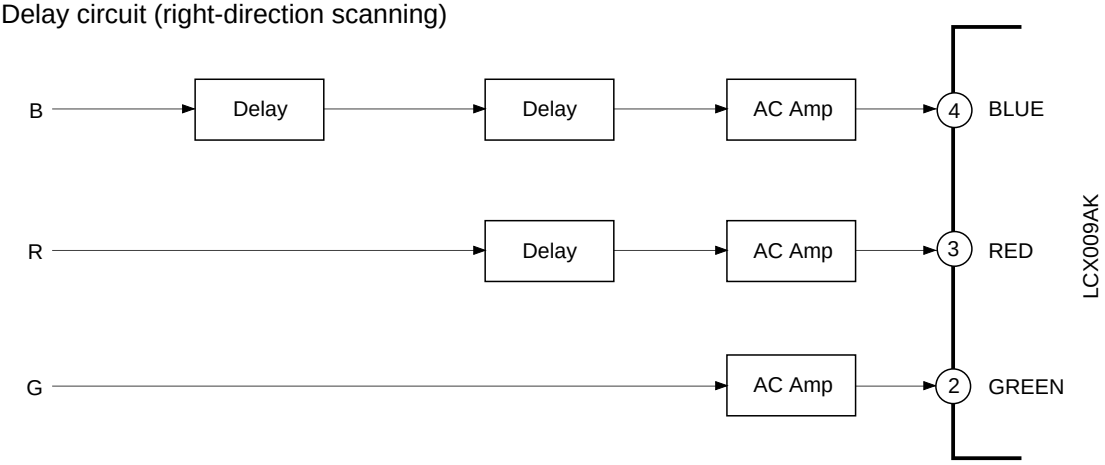
(1) Sample-and-hold (right-direction scanning)



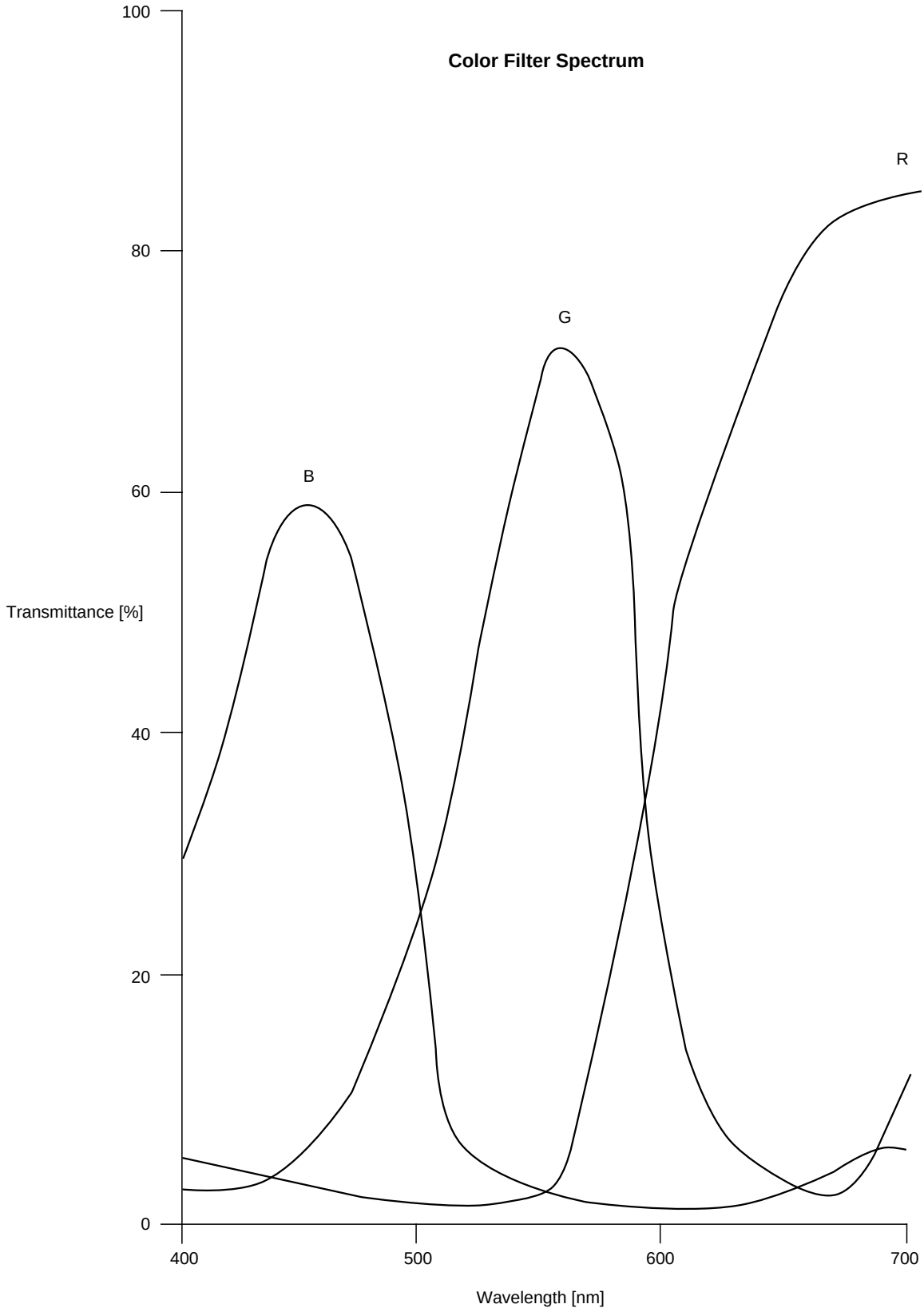
<Phase relationship of delaying sample-and-hold pulses> (right-direction scanning)



(2) Delay circuit (right-direction scanning)

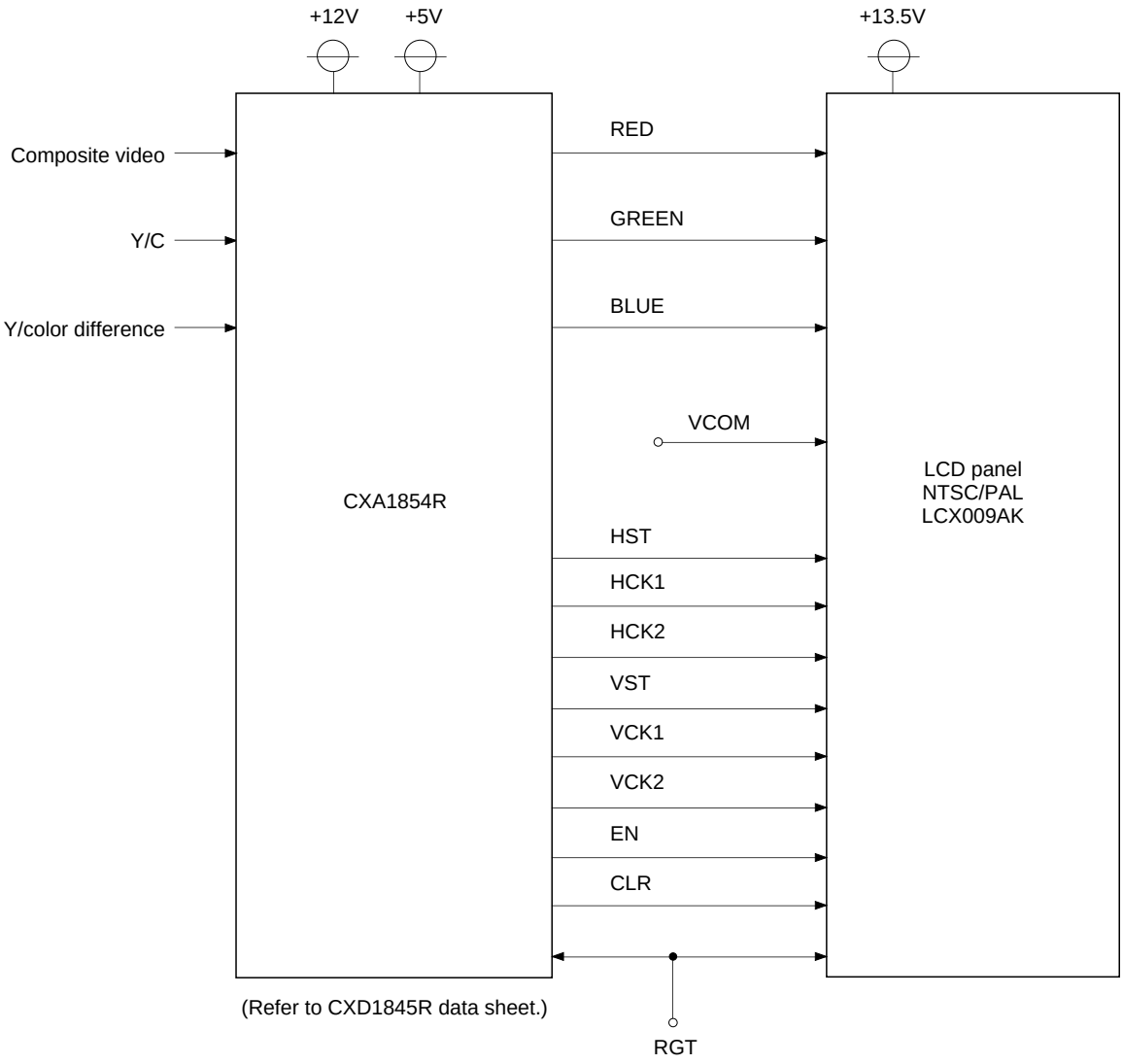


Example of Color Filter Spectrum (Reference)



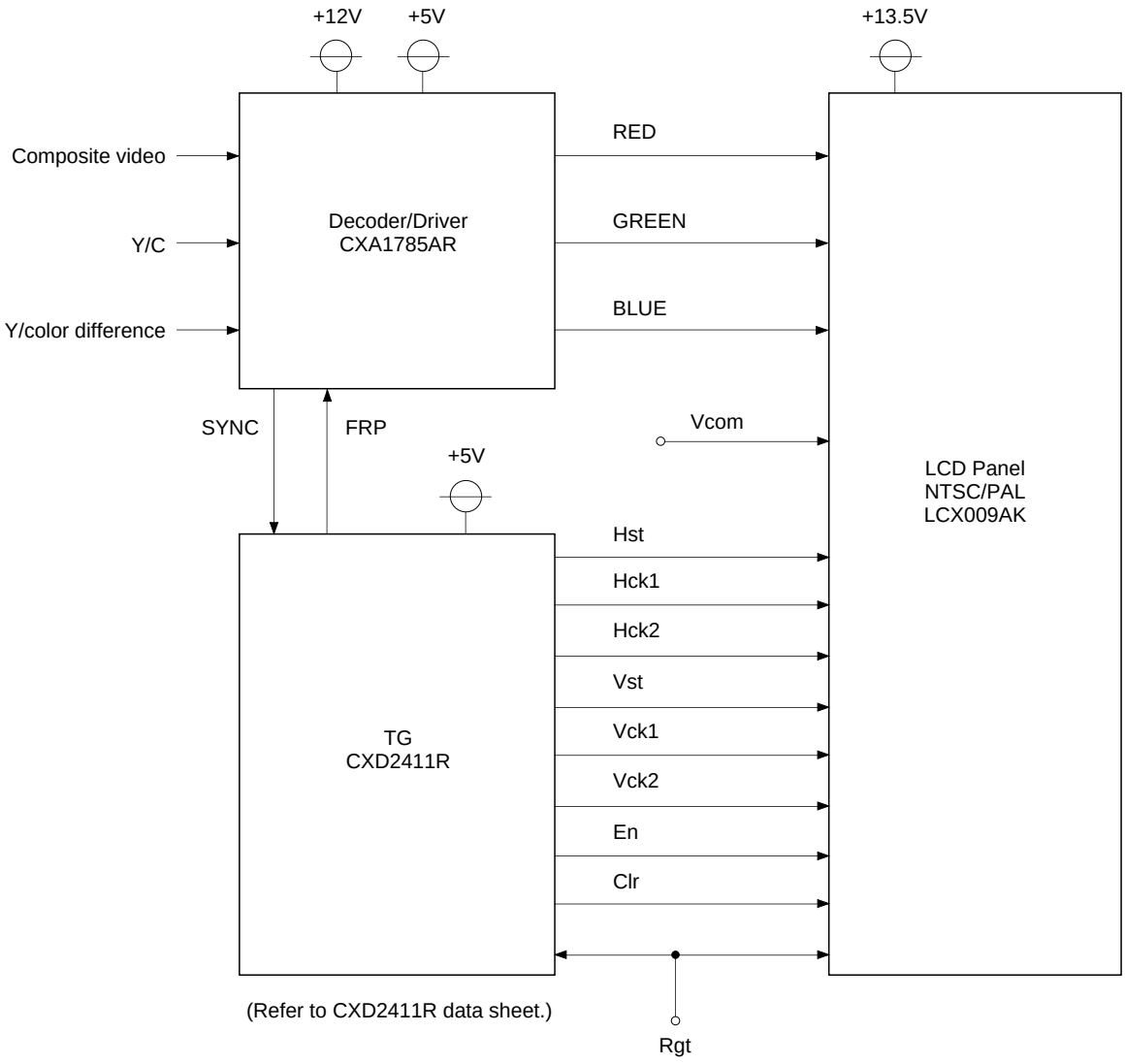
Color Display System Block Diagram (1)

An example of single-chip display system is shown below.



Color Display System Block Diagram (2)

An example of dual-chip display system is shown below.



Notes on Handling

(1) Static charge prevention

Be sure to take following protective measures. TFT-LCD panels are easily damaged by static charge.

a) Use non-chargeable gloves, or simply use bare hands.
b) Use an earth-band when handling.
c) Do not touch any electrodes of a panel.
d) Wear non-chargeable clothes and conductive shoes.
e) Install conductive mat on the working floor and working table.
f) Keep panels away from any charged materials.
g) Use ionized air to discharge the panels.

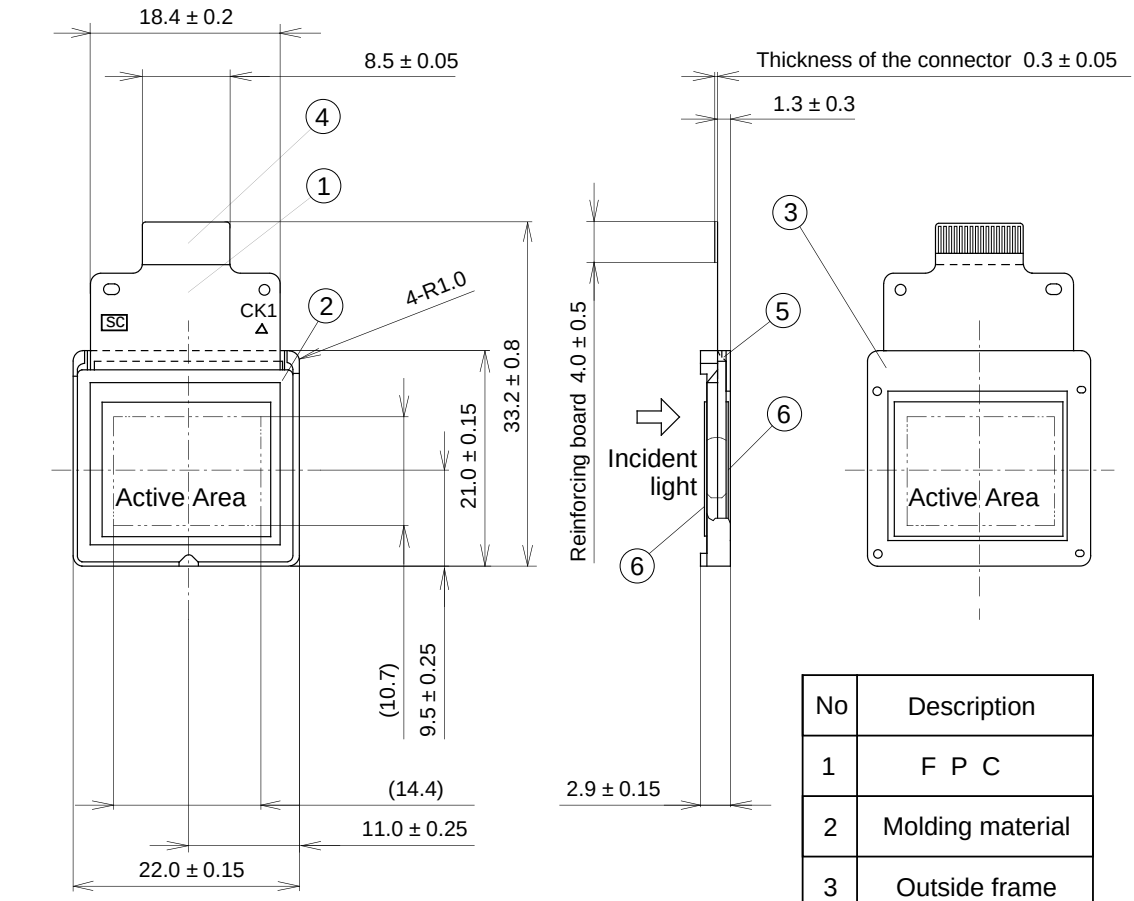
(2) Protection from dust and dirt

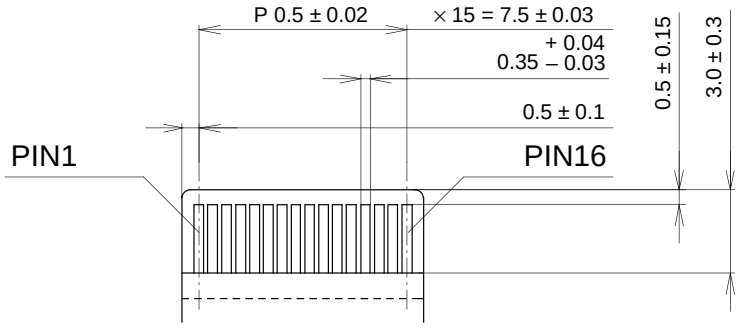
a) Operate in clean environment.
b) When delivered, a surface of a panel (Polarizer) is covered by a protective sheet. Peel off the protective sheet carefully not to damage the panel.
c) Do not touch the surface of a panel. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stain on the surface.
d) Use ionized air to blow off dust at a panel.

(3) Other handling precautions

a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
b) Do not drop a panel.
c) Do not twist or bend a panel or a panel frame.
d) Keep a panel away from heat source.
e) Do not dampen a panel with water or other solvents.
f) Avoid to store or to use a panel in high temperature or in high humidity, which results in panel damages.

Package Outline Unit: mm





electrode (enlarged)

No	Description
1	F P C
2	Molding material
3	Outside frame
4	Reinforcing board
5	Reinforcing material
6	Polarizing film

weight 2g