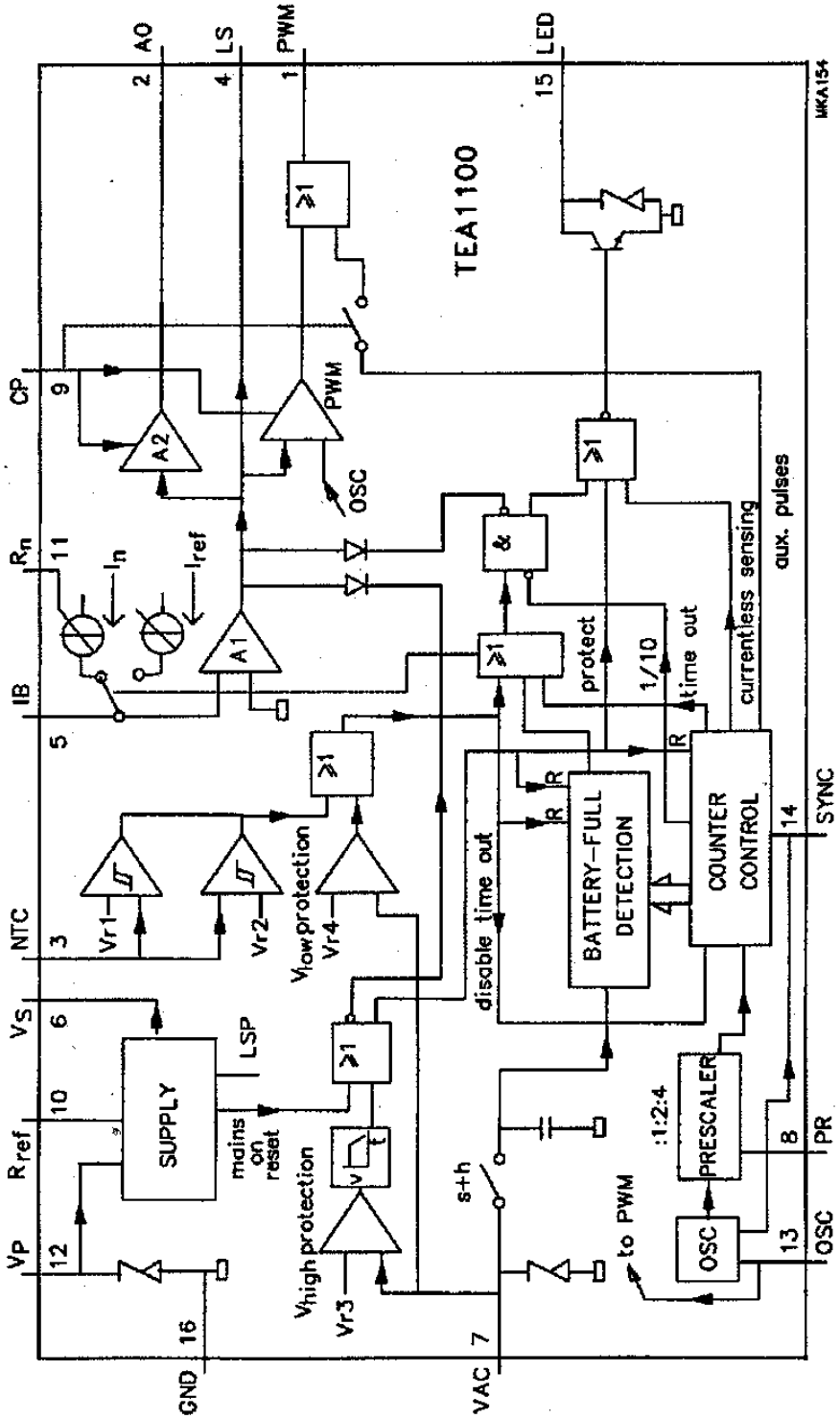



Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

## FEATURES

- Accurate regulation of charge current settings in co-operation with a switched mode power supply
- Accurate detection of fully charged batteries by currentless battery voltage sensing
- Switch over from fast to normal charging when batteries are fully charged
- Adjustable fast charging level (1 C to 5 C)
- Adjustable normal charging level (0.05 C to 0.25 C)
- Temperature guarding by means of an NTC resistor
- Tracking of maximum fast charging time with fast charging current level
- Protections against short-circuited and open batteries
- Large battery voltage range
- Both DC and PWM outputs with polarity switch

## APPLICATIONS

- Charge systems for NiCd and NiMH batteries

## GENERAL DESCRIPTION

The TEA1100 is manufactured in a BICMOS process intended to be used as a battery monitor circuit in charge systems for NiCd and NiMH batteries.

The circuit has to be situated on the secondary side in mains-isolated systems where it monitors the battery voltage and the charge current. The circuit drives, by means of an opto-coupler or a pulse transformer interface, an SMPS circuit, situated on the primary side of the system, thus controlling the charge current of the batteries. The circuit can drive the external power transistor in switched mode systems, which have a DC power source, via a driver stage.

## ORDERING INFORMATION

| EXTENDED TYPE NUMBER | PACKAGE | | | |
|---|---|---|---|---|
| | PINS | PIN POSITION | MATERIAL | CODE |
| TEA1100 | 16 | DIL | plastic | SOT38G |
| TEA1100T | 16 | SO16L | plastic | SOT162A |

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_P$ | positive supply voltage range | | 5.65 | – | 11.5 | V |
| $I_P$ | supply current | outputs off | – | – | 4.1 | mA |
| $V_{VAC}$ | voltage range of battery-full detection | | 0.385 | – | 3.85 | V |
| $dV_{VAC}/V_{VAC}$ | –dV detection level w.r.t. top value | note 1 | – | 1 | – | % |
| $I_{VAC}$ | input current battery monitor | | – | – | 1 | nA |
| $V_{VAC}$ | voltage protection<br>battery low<br>battery high | | <br>–<br>– | <br>0.3<br>4.25 | <br>–<br>– | <br>V<br>V |
| <br>$I_{ref}$<br>$I_n$ | charging level<br><br>fast<br>normal | $I_{charge} = R1/R_s \times I$; see Fig. 3<br>$I = I_{ref}$<br>$I = 1/p \times 0.1 \times I_n$<br>(p = prescale factor) | <br>20<br>10 | <br>–<br>– | <br>100<br>50 | <br>µA<br>µA |
| $f_{osc}$ | oscillator frequency | | 10 | – | 100 | kHz |

**Note to the quick reference data**

1. The –dV detection level can be adjusted by use of an external voltage regulator diode to increase the sensitivity.

# Battery monitor for NiCd and NiMH chargers

# TEA1101; TEA1101T

## FEATURES

- Accurate detection of fully charged batteries by currentless –dV sensing
- Digital filtering of the battery voltage to avoid false –dV triggering
- Minimum and maximum temperature guarding by means of an NTC resistor
- Battery checking to protect against short-circuit and open batteries
- Battery monitor allows recharging different battery-pack voltages
- Tracking of maximum fast charging time with fast charging current level
- Accurate regulation of charge current settings in co-operation with a switched mode power supply or DC current source
- Both DC and PWM outputs with polarity switch
- Adjustable fast charge level (1 C to 5 C)
- Adjustable pulsating trickle charge level (0.05 C to 0.25 C)
- Large operating temperature range.

## APPLICATIONS

- Charge systems for NiCd and NiMH batteries.

## GENERAL DESCRIPTION

The TEA1101 is manufactured in a BICMOS process intended to be used as a battery monitor circuit in charge systems for NiCd and NiMH batteries.

The circuit has to be situated on the secondary side in mains-isolated systems where it monitors the battery voltage and the charge current. The circuit drives, by means of an opto-coupler or a pulse transformer interface, an SMPS circuit, situated on the primary side of the system, thus controlling the charge current of the batteries.

The circuit can drive the external power transistor in switched mode systems, which have a DC power source, via a driver stage.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_P$ | positive supply voltage | | 5.65 | – | 11.5 | V |
| $I_P$ | supply current | outputs off | – | – | 4.3 | mA |
| $V_{VAC}$ | voltage range of battery-full detection | | 0.385 | – | 3.85 | V |
| $dV_{VAC}/V_{VAC}$ | –dV detection level w.r.t. top value | note 1 | – | 0.25 | – | % |
| $I_{VAC}$ | input current battery monitor | | – | – | 1 | nA |
| $V_{VAC}$ | voltage protection | | | | | |
| | battery low | | – | 0.3 | – | V |
| | battery high | | – | 4.25 | – | V |
| | charging level | $I_{charge} = R1/R_s \times I$; see Fig.3 | | | | |
| $I_{ref}$ | fast | $I = I_{ref}$ | 20 | – | 100 | µA |
| $I_n$ | normal | $I = 1/p \times 0.1 \times I_n$ (p = prescale factor) | 10 | – | 50 | µA |
| $f_{osc}$ | oscillator frequency | | 10 | – | 100 | kHz |

### Note

1. The –dV detection level can be adjusted by use of an external voltage regulator diode to increase the sensitivity.

## ORDERING INFORMATION

| EXTENDED TYPE NUMBER | PACKAGE | | | |
|---|---|---|---|---|
| | PINS | PIN POSITION | MATERIAL | CODE |
| TEA1101 | 16 | DIL | plastic | SOT38G |
| TEA1101T | 16 | SO16L | plastic | SOT162A |

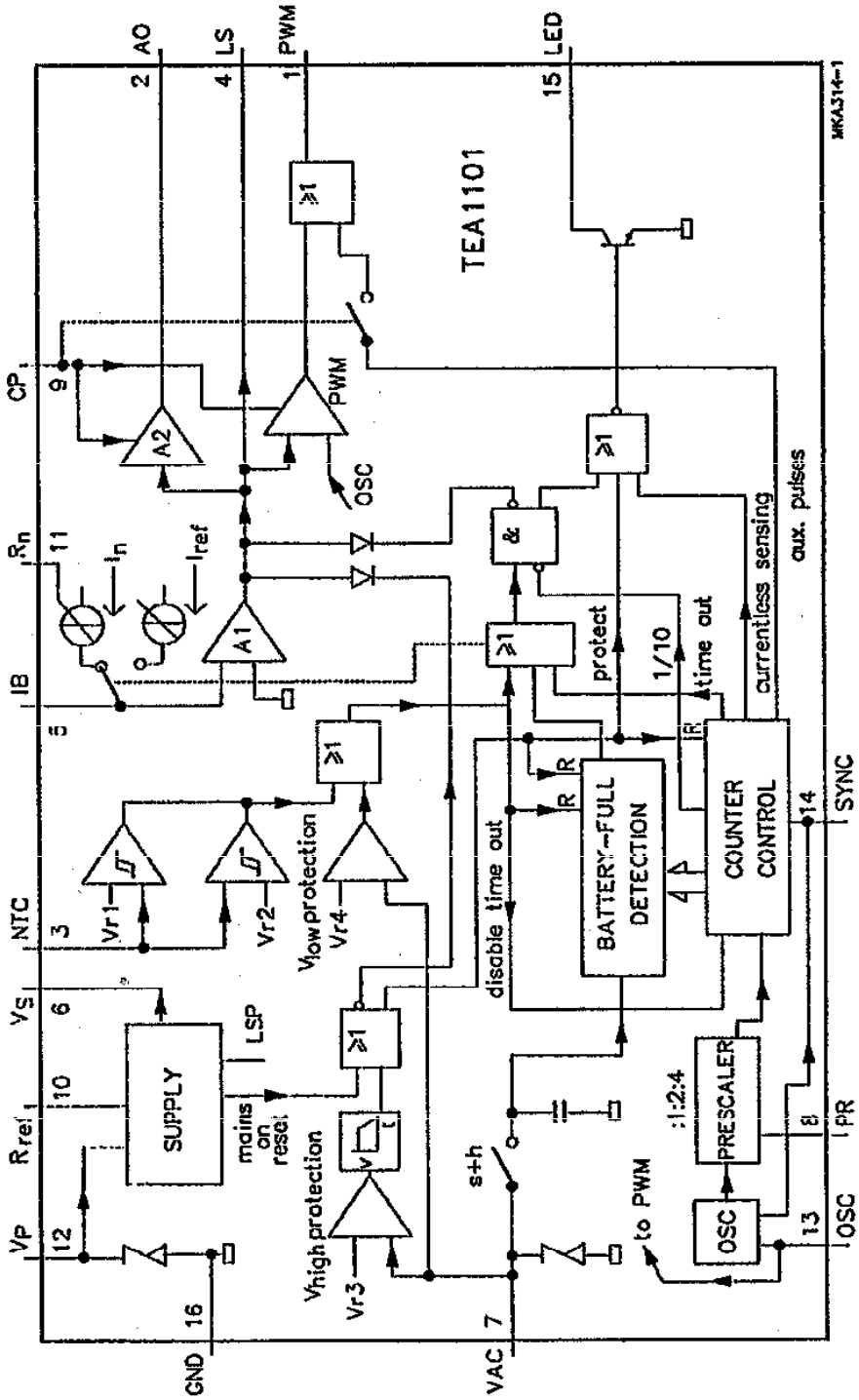



Fig.1 Block diagram.

## PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| PWM | 1 | pulse width modulator |
| AO | 2 | analog output |
| NTC | 3 | temperature sensor input |
| LS | 4 | loop stability |
| IB | 5 | charge current |
| $V_S$ | 6 | stabilized supply voltage |
| VAC | 7 | battery voltage |
| PR | 8 | prescaler |
| CP | 9 | change polarity |
| $R_{ref}$ | 10 | reference resistor |
| $R_n$ | 11 | normal charge reference resistor |
| $V_P$ | 12 | positive supply voltage |
| OSC | 13 | oscillator input |
| SYNC | 14 | synchronization input |
| LED | 15 | LED output |
| GND | 16 | ground |

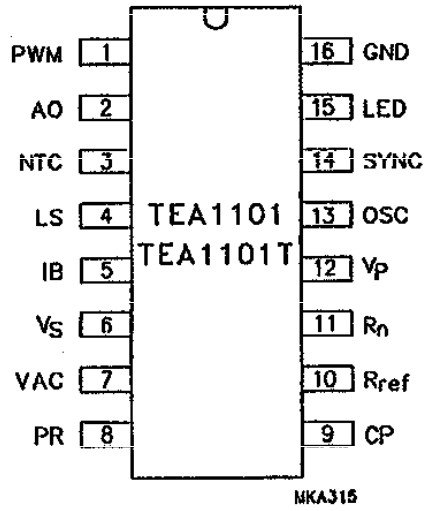



Fig.2 Pin configuration.

## FUNCTIONAL DESCRIPTION

The operation of the circuit will be explained with the aid of Fig.1 (block diagram) and Fig.3 (application diagram). The circuit is divided into several blocks which are described separately.

### Supply block

The circuit requires a supply voltage on pin $V_P$ with a value between 5.65 and 11.5 V. Above 6.4 V typical, the circuit starts up assuming that mains is connected to the system and the charge session begins. This supply can be generated by a separate winding on the transformer, as shown in Fig.3, in either the flyback or the forward stroke. Another possibility is rectification from the mains secondary winding (at the connection D1 and L2). Considerations for choosing the method of supplying the IC are:

- Supply voltage range of 5.65 to 11.5 V under all circumstances (also during the 90% pause at normal charging, the standby current then is 1 mA typical)
- Maximum battery voltage (flyback stroke)
- Minimum power delivered by the primary SMPS (normal charging)

The supply block delivers the following outputs:

- By using an external resistor $R_{ref}$ at pin 10 a reference current is obtained which defines all external related currents (charge reference currents, oscillator)
- Externally available 4.25 V stabilized voltage source ($V_S$). This source is used internally for a large part of the circuit and can be used to set the NTC biasing and to supply other external circuitry. $V_S$ is cut off in the 90% pause during normal charging
- Low Supply voltage Protection signal (LSP). When the supply voltage is lower than 5.25 V typical, there is enough supply voltage left to switch off the power regulation and hereafter the IC current is limited to the start level of 35 µA typical
- Mains on reset pulse resets all digital circuitry after a start or restart due to an interrupted supply ($V_P$).

### Charge current regulation

The charge current has to be sensed by means of a low-ohmic resistor in series with diode D1. The waveform on resistor $R_s$ (see Fig.5 for a flyback converter) has the form of a negative-going ramp and after filtering a negative DC voltage is obtained. A positive voltage across resistor R1 is created by means of the current sources set by the pins $R_{ref}$ and $R_n$. The error amplifier A1

references the result to ground and via the regulation loop of the SMPS, the secondary current will be regulated to a value which is defined by:

$I_{ch} \times R_s = R1 \times I_{ref}$ (fast charge) or,
$I_{ch} \times R_s = R1 \times I_n$ (normal charge)

The $I_{ref}$ current is the fast charging reference current, the $I_n$ current is used for regulation after a full battery is detected. The $I_{ref}$ current is the reference current set by $R_{ref}$ while $I_n$ is dependent on the resistor at pin $R_n$. With no resistor on pin $R_n$, the $I_n$ current has a default value which is half the $I_{ref}$ current.
By choosing the correct resistor values $R_s$, R1, $R_{ref}$ and $R_n$, a wide range of charge currents can be set plus a wide range of the ratio fast charge current as a function of normal charge current. For determination of the normal charge current the 1:10 duty cycle and the programmable prescale factor (p) should be taken into account (see Logic block); $I_n = 1/p \times 0.1 \times I_{ref}$. The output of amplifier A1 is available at the loop stability pin (LS), so the time constant of the SMPS loop can be set at the secondary side of the system.

### NTC block

The voltage at the NTC pin is compared with two reference voltages. When the NTC voltage is between $V_{r1}$ and $V_{r2}$, the charge current regulation is unaffected. When the NTC voltage is outside this window, the power of the SMPS is reduced to the normal charge level.
The NTC input can be used for temperature protection as shown in Fig.3 (application diagram) by using a suitable NTC resistor. To avoid switching on and off with temperature, a hysteresis is built in for both levels.

### Output drivers

The SMPS regulation signal is available at different pins:

- Analog voltage output (push or pull) at AO (pin 2) to drive an opto-coupler in mains separated applications when an external resistor is connected between AO and the opto-coupler. The maximum current through the opto-coupler diode is 2 mA. The voltage gain of amplifier A2 is: $A = (V_{LS} - 1.4) \times 4$ and is typically 12 dB. The voltage at AO can also be used to directly drive a PWM input of an SMPS circuit. During 'inhibit SMPS' the AO output is fixed to zero charge current for currentless sensing
- The LS voltage is compared internally with the oscillator voltage to deliver a pulse width modulated output at PWM (pin 1) to drive an output device in a DC/DC converter application via a driver stage. The PWM output is latched to prevent multi-pulsing. Moreover with the latch a kind of current mode control is possible. The maximum duty factor is internally fixed to 78% (typical). The 'PWM' output can be used for synchronization and duty factor control of a primary SMPS via a pulse transformer (the SMPS inhibit and auxiliary pulses are also available at pin PWM)
- The AO and PWM outputs can be changed in polarity by programming the change polarity pin CP. The PWM output in the on-state pushes current (CP = 0) or pulls current (CP = 1). The appearance of the auxiliary pulses at pin PWM can also be programmed with CP.

The 'LED' output pin offers the following output signals:

- 10/90% signal for driving a LED when the duty factor is too small during the 10% time. This occurs when there is a large difference between fast and normal charge currents. The LED frequency is $f_{LED} = 2^{-12} \times 1/p \times f_{osc}$
- An SMPS inhibit period (duration 10 OSC pulses) for currentless VAC sensing
- VAC high voltage protection signals.

### Battery monitor

Two batteries can be connected directly to the 'VAC' pin (Voltage ACcumulator). At higher battery voltages it is advised to divide the battery voltage with a factor by an external resistor tap, before offering this to pin VAC. It is also possible to take a tap on the chain of batteries. The VAC voltage range has to be between 0.385 V and 3.85 V.
The VAC voltage is sampled at a low cycle frequency ($f_{cycle} = 2^{-16} \times f_{osc}$) and the analog value of VAC is digitized and stored in a register. One cycle later, the digitized value is converted back to the analog value and compared with the actual value of VAC. If the actual value is higher, then the new VAC voltage is stored in the register, otherwise no conversion is carried out. Thus the VAC top value is stored and it is possible to detect an increasing VAC indicating 'not yet full batteries' or decreasing VAC indicating that the batteries are probably fully charged. The circuit waits until the battery voltage has dropped 0.25% below the top value before indicating 'full batteries'. However, by applying a voltage regulator diode in the battery voltage sense-line (see Fig.8) an increased sensitivity of the –dV detection level can be obtained, e.g. 0.125%.
In Fig.6 the battery voltage as

function of the charging time is shown. The negative slope depends on the charge current and the battery type.

The switching of the SMPS can cause interference on the battery voltage and therefore it has been necessary to stop the SMPS during the inhibit time (see Fig.9). This can be achieved automatically via the regulation pins AO and PWM or by using the SYNC output of the logic block. The SMPS is stopped for 10 periods at the end of which sampling is carried out. The VAC voltage will now be sensed currentless. To avoid false decisions concerning a falling VAC voltage, VAC is digitally filtered and analog stored in a sample-and-hold circuit. This approach ensures, even at very high –dV sensitivity (<0.25%) accurate detection of the battery full condition. Immediately after decisions and VAC digitizing takes place. The benefit of a sample-and-hold circuit is that at high frequencies the noise on the VAC voltage is filtered and the VAC manipulations like decisions and digitizing are carried out on the same VAC voltage available in the sample-and-hold circuit.

When a –dV is detected, the reference current $I_{ref}$ is switched off, the normal current $I_n$ is switched on during 10% of regulation and the outputs are high-ohmic during 90%. This 1:10 ratio in active regulation, together with the ratio in reference currents ($I_n$ as a function of $I_{ref}$), ensures that the resulting charge current is low enough to be allowed to flow through the batteries for a long time to overcome the self-discharge of the batteries without causing memory effects. If the prescale factor p is programmed, the $I_n$ current has to be lowered with the p factor, so $I_n = 1/p \times 0.1 \times I_n$.

**Protections**

- The circuit goes into standby (not active, low current consumption) when the supply voltage is less than 5.25 V (LSP).
- When the divided battery voltage exceeds the $V_{r3}$ level (nominal 4.25 V) this is recognized as open or removed batteries and the output control signals terminate to stop the SMPS operation. This over-voltage sensing is digitally filtered. In above events the 'battery full detector' and the 'counter/control' will be reset.
- When the divided battery voltage is less than $V_{r4}$ (0.3 V), the circuit assumes short-circuited batteries, the charge current is reduced to the normal charge level. As soon as the voltage exceeds $V_{r4}$, the fast charging starts.
- The temperature protections are already mentioned in section NTC. In the event of short-circuited batteries or active temperature protections the 'battery full detector' is reset and the 'counter/control' is stopped.

**Oscillator and control logic**

The complete timing of the circuit is controlled by the oscillator.
The period time is defined by:
$T_{osc} = 0.93 \times R_{ref} \times C_{osc}$.

The counter block defines a maximum fast charge time called 'Time Out' (TO). As the charge current and the oscillator frequency (and thus the TO) are both set by $R_{ref}$, changing one affects the other. Initially the oscillator capacitor can be chosen such that the fast charge time is half the TO time. This means that in the event of a one hour (1C) charger, the TO signal occurs at 2 hours, in the event of a quarter of an hour (4C) charger, the TO signal is active after half an hour. After that the circuit switches over to normal charging.

To adapt the SMPS switching frequency in the synchronized mode to the required oscillator frequency of the timing logic, the timer logic is preceded by a programmable divider. The divider ratio can be set to 1, 2 or 4 (p factor) by means of the PR pin. Doing this means that the oscillator frequency can be increased with the factor p without changing TO.

Fast charging current:
$I_{ch} = R1/R_s \times V_{ref}/R_{ref}$
Time out:
$TO = 2^{26} \times 0.93 \times R_{ref} \times C_{osc} \times p$
Normal charging current:
$I_{ch} = R1/R_s \times 1/p \times 0.1 \times V_{ref}/R_n$

The control block determines the following timing sequences:

- VAC sampling; this takes 1 clock pulse every interval cycle.

  The power converter is switched off during VAC sampling. As there are several types of converters, there also are several control signals available at :

  pin 'SYNC' for synchronization in analog voltage controlled primary SMPS circuits

  pin 'PWM' for digital controlled primary SMPS and DC/DC converters

  pin 'LED' in special applications
- Disabling –dV during $2^{-5} \times TO$ (3% of TO) for correct start with flat or inversely polarized batteries. Disabling is active at each fast charge cycle
- Maximum fast charging time (TO): the maximum timer is stopped during VAC low voltage protection and outside temperature range

- The normal charge duty cycle is 1/p x 0.1
- Auxiliary pulses to support the supply voltage of the primary SMPS circuit via pin PWM: the pulses can be programmed on and off at an appearance rate of $f_{osc}/8$ with a duty cycle of 14%; programming is achieved by activating CP.

The timing logic and the –dV recognition circuitry are reset after each supply voltage failure and after a battery over-voltage recognition. The –dV circuit is also reset during normal charging.

The SYNC output delivers negative-going synchronization pulses which are suppressed during the sampling of the battery voltage. With these sync pulses the SMPS can be synchronized.The polarity of the sync pulses is chosen so that in the event of an open SYNC pin in the synchronization mode, the power is regulated to a minimum. During the VAC sampling the absense of sync pulses causes the SMPS to stop thus minimizing interference (see Fig.9, synchronization waveforms).

During the 90% pause, only the oscillator and the control logic are operative to save current. In the pause $V_P$ is never allowed to become less than $V_{LSP}$. This would cause a 'mains-on-reset' and thus fast charging.

**Programming**

With pins 'CP' (change polarity) and 'PR' (prescaler) several functions can be programmed.

By defining the current ($V_{ref}/R_{CP}$) at pin CP, the following functions can be activated :

| | | |
|---|---|---|
| 1 | change polarity | CP = 0, normal polarity<br>CP = 1, changed polarity |
| 2 | no auxilliary pulses at PWM | aux = 0 |
| 3 | auxilliary pulses at f/8 | aux = 8 |

| CP PIN | FUNCTIONS | |
|---|---|---|
| | CP | aux |
| Open pin | 0 | 0 |
| 10 µA | 0 | 8 |
| 22 µA | 1 | 0 |
| 57 µA | 1 | 8 |

By defining the voltage at pin PR, the following functions can be activated :

| PR PIN | FUNCTIONS |
|---|---|
| $V_s$ | prescaler divide by 1 |
| Open pin | prescaler divide by 2 |
| Ground | prescaler divide by 4 |

**Table 1 Formulae.**

| DESCRIPTION | SYMBOL | FORMULA | FUNCTION |
|---|---|---|---|
| Timing | $T_{osc}$ | $0.93 \times R_{ref} \times C_{osc}$ | repetition |
| | TO | $2^{-26} \times p \times T_{osc}$ | duration |
| | $T_{disable}$ | $2^{-5} \times TO$ | duration |
| | $T_{LED} = T_{trickle}$ | $2^{12} \times p \times T_{osc}$ | repetition |
| | $T_{LED} = T_{trickel}$ | $3/4 \times 2^{9} \times T_{osc}$ | duration |
| | $T_{inhibit}$ | $2^{16} \times T_{osc}$ | repetition |
| | $T_{inhibit}$ | $10 \times T_{osc}$ | duration |
| Charge currents | $I_{fast}$ | $R1/R_s \times V_{ref}/R_{ref}$ | |
| | $I_{normal}$ | $R1/R_s \times 1/p \times 0.1V_{ref}/R_{ref}$ | |

## LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134); note 1.

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| **Voltages** | | | | |
| $V_P$ | positive supply voltage (pin12) | −0.5 | 13.2 | V |
| $V_{LED}$ | LED voltage (pin 15) | −0.5 | 13.2 | V |
| $V_{1,8,4,3}$ | voltage at PWM (pin 1), PR (pin 8), LS (pin 4), NTC (pin 3) | −0.5 | $V_P$ | V |
| $V_{IB}$ | voltage at IB (pin 5) | −0.5 | +1 | V |
| **Currents** | | | | |
| $I_{VS}$ | current at $V_S$ (pin 6) | −3 | +0.01 | mA |
| $I_{LED}$ | current at LED (pin 15) | − | 25 | mA |
| $I_{AO}$ | current at AO (pin 2) | −5 | +5 | mA |
| $I_{PWM}$ | current at PWM (pin 1) | −15 | +15 | mA |
| $I_{SYNC}$ | current at SYNC (pin 14) | −2 | +2 | mA |
| $I_{11,10,9}$ | current at $R_n$ (pin 11), $R_{ref}$ (pin 10), CP (pin 9) | −1 | +0.01 | mA |
| $I_{4,5,7}$ | current at LS (pin 4), IB (pin 5), VAC (pin 7) | −1 | +1 | mA |
| $I_P$ | current at $V_P$ (pin 6) | − | 15 | mA |
| **Dissipation** | | | | |
| $P_{tot}$ | total power dissipation at $T_{amb}$ = 85 °C | | | |
| | SOT38G | − | 0.6 | W |
| | SOT162A | − | 0.3 | W |
| **Temperatures** | | | | |
| $T_{amb}$ | operating ambient temperature | −20 | +85 | °C |
| $T_j$ | junction temperature | − | +150 | °C |
| $T_{stg}$ | storage temperature | −55 | +150 | °C |

**Note**

1. All voltages with respect to ground; positive currents flow into the IC; all pins not mentioned in the voltage list are not allowed to be voltage driven. The voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the power rating is not violated.

## CHARACTERISTICS

$V_P$ = 10 V; $T_{amb}$ = 25 °C; $R_{ref}$ = 33 kΩ; $R_n$ = 68 kΩ; $C_{OSC}$ = 1 nF; CP open-circuit; PR connected to $V_S$; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supply ($V_P$, $V_S$, $R_{ref}$)** | | | | | | |
| $V_P$ | supply voltage range | | 5.65 | – | 11.5 | V |
| $V_{PC}$ | clamping voltage | $I_{PC}$ = 10 mA | 11.5 | – | 12.8 | V |
| $V_{PS}$ | start voltage | | 6.1 | 6.4 | 6.7 | V |
| $V_{PLSP}$ | low supply protection level | | 4.85 | 5.25 | 5.65 | V |
| $V_{PLSPH}$ | hystereris of $V_{PLSP}$ | | 0.5 | 0.95 | – | V |
| $I_P$ | supply current | outputs off | – | – | 4.3 | mA |
| $I_{PP}$ | supply pause current | $V_P$ = 6 V | – | – | 1.71 | mA |
| $I_{PSB}$ | standby current | $V_P$ = 4 V | – | 35 | 45 | µA |
| $V_S$ | source voltage (stabilized) | $I_S$ = 1 mA | 4.03 | 4.25 | 4.46 | V |
| $V_{ref}$ | reference voltage | $I_{ref}$ = 20 µA | 1.18 | 1.25 | 1.31 | V |
| TC | temperature coefficient of $V_{ref}$ | $T_{amb}$= 0 to 45 °C | – | ±100 | ±200 | ppm/K |
| PSRR | power supply rejection ratio of $V_{ref}$ | f = 100 Hz; $dV_P$ = 2 V (p-p); $V_P$ = 8 V | –46 | – | – | dB |
| $\Delta V_{ref}$ | voltage difference | $dI_S$ = 1 mA | – | – | 5 | mV |
| $I_{Rref}$ | current range of $R_{ref}$ | | 10 | – | 100 | µA |
| **Charge current regulation (IB, $R_n$, $R_{ref}$)** | | | | | | |
| $V_n$ | voltage at pin $R_n$ | $I_n$ = 10 µA; $I_{ref}$ = 20 µA | 1.17 | 1.25 | 1.32 | V |
| $I_n$ | current range at $R_n$ | | 5 | – | 50 | µA |
| $I_{IB}/I_{ref}$ | input current ratio | $R_n$ not connected | | | | |
| | normal charging | $V_{IB}$ = 0 | 0.475 | 0.5 | 0.525 | |
| | fast charging | $V_{IB}$ = 0 | 0.95 | 1 | 1.05 | |
| $I_{IB}/I_n$ | input current ratio | $R_n$ connected | | | | |
| | normal charging | | 0.90 | 0.97 | 1.04 | |
| $V_{thIB}$ | threshold voltage at IB | | | | | |
| | $T_{amb}$ = 25 °C | | –2 | – | +2 | mV |
| | $T_{amb}$ = 0 to 45 °C | | –3 | – | +3 | mV |
| **NTC input** | | | | | | |
| $V_{NTCSPH}$ | switching protection voltage on high temperatures | | 0.75 | 0.81 | 0.87 | V |
| $V_{NTCHH}$ | hysteresis of $V_{NTCSPH}$ | | 60 | 90 | 120 | mV |
| $V_{NTCSPL}$ | switching protection voltage on low temperatures | | 2.78 | 3.00 | 3.20 | V |
| $V_{NTCHL}$ | hysteresis of $V_{NTCSPL}$ | | 65 | 100 | 135 | mV |
| $I_{NTC}$ | input current | $V_{NTC}$ = 2 V | –5 | – | +5 | µA |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Output drivers (AO, LS, PWM, LED)** | | | | | | |
| $I_{AOsource}$ | source current | $V_{AO}$ = 3 V; CP = 0 | – | – | –2 | mA |
| $I_{AOsink}$ | sink current | $V_{AO}$ = 0.5 V; CP = 1 | 2 | – | – | mA |
| $g_m$ | transconductance A1 | $V_{IB}$ = 50 mV | – | 300 | – | µS |
| $G_{v1}$ | voltage gain A1 x A2 | $V_{AO}$ = 2 V (p-p) | – | 72 | – | dB |
| $G_{v2}$ | voltage gain A2 | $V_{AO}$ = 2 V (p-p) | – | 12 | – | dB |
| $I_{LSsource}$ | maximum source current | $V_{LS}$ = 2.25 V | –25 | –21 | –16 | µA |
| $I_{LSsink}$ | maximum sink current | $V_{LS}$ = 2.25 V | 16 | 21 | 25 | µA |
| $I_{PWMH}$ | HIGH level output current | $V_{PWM}$ = 3 V | –18 | –14 | –10 | mA |
| $I_{PWML}$ | LOW level output current | $V_{PWM}$ = 0.5 V | 7 | 12 | 17 | mA |
| $I_{PWMleak}$ | leakage current | $V_{PWM}$ = 4.25 V | – | 0.2 | 10 | µA |
| $\delta_{PWM}$ | maximum duty cycle | | 70 | 78 | 86 | % |
| $\delta_{PWMaux}$ | auxiliary pulse duty cycle | | 12.6 | 14 | 15.4 | % |
| $V_{LEDsat}$ | saturation voltage | $I_{LED}$ = 15 mA | – | – | 600 | mV |
| $I_{LEDleak}$ | leakage current | $V_{LED}$ = 10 V | – | – | 5 | µA |
| **Battery monitor (VAC)** | | | | | | |
| $I_{VAC}$ | input current | $V_{VAC}$ = 4.25 V | – | 1 | – | nA |
| $V_{VAC}$ | voltage range of –dV detection | | 0.385 | – | 3.85 | V |
| $dV_{VAC}/V_{VAC}$ | –dV detection level w.r.t. top level | $V_{VAC}$ = 2 V | – | 0.25 | – | % |
| $\Delta V_{VAC}$ | resolution –dV | | 0.42 | 0.6 | 0.78 | mV |
| $T_{-dV}$ | temperature range of –dV detection | | 0 | – | 50 | °C |
| **Protections (VAC)** | | | | | | |
| $V_{VACLBP}$ | low battery voltage protection | | – | 0.3 | 0.33 | V |
| $V_{VACHBP}$ | high battery voltage protection | with respect to $V_P$ | – | 0 | 150 | mV |
| **Oscillator, logic (OSC, SYNCH)** | | | | | | |
| $V_{OSCH}$ | oscillator switching level HIGH | | – | 2.5 | – | V |
| $V_{OSCL}$ | oscillator switching level LOW | | – | 1.5 | – | V |
| K | period time | $T_{OSC} = K \times R_{ref} \times C_{OSC}$ | 0.84 | 0.93 | 1.02 | |
| $f_{OSC}$ | oscillator frequency range | | 10 | – | 100 | kHz |
| $V_{SYNCH}$ | SYNC output level HIGH | $I_{SYNCH}$ = –0.4 mA | 3.4 | – | – | V |
| $V_{SYNCL}$ | SYNC output level LOW | $I_{SYNCL}$ = 0.4 mA | – | – | 0.85 | V |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Programming (CP)** | | | | | | |
| $I_{CP}$ | programming currents | | | | | |
| | CP = 0; aux = 0 | $R_{CP}$ = 330 kΩ | – | – | 4.2 | µA |
| | CP = 0; aux = 8 | $R_{CP}$ = 120 kΩ | 9.4 | 10.4 | 11.4 | µA |
| | CP = 1; aux = 0 | $R_{CP}$ = 56 kΩ | 20.0 | 22.3 | 24.5 | µA |
| | CP = 1; aux = 8 | $R_{CP}$ = 22 kΩ | 51.1 | 56.8 | 62.5 | µA |

**QUALITY SPECIFICATION**

General quality specification for integrated circuits: UZW-B0/FQ-0601.

Note: For the synchronization pin (14), the ESD positive zap voltage is restricted to a maximum of 1000 V.

## TEST AND APPLICATION INFORMATION

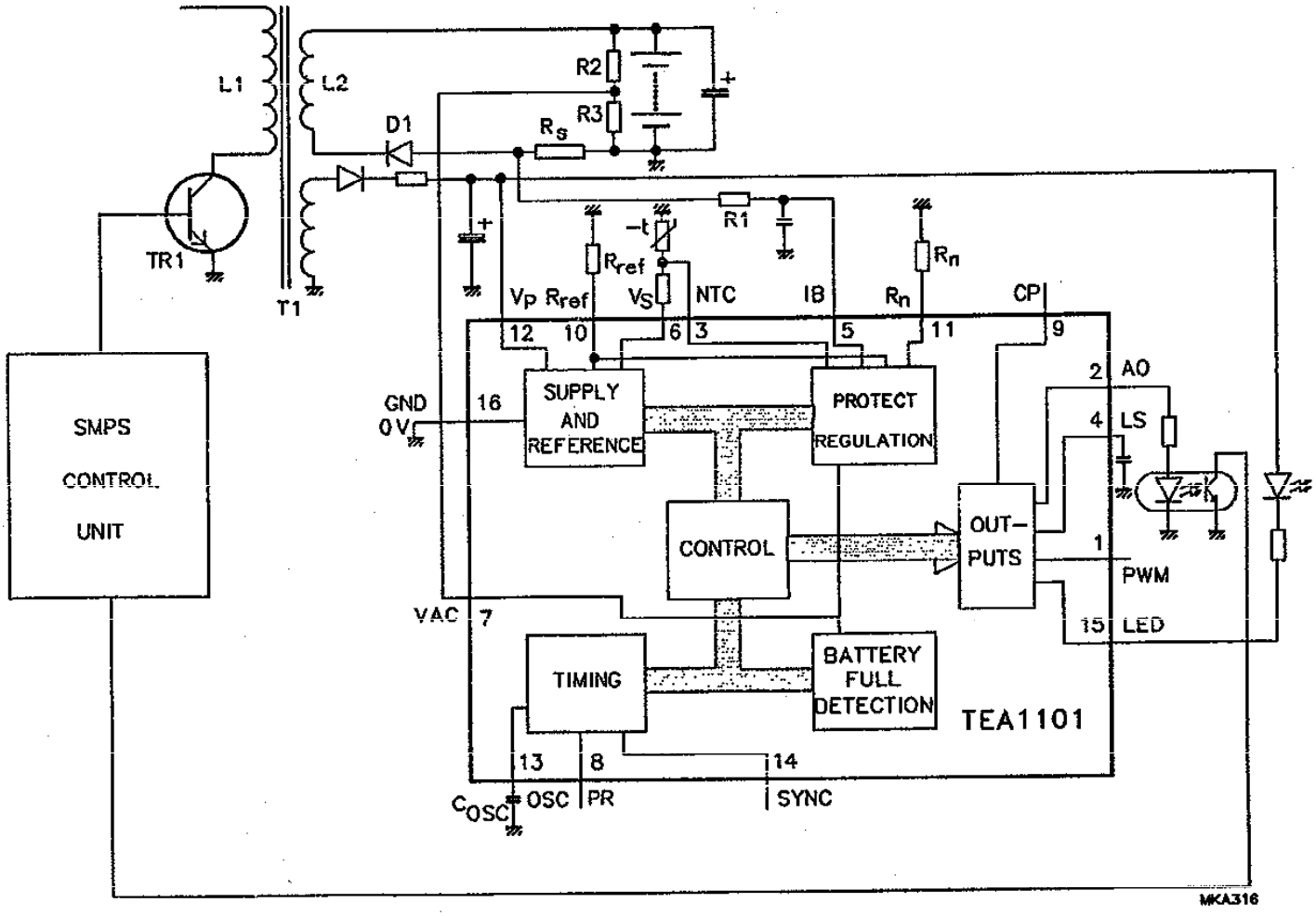



Fig.3 Application diagram.

### Notes to Fig.3

1. Signaling the status of the charging session can be achieved by an LED-diode-resistor combination parallel to L2 (transformer T1). During the fast charging period the LED will burn continuously. During normal charging the LED will switch with the 10/90% rhythm. With mains-off the LED is off, thus not discharging the batteries. If at normal charging the duty cycle is too low during the 10% because of a very large difference between the fast charge and the normal charge levels, the LED can be driven by the LED pin.
2. With $R_s$ = 50 MΩ and a required fast charging current level of 6 A (5C for 1.2 Ah batteries), the average current sense level is 300 mV. Power dissipation in $R_s$ = 1.8 W.

   With a 3 kΩ resistor for R1, the required $I_{ref}$ current is 300 mV/3 kΩ = 100 µA. For a normal charge level of 0.25C (300 mA) the voltage drop over $R_s$ is 15 mV. Taking into account the duty cycle of 10%, the voltage drop over R1 = 150 mV. Thus the $I_{Rn}$ current has to be 150 mV/3 kΩ = 50 µA (p = 1).

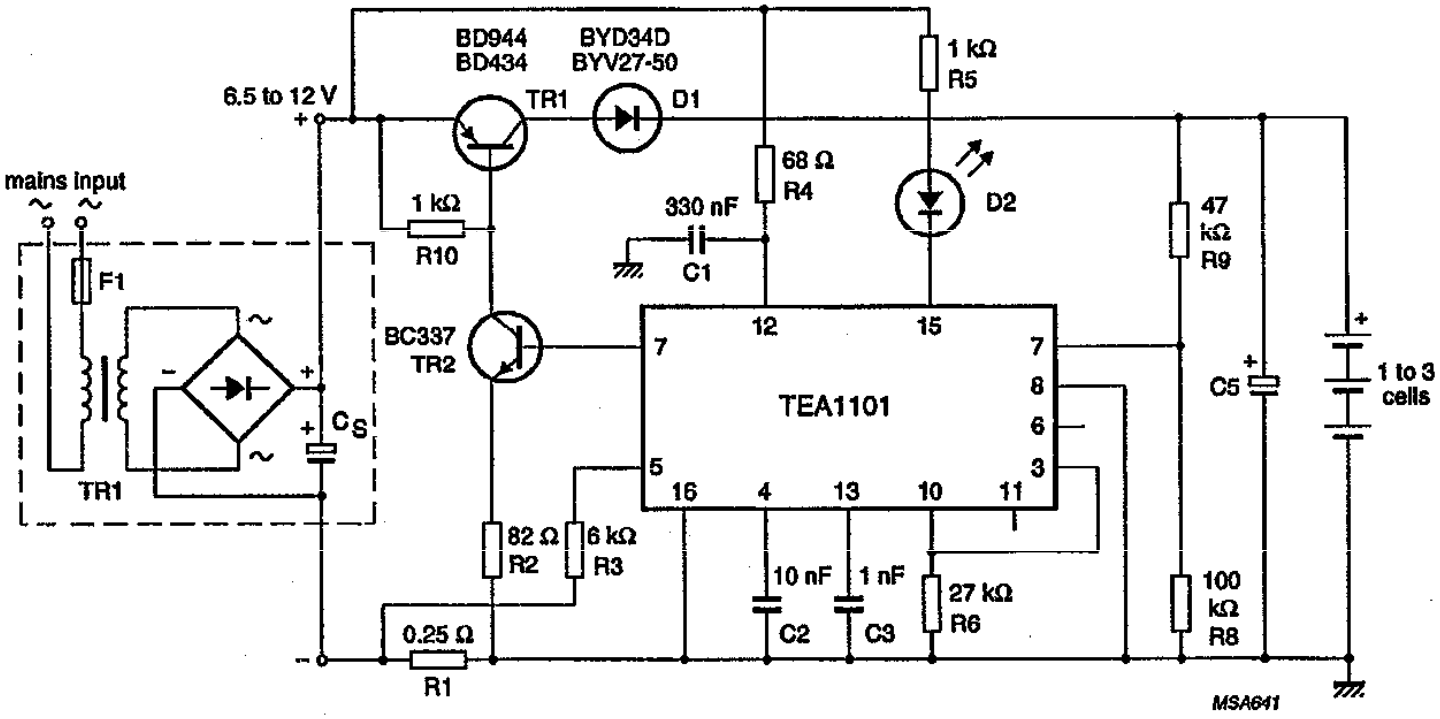



Fig.4 Battery charger with linear regulator.

### Method to increase –dV sensitivity

The basic, direct battery sensing via a resistive divider, which adapts the battery voltage within the $V_{AC}$ range, is shown in Fig.7. Detection occurs at $-dV = 0.25\%$ of $V_{B(max)}$.

The position of the Zener diode is shown in Fig.8. The TEA1101 now senses the voltage $V_R$, which is the battery voltage minus the Zener-diode voltage ($V_R = V_B - V_Z$).

Detection occurs at $-dV_R = 0.25\%$ of $V_{Rmax}$. If the Zener voltage is half the maximum battery voltage, the $dV_B$ detection will be at –0.125%.

### Design example for six-cell battery and 0.125% –dV cut-off

Conditions:

- Maximum battery voltage (1.7 V/cell) = 10.2 V
- Sense network current ≈ 300 µA
- Maximum monitor sense voltage $V_{AC} = 3.6$ V (< 3.85 V).

For $-dV \approx 0.125\%$, a Zener voltage of about half the battery voltage is required; choose $V_Z = 5$ V. Now $V_R$ at top level is ≈ 5.2 V and the required divider factor ($V_{AC}/V_R$) is 0.69. R1 and R2 become 5.6 kΩ and 12 kΩ respectively (see Figs 6 and 7).

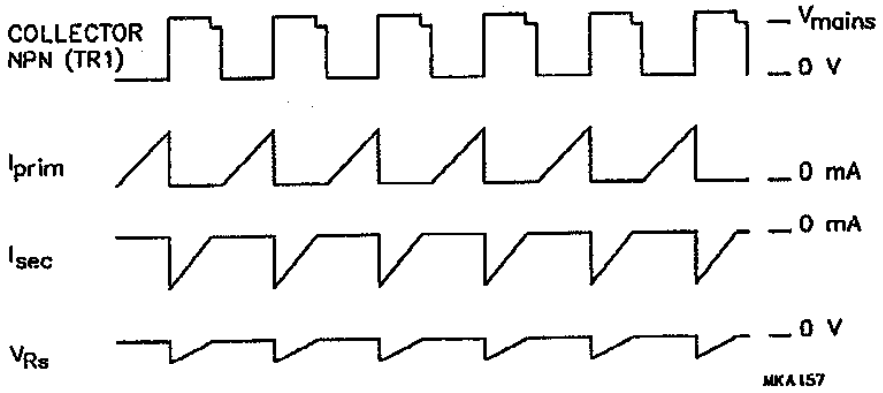



Fig.5 SMPS voltage and current waveforms.

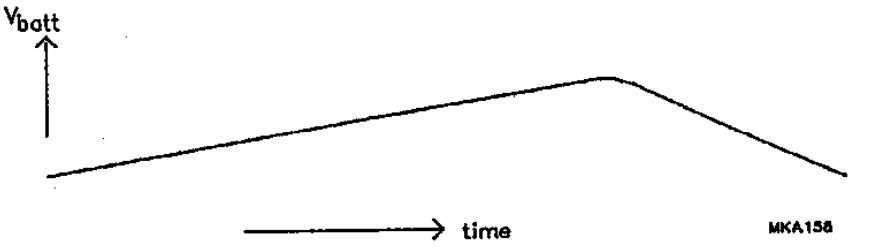



Fig.6 Battery voltage during charging.

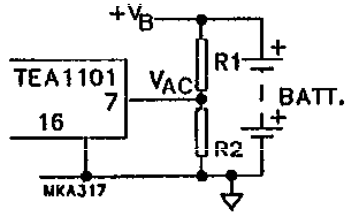



Fig.7 Basic circuit for direct battery sensing.

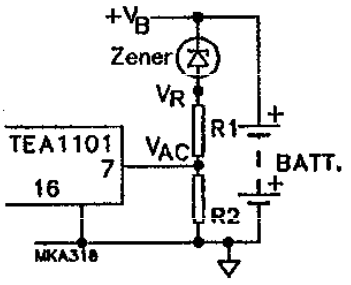



Fig.8 Basic circuit showing the use of a Zener diode.

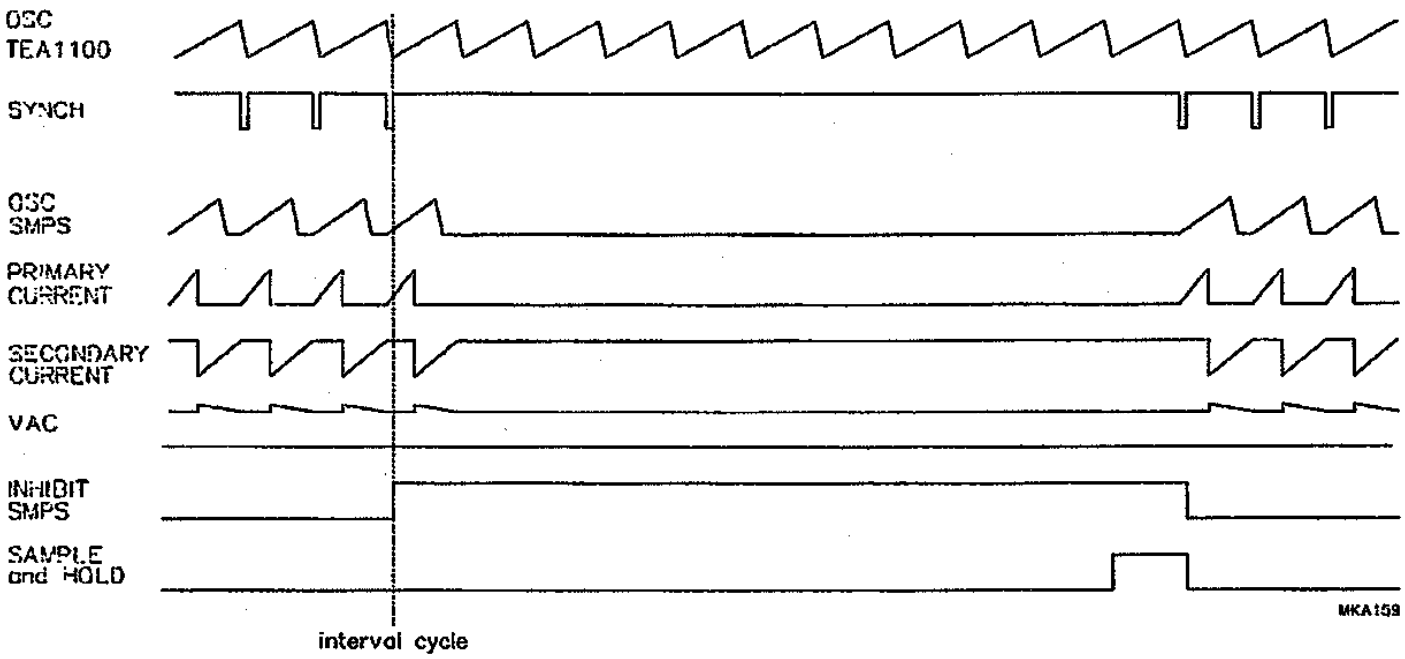
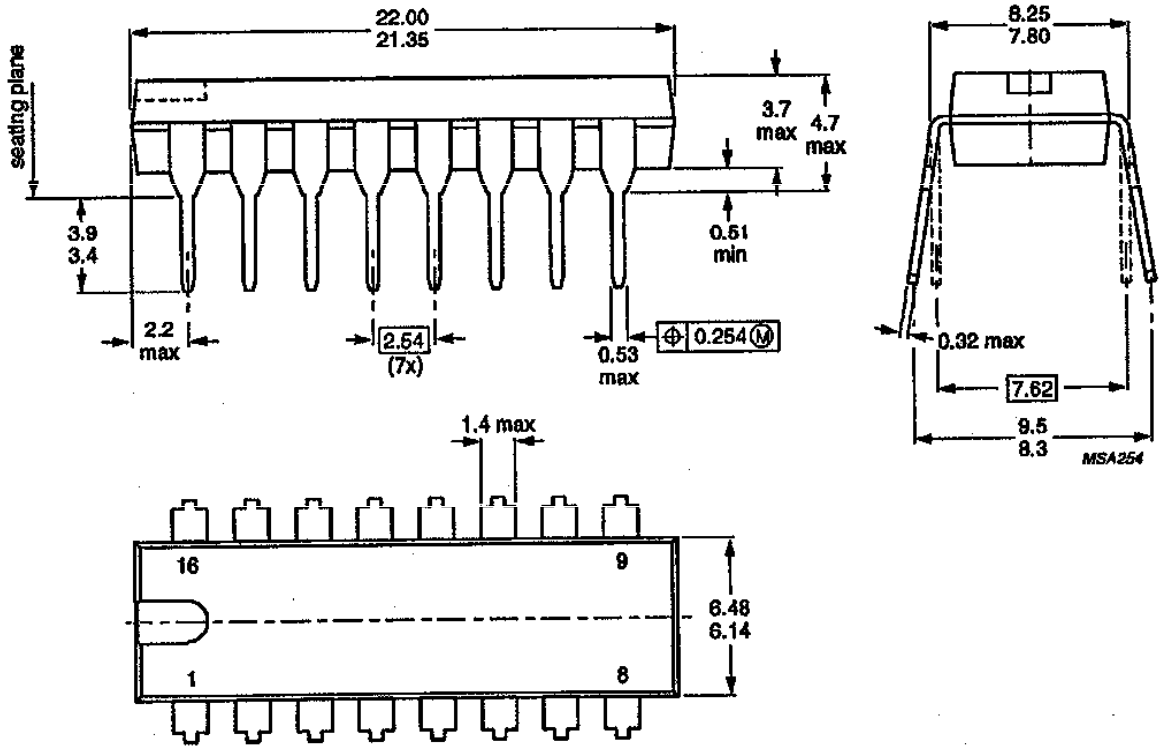


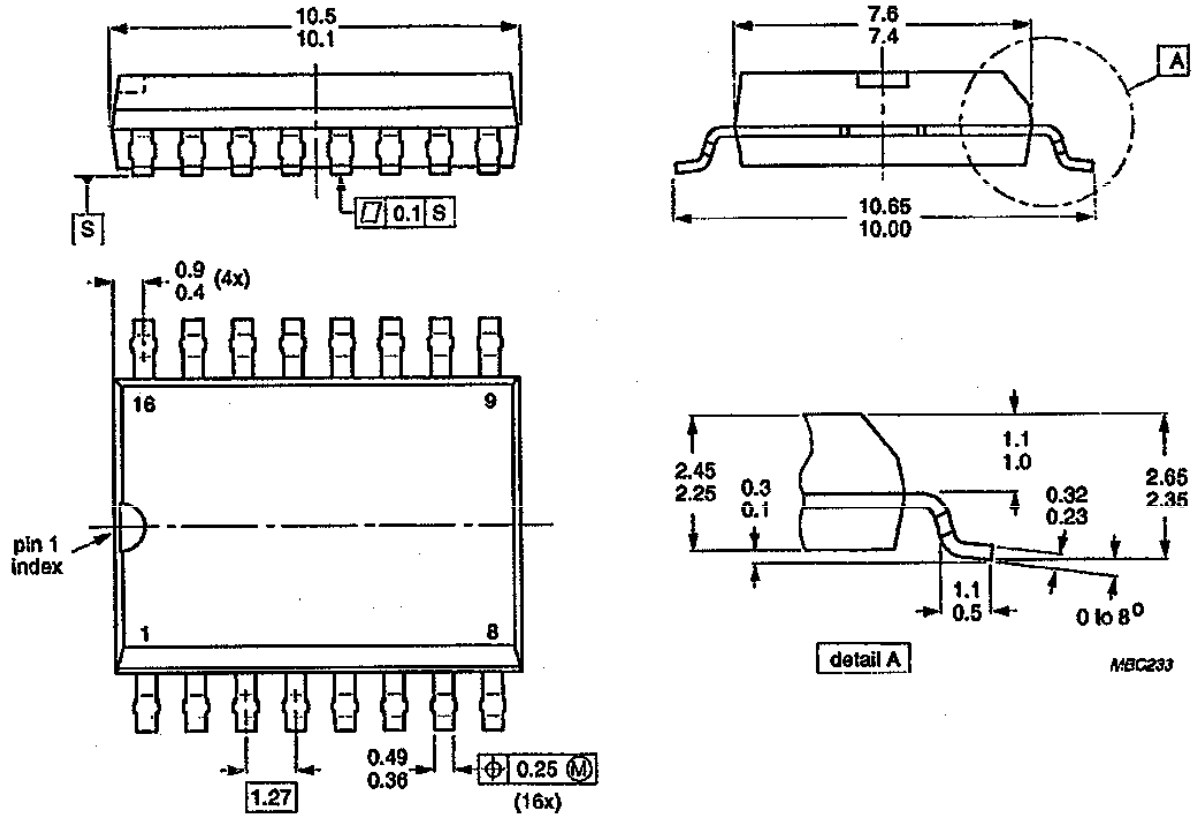

Fig.9 Synchronization waveforms.

## 'ACKAGE OUTLINES




Dimensions in mm.

Fig.10 16-lead dual in-line; plastic (SOT38G).




Dimensions in mm.

Fig.11 16-lead mini-pack; plastic (SO16L; SOT162A).

## SOLDERING

### Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

## SOLDERING

### Plastic mini-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.