PORTABLE PENTIUM® II & III POWER SUPPLY CONTROLLER

PRELIMINARY - August 27, 1999

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DESCRIPTION

The SC1406 is a High Speed, High performance Hysteretic Mode controller. It is part of a two chip solution, with the SC1405 Smart Driver, providing power to advanced micro-processors. It uses a Dynamic Set Point switching technique along with an ultra-fast comparator to provide the control signal to an external high speed Mosfet driver. A 5-bit DAC sets the output voltage, thus providing a voltage resolution of 25mV.

SC1406 has two on-chip linear regulators which drive external PNP transistors with output voltage settings of 1.5V and 2.5Vdc. The linear regulator drivers have a separate soft start. A PWRGD TTL level signal is asserted when all voltages are within specifications. The part features Low Battery Detect and Undervoltage Lock-Out for the main Hysteretic controller to assure V-DC is within acceptable limits. An Over-Current comparator disables the main controller during an overcurrent condition using an externally programmable threshold.

FEATURES

- High Speed Hysteretic controller provides high efficiency over a wide operating load range
- Inherently stable
- Complete power solution with two LDO drivers
- Programmable output voltage for Pentium® II & III Processors

APPLICATIONS

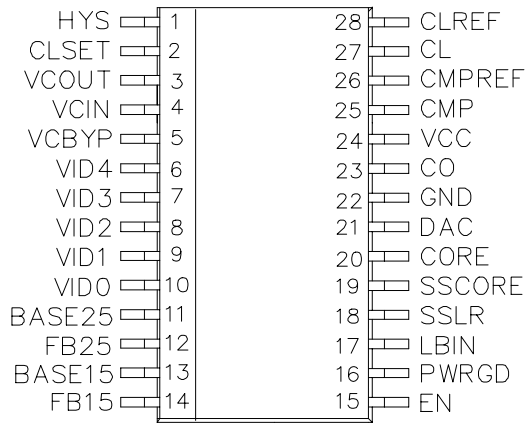
- Laptop and Notebook computers
- High performance Microprocessor based systems
- High efficiency distributed power supplies

ORDERING INFORMATION

DEVICE	PACKAGE	TEMP. (T_J)
SC1406TS	TSSOP-28	0 - 125°C

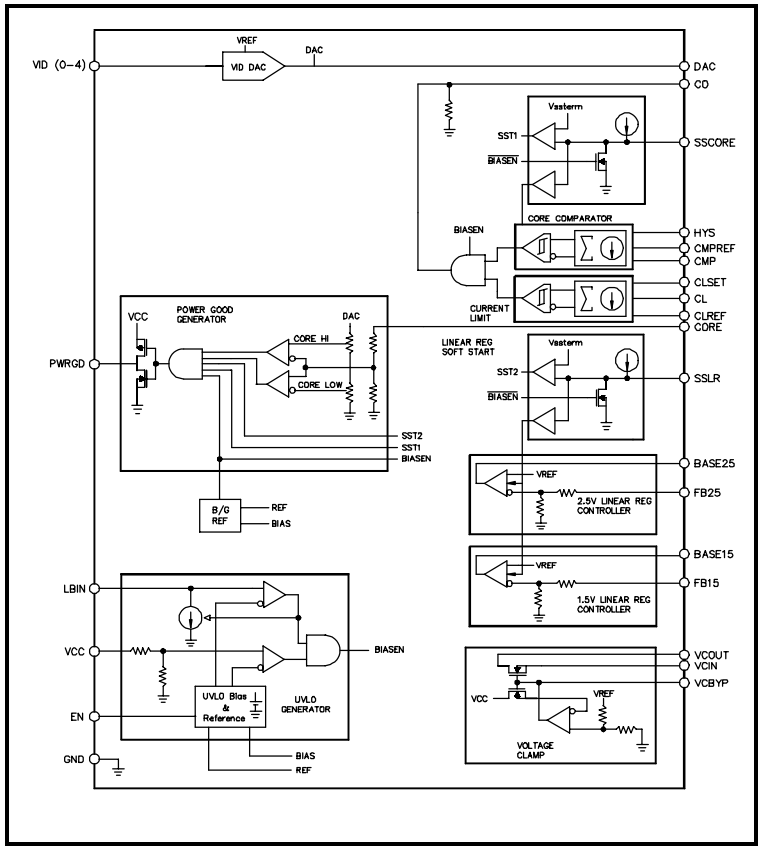
PIN CONFIGURATION

Top View



TSSOP-28

BLOCK DIAGRAM



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PIN DESCRIPTION:

Pin	Pin Name	Pin Function
1	HYS	Core comparator hysteresis settling.
2	CLSET	Current limit setting pin.
3	VCOUT	Voltage clamp output.
4	VCIN	Voltage clamp input.
5	VCBYP	Voltage clamp bypass pin.
6	VID4	VID most significant bit input.
7	VID3	VID input
8	VID2	VID input
9	VID1	VID input
10	VID0	VID least significant bit input.
11	BASE25	2.5V Linear regulator drive.
12	FB25	2.5V Linear regulator output feedback.
13	BASE15	1.5V Linear regulator drive.
14	FB15	1.5V Linear regulator output feedback.
15	EN	Enables the IC when high. This is capable of accepting 5.0V signal level.
16	PWRGD	When the main converter output is within +10% of the VID DAC setting, this signal is driven high to VCC level. Internal pull-down 100K.
17	LBIN	Low battery input. This pin is used to set the minimum voltage to the converter. When the input to this pin is less than 1.225V, the converter is held in an Under-Voltage-Lock-Out mode regardless of the status of EN.
18	SSLR	Linear regulators soft start. During power-up, the external soft-start capacitor (1200pF, typ) is charged by an internal 1µA current source to set the ramp up time of the linear regulator outputs, 1.5V and 2.5V. This ramp up time is typically 2ms, 6ms max. This is discharged when BIASEN (internal signal) is low.
19	SSCORE	Main controller output soft start. During power-up, the external Soft-Start capacitor (1800pF, typ) is charged by an internal 1µA current source to set the ramp up time of the main converter output. This ramp up time is typically 3ms, 6ms max. This is discharged when BIASEN is low. Core soft start current tolerance tracks the LDO soft start current to within 10%.
20	CORE	Converter output feedback.
21	DAC	VID digital to analog output.
22	GND	Ground
23	CO	Comparator output. Main regulator controller output. Internal pull-down 100K.
24	VCC	Supply voltage.
25	CMP	Core comparator input pin.
26	CMPREF	Core comparator reference input pin.
27	CL	Current limit input pin.
28	CLREF	Current limit reference input pin.

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MAXIMUM	UNITS
VCC Supply Voltage	$Vmax_{VCC}$	7	V
Low Battery Input	LBIN	7	V
Input & Output Pins		V_{CC} + 0.3 GND - 0.3	V
Enable	EN	7	V
Operating Junction Temperature	T_J	0 to +125	°C
Lead Temperature (Soldering) 10 seconds	T_L	300	°C
Storage Temperature	T_{STG}	-65 to 150	°C

ELECTRICAL CHARACTERISTICS

Unless specified: $0 < T_A < 100°C$; V_{CC} = 3.3V (See Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY, BIAS, UVLO, VDC MONITOR AND POWERGOOD						
Supply (VCC, GND)						
VCC Supply Voltage Range	V_{CCMAX}		3.0	3.3	6.0	V
VCC Quiescent Current	I_{CCQ}	EN is low, $3.0V \le V_{CC} \le 3.6V$			10	µA
		EN is high and in UVLO			350	
VCC Operating Current	I_{CC}	EN is high		10.0	15	mA
Under Voltage Lock Out Circuit						
Threshold	V_{HCC}				2.95	V
	V_{LCC}		2.7			
Hysteresis	V_{HYSTCC}		20			mV
Enable Input						
Input High	Vih	$3.0 \le V_{CC} \le 5V$	$0.7*V_{CC}$			V
Input Low	Vil				0.8	V
Low Battery Monitor						
Threshold	V_{THDC}		1.175	1.225	1.275	V
Input Bias Current	I_{BDC}	$V_{LB\_IN} > V_{THDC}$			±0.3	µA
		$V_{LB\_IN} < V_{THDC}$	0.6	1.0	10.5	
VCORE Power Good Generator						
Input Threshold	V_{HCORE}	V_{DAC} = 0.9V - 1.675V	$1.08*V_{CC}$		$1.12*V_{CC}$	V
	V_{LCORE}		$0.88*V_{CC}$		$0.92*V_{CC}$	V
Output Voltage	V_{HPWRGD} (Active Hi)	I_{PWRGD} = 10µa (source) EN is high	$0.95*V_{CC}$			V
	V_{LPWRGD} (Active low)	I_{PWRGD} = 10µA (sink), EN is high			0.4	V
	V_{PWRGD}	I_{PWRGD} = 10µA (sink), UVLO			0.8	V
	V_{OUT}	During the latency time (50µs) of any VID code change		Don't care		

Note 1: Specification refers to application circuit (Figure 1.).

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ELECTRICAL CHARACTERISTICS (CONT.)

Unless specified: -0 < T_A < 100°C; V_{CC} = 3.3V (See test circuit)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CORE CONVERTER CONTROLLER						
Core Converter Soft Start Current						
Core Converter Soft Start Current	I_{SSCORE}	Charge (Source) current	0.6	1	1.45	µA
		Discharge (Sink) current	0.30	1		mA
V_{SSCORE} Soft Start Termination Threshold	V_{SSTERM}		1.53	1.70	1.87	V
V_{SSCORE} Discharge Threshold	V_{SSDIS}			150	400	mV
VID DAC						
VID Input Threshold	V_{VID_IH}	3.0V < V_{CC} < 3.6V	0.7*V_{CC}			V
	V_{VID_IL}				0.8	
VID Input-Pull-up Current,VID (0-4)	I_{VID}	VID (0-4) = 00000...11111	6		40	µA
Output Voltage Accuracy	V_{DAC_ERR}	I_{DAC} = 0, VID(0-4) = 00000...11111	-0.85		+0.85	%
Settling Time*	t_{pdVID_DAC}	C_{DAC} = 1000pF VID is set to change VCORE from 1.30V to 1.45V or 1.45V to 1.30V			35	µs
CORE Comparator (CMP, CMPREF, HYS, CO)						
Input Bias Current	I_{BCMP}	V_{CMP} = V_{CMPREF} = 1.3V			±2	µA
Input Offset Voltage	$V_{CPM-VCPMREF}$	V_{CMPREF} = 1.3V		±1.5	±3	mV
Hysteresis Setting Current	I_{CMPREF}	R_{HYS} = open			±2	µA
		R_{HYS} = 17kΩ	±89	±100	±111	
		R_{HYS} = 170kΩ	±8	±10	±12.5	
Output Voltage	$V_{HCO\ CMP<CMPREF}$	Load Impedance = 100k in parallel with 10pF, V_{CC} = 3.0V	2.5			V
	$V_{LCO\ CMP>CMPREF}$	Load Impedance = 100k in parallel with 10pF, V_{CC} = 3.6V			0.4	V
Propagation Delay Time** Measured at device pins, from the trip point to 50% of CO transition.	$T_{pd\ CMP-CO}$	V_{CMPREF} = 1.3V Δ V_{CMP} = +40mV step with +20mV, overdrive T_A = 25°C, T_A = full range			20 30	ns
		V_{CMPREF} = 1.3V Δ V_{CMP} = 40mV step with 20mV overdrive, T_A = 25°C, T_A = full range			20 30	
Output Rise/Fall Times** Measured between 30% and 70% points of CO transition	T_R	C_{CO} = 10pF V_{CC} = 3.0V		7	10	ns
	T_F	R_{CO} = 100K		7	10	

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ELECTRICAL CHARACTERISTICS (CONT.)

Unless specified: -0 < T_A < 100°C; V_{CC} = 3.3V (See test circuit)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current Limit Comparator (CL, CLREF, CLSET)							
Input Bias Current	$\pm I_{CL}$	V_{CS} = 1.3V				5	µA
Current Limit Setting Current *The Tamky device is required to meet the CL setting current requirements for R_{CLSET} of "17kΩ and 170kΩ or "42.5kΩ and 20kΩ". Supplier production testing will use the 17kΩ /170kΩ combination or the 42.5kΩ /20kΩ combination.	$\lvert\pm I_{CLREF}\rvert$	R_{CLSET} = open	V_{CLREF}-V_{CL} = 10mV			7.5	µA
			V_{CLRER}-V_{CL} = -10mV			5.0	
		R_{CLSET} = 17kΩ*	V_{CLREF}-V_{CL} = 10mV	262.5	300	337.5	µA
			V_{CLREF}-V_{CL} = -10mV	175	200	225	
		R_{CLSET} = 170kΩ*	V_{CLREF}-V_{CL} = 10mV	19.5	30	40.5	µA
			V_{CLREF}-V_{CL} = -10mV	13	20	27	
		R_{CLSET} = 42.5kΩ*	V_{CLRER}-V_{CL} = 10mV	100.5	120	139.5	µA
			V_{CLRER}-V_{CL} = -10mV	67	80	93	
		R_{CLSET} = 20kΩ*	V_{CLREF}-V_{CL} = 10mV	222	255	288	µA
			V_{CLRER}-V_{CL} = -10mV	148	170	192	
Input Offset Voltage	V_{CL} - V_{CLREF}	V_{CLREF} = 1.3V			±4	±6	mV
Propagation Delay Time** Measured at the device pins, from the trip point to 50% of CO transition	T_{pd_CL-CO}	V_{CMPREF} = 1.3V, Δ V_{CMP} = +50mV step with +20mV overdrive, T_A = 25°C,				100	ns
		T_A = full range				150	
		V_{CMPREF} = 1.3V, Δ V_{CMP} = -50mV step with -20mV overdrive, T_A = 25°C,				100	
		T_A = full range				150	

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ELECTRICAL CHARACTERISTICS (CONT.)

Unless specified: -0 < T_A < 100°C; V_{CC} = 3.3V (See test circuit)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
LINEAR REGULATOR CONTROLLERS							
1.5V Linear Regulator Controller							
Input Bias Current	I_{LR15}	V_{FB_15} = 1.5V				1	mA
Output Voltage $C_{O\_1.5}$ = 56µF, 20mΩ ESR max or 150µF, 45mΩ ESR max Capacitance tolerance = 20%	$V_{O\_1.5}$, Imin = 0.1mA	I_O = 500mA, pnp BJT with $B_{MIN} \geq 50$ @ I_C = 500mA		1.47	1.50	1.54	V
Base Drive Output Current	$I_{BASE\_1.5}$	@ 25°C		10		120	mA
2.5V Linear Regulator Controller							
Input Bias Current	I_{LR25}	V_{FB_25} = 2.5V				1	mA
Output Voltage $C_{O\_2.5}$ = 1µFceramic ESR range = 1mΩ – 30mΩ Capacitance tolerance = 20%	$V_{O\_2.5}$, Imin = 0A Imax=0.1A	I_O = Imax, pnp BJT with $B_{MIN} \geq 50$ @ I_C = 100mA		2.45	2.50	2.55	V
Base Drive Output Current	$I_{BASE\_2.5}$			3.5		20	mA
Linear Regulator Soft Start (LRSS)							
Linear Reg Soft-Start Current	I_{LRSS}	Charge Current, V_{LRSS} = 0V		-0.6	-1	-1.4	µA
		Discharge Current, V_{LRSS} = 1.50V, EN is low or in UVLO		0.3	1	1.45	mA
Enable Threshold	V_{SSLR_EN}				150	400	mV
Soft Start Termination Threshold	V_{TH_LRSS}			1.53	1.70	1.87	V
Voltage Clamp (VCIN, VCOUT, VCBYP)							
Input Voltage	V_{H_VCIN}			0.95	1.5	1.60	V
Output Voltage Imin = 10µA	V_{H_VCOUT}	R_{VCOUT} = 150Ω tied to V_S = 2.5V I_{VCIN} = -10µA	VCIN is open	$0.8V_S$		V_S	V
	V_{L_VCOUT}		V_{VCIN} = 0.175V			0.375	
Progagation Delay**	$T_{pd\ VCIN\_VCOUT}$	R_{VCOUT} = 150Ω tied to V_S = 2.5V C_{VCBYP} = 1500pF, VCIN steps from 0.175V to 1.50V and back. Measured from 50% of VCIN step to 50% of VCOUT transient				10	ns

* Guaranteed by design.
**Guaranteed by characterization.

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VID vs. V_{DAC} VOLTAGE

VID					MIN	TYP	MAX
4	3	2	1	0	1% < V_O	V_O	1% > V_O
0	0	0	0	0	1.658	1.675	1.692
0	0	0	0	1	1.633	1.650	1.666
0	0	0	1	0	1.609	1.625	1.641
0	0	0	1	1	1.584	1.600	1.616
0	0	1	0	0	1.560	1.575	1.591
0	0	1	0	1	1.534	1.550	1.565
0	0	1	1	0	1.510	1.525	1.540
0	0	1	1	1	1.485	1.500	1.515
0	1	0	0	0	1.460	1.475	1.490
0	1	0	0	1	1.435	1.450	1.464
0	1	0	1	0	1.411	1.425	1.439
0	1	0	1	1	1.386	1.400	1.414
0	1	1	0	0	1.361	1.375	1.389
0	1	1	0	1	1.336	1.350	1.363
0	1	1	1	0	1.312	1.325	1.338
0	1	1	1	1	1.287	1.300	1.313
1	0	0	0	0	1.262	1.275	1.288
1	0	0	0	1	1.237	1.250	1.262
1	0	0	1	0	1.213	1.225	1.237
1	0	0	1	1	1.188	1.200	1.212
1	0	1	0	0	1.163	1.175	1.187
1	0	1	0	1	1.138	1.150	1.161
1	0	1	1	0	1.114	1.125	1.136
1	0	1	1	1	1.089	1.100	1.111
1	1	0	0	0	1.064	1.075	1.086
1	1	0	0	1	1.039	1.050	1.060
1	1	0	1	0	1.015	1.025	1.035
1	1	0	1	1	0.99	1.00	1.01
1	1	1	0	0	0.965	0.975	0.984
1	1	1	0	1	0.940	0.950	0.959
1	1	1	1	0	0.916	0.925	0.934
1	1	1	1	1	0.891	0.900	0.909

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FUNCTIONAL DESCRIPTION

SUPPLY

The chip is optimized to operate from a 3.3V ± 5% rail but is also designed to work up to 6V maximum supply voltage. If V_{CC} is out of the 3.3V ± 5% voltage range, the quiescent current will increase somewhat and slight degradation of line regulation is expected.

UNDER VOLTAGE LOCK-OUT CIRCUIT

The under voltage lockout circuit consists of two comparators, the low battery and low V_{CC} (low supply voltage) comparators. The output of the comparator gated with the Enable signal turns on or off the internal bias, enables or disables the CO output, and initiates or resets the soft start timers.

POWER GOOD GENERATOR

If the chip is enabled but not in UVLO condition, and the core voltage gets within ±10% of the VID programmed value, then a high level Power Good signal is generated on the PWRGD pin to trigger the CPU power up sequence. If the chip is either disabled or enabled in UVLO condition, then PWRGD stays low. This condition is satisfied by the presence of an internal 100kΩ pull-down resistor connected from PWRGD to ground.
During soft start, PWRGD stays low independently from the status of Vcore voltage. During this time, PWRGD status is "don't care".

BAND GAP REFERENCE

A better than ±1% precision band gap reference acts as the internal reference voltage standard of the chip, which all critical biasing voltages and currents are derived from.

CORE CONVERTER CONTROLLER

Precision VID DAC Reference

The 5-bit digital to analog converter (DAC) serves as the programmable reference source of the core comparator. Programming is accomplished by CMOS logic level VID code applied to the DAC inputs. The VID code vs. the DAC output is shown in the Output Voltage Table. The accuracy of the VID DAC is maintained on the same level as the band gap reference. There is a 10µA pull-up current on each DAC input while EN is high.

Core Comparator

This is an ultra-fast hysteretic comparator with a typical propagation delay of approximately 20ns at a 20mV overdrive. Its hysteresis is determined by the resistance ratio of two external resistors, R_{HYS} and R_{OH}, and the high accuracy internal reference voltage, V_{REF}.

$$V_{HYS} = \frac{R_{OH}}{R_{HYS}} \quad V_{REF} = 1.7V$$

This chip can be used in standard hysteretic mode controller configuration and in DSPS (Dynamic Set Point Switching) hysteretic controller scheme.

In standard hysteretic controller configuration, the core comparator compares the output voltage of the core converter, V_{CORE} to the VID code programmed DAC voltage, V_{DAC}.

$$V_{CORE}(t) = V_{DAC} + V_{HYST}(t)$$

The core voltage ramps up and down between the two thresholds determined by the hysteresis of the comparator:

$$V_{HCORE} = V_{DAC} + V_{HYST}$$
$$V_{LCORE} = V_{DAC} - V_{HYST}$$

In DSPS hysteretic controller configuration, the core comparator compares the core voltage, V_{CORE}, not to the DAC voltage, V_{DAC} directly but rather to a voltage less than the DAC voltage by a DSPS voltage,

$$V_{DSPS}.V_{CORE}(t) = V_{DAC} - V_{DSPS}(t) + V_{HYST}(t)$$

The DSPS voltage is a function of the load current. It is generated from the current sense voltage, V_{CS}, developed across a sense resistor, $R_{CS,}$ which is inserted in series with the main buck inductor and also used for current sensing for the cycle-by-cycle current limiting. The sense voltage is scaled up by the DSPS gain, A_{DSPS}, which is set by the resistance ratio of two external resistors, R_{DAC} and R_{CORE}.

$$V_{DSPS}(t) = A_{DSPS} \bullet V_{CS}(t) = \left(1 + \frac{R_{DAC}}{R_{CORE}}\right) \bullet R_{CS} \bullet i_{CORE}(t)$$

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In DSPS hysteretic controller configuration (Cont'd)

The comparator reference voltage positioning is such that an increasing current sense voltage, VCS, i,e, an elevating load current, causes the reference voltage to decrease, and as a consequence, the core output voltage also droops. At no load current, there is no droop while a maximum load, the droop is likewise maximum.

In order for the core voltage to be positioned around the nominal V_{DAC} voltage symmetrically and not just one way downward from the nominal value, a DSPS offset voltage, $V_{DSPSOFFS}$, can be introduced. The offset voltage moves the comparator reference voltage upward at no load. At optimal offsetting, the reference voltage is above the nominal level for load currents less than half of the maximum load, and below the nominal value for currents higher than that. The maximum amount of core voltage positioning can be determined from the constrain which says the output voltage at no load condition must still remain below the upper threshold of the core voltage regulation window, and at maximum load, it must be above the lower threshold.

The offset voltage can be generated across a resistor, R_{OH}, which is also used to create the hysteresis voltage by forcing a unipolar DSPS offsetting current through it. The offsetting current is conveniently provided by a high value resistor, R_{OFFSET}, connected from the comparator CMP pin to the ground.

$$V_{DSPSOFFS} = R_{OH} \cdot I_{DSPS} = R_{OH} \bullet \frac{V_{CS} + V_{CORE}}{R_{OH} + R_{OFFSET}}$$

$$VCS << VCORE, VCORE = VDAC, ROH << ROFFSET \approx \frac{R_{OH}}{R_{OFFSET}} \bullet V_{DAC}$$

In DSPS hysterestic controller configuration, the comparator thresholds can be calculated from the DAC voltage, V_{DAC}, the DSPS offsetting voltage, $V_{DSPSOFFS}$, the DSPS voltage V_{DSPS}, and the bipolar hysteresis voltage, V_{HYST} by summing them at the comparator inputs at the appropriate load current levels:

$$Vcore := \frac{Vdac \bullet (Roffset + Roh) \bullet Rcore - Rcs \bullet Icore \bullet Roffset \bullet (Rcore + Rdac}{Rcore \bullet Roffset - Rdac \bullet Roh}$$

$$\Delta Vcore := 2 \bullet Vhys \bullet \frac{Rcore \bullet (Roffset + Roh)}{Rcore \bullet Roffset - Rdac \bullet Roh} \bullet \frac{Resr}{Resr + \frac{Rcore \bullet (Roffset + Roh)}{Rcore \bullet Roffset - Rdac \bullet Roh}}$$

Core Voltage Offsetting

In order for the core voltage to be positioned around the nominal V_{DAC} voltage symmetrically and not just always one direction downward, a core offset voltage, V_{OFFS} can be introduced. The offset voltage moves the comparator reference voltage upwards. Using optimal offsetting, the core comparator reference voltage will be above the VID programmed nominal DAC voltage for load currents less than half of the maximum load, and below that for higher current. The maximum amount of the core voltage positioning can be determined from the constraint that the output voltage regulation window, and at maximum load, it has to be above the lower threshold.

The positioning offset voltage can be generated across the same resistor, ROH also used to create the hysteresis voltage, by forcing a unipolar offsetting current through it. The offsetting current is conveniently provided by a high value resistor, ROFFS connected from the comparator CMP pin to the ground.

Current Limit Comparator

The current limit comparator monitors the core converter output current and turns the high side switch off when the current exceeds the upper current limit threshold, VHCL and re-enable only if the load current drops below the lower current limit threshold, VLCL. The current is sensed by monitoring the voltage drop across the current sense resistor, R_{CS}, connected in series with the core converter main inductor (the same resistor used for DSPS input signal generation). The thresholds have the following relationships:

$$V_{HCL} = 3 \bullet \frac{R_{CLOH}}{R_{CLSET}} \bullet V_{REF}$$

$$V_{LCL} = 2 \bullet \frac{R_{CLOH}}{R_{CLSET}} \bullet V_{REF}$$

$$V_{HYSCL} = \frac{R_{CLOH}}{R_{CLSET}} \bullet V_{REF}$$

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Core Converter Soft Start Timer
The main purpose of this block is to control the ramp-up time of the core voltage in order to reduce the initial inrush current on the core input voltage (battery) rail. The soft start circuit consists of an internal current source, external soft start timing capacitor, internal switch across the capacitor, and a comparator monitoring the capacitor voltage.

LINEAR REGULATOR CONTROLLER

1.5V Linear Regulator
This block is a linear regulator controller, which drives an external PNP bipolar transistor as a pass element. The linear regulator is capable of delivering 500mA steady state DC current and should support transient current of 1A, assuming the output filtering capacitor is properly selected to provide enough charge for the duration of the load transient.

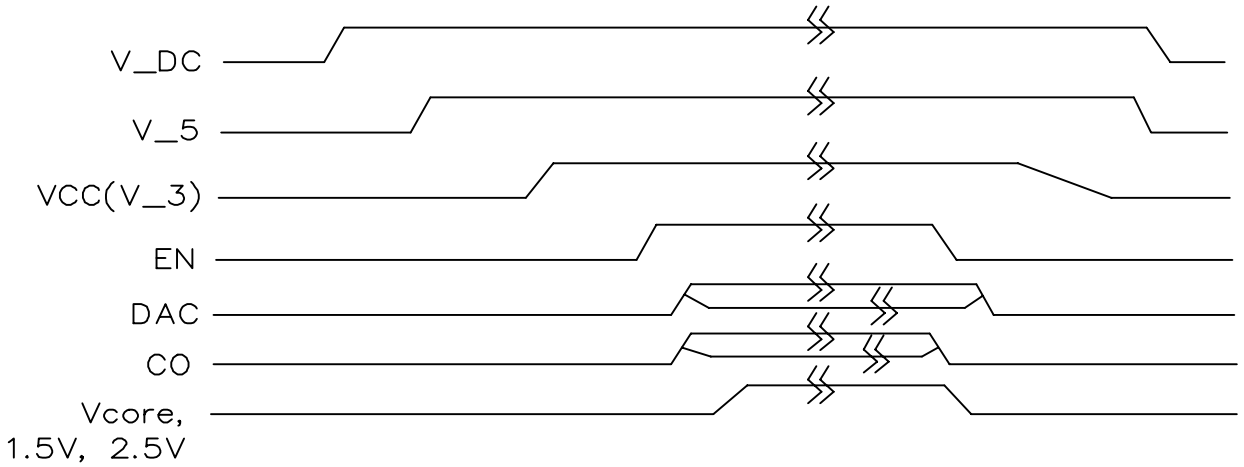
2.5V Linear Regulator
This block is a low drop-out (LDO) linear regulator controller, which drives an external PNP bipolar transistor as a pass element. The LDO linear regulator is capable of delivering 100mA steady DC current and should support transient current of 100mA, assuming the output filtering capacitor is properly selected to provide enough charge for the duration of the load transient.

Linear Regulator Soft Start Timer
A soft start timer circuit of the linear regulators is similar to that of the core converter, and is used to control the ramp up time of the linear regulator output voltages. For maximum flexibility in controlling the start up sequence, the soft start function of the linear regulators is separated from that of the core converter.

VOLTAGE CLAMP
The level translator converts an input voltage swing on the IO rail, into a voltage swing on the CLK or VCC rail depending on where the open drain output of the translator is tied to through an external pull-up resistor. The level translator has to track the input in phase, and must be able to switch in 5ns (typical) following an input threshold intercept.

APPLICATION INFORMATION

Power on/off Sequence



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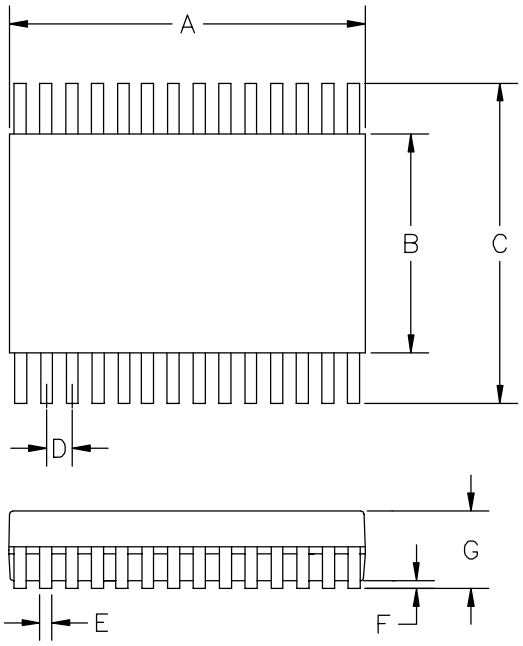
OUTLINE DRAWING - TSSOP-28



DIMENSIONS (1)					
DIM N	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.3779	.3858	9.60	9.80	(2)
B	.169	.177	4.30	4.50	(2)
C	.252 BSC		6.40 BSC		—
D	.026 BSC		.65 BSC		—
E	.007	.012	.19	.30	—
F	.0015	.0080	.05	.15	—
G		.078		1.20	—
J	.0040	.0100	.09	.20	—
K	0°	8°	0°	8°	—
L	.022	.037	.45	.75	—

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(2) DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

(1) CONTROLLING DIMENSIONS: MILLIMETERS.

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