

**96-Bit AC-PDP DRIVER**

The  $\mu$ PD16334 is a high-voltage CMOS driver designed for flat display panels such as PDPs, VFDs and ELs. It consists of a 96-bit bi-directional shift register, 96-bit latch and high-voltage CMOS driver. The logic block is designed to operate using a 5-V power supply/3.3-V interface enabling direct connection to a gate array or a microcontroller. In addition, the  $\mu$ PD16334 achieves low power dissipation by employing the CMOS structure while having a high withstand voltage output (80 V, 50 mA).

**FEATURES**

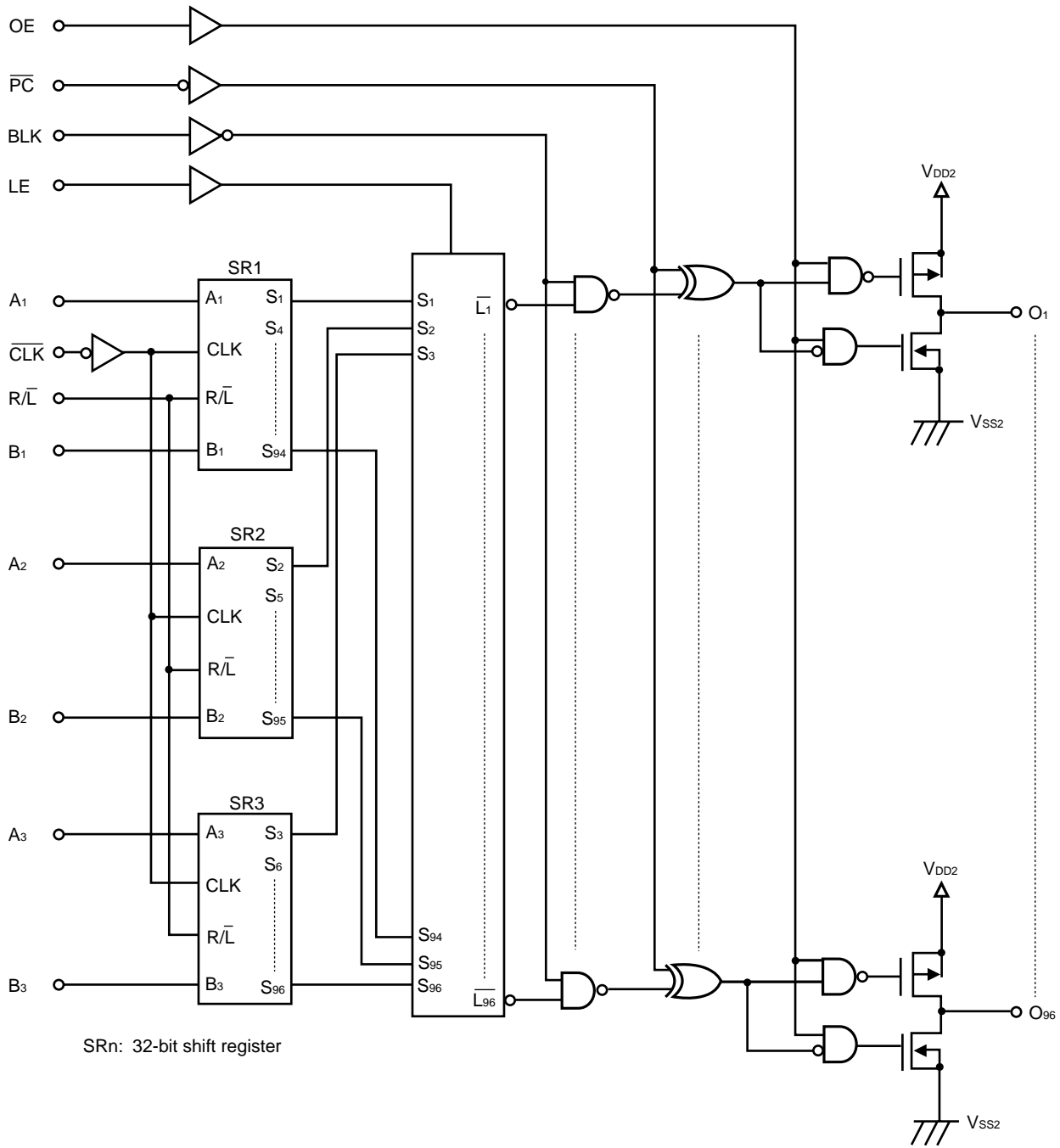
- Selectable by IBS pin; three 32-bit bi-directional shift register circuits configuration or six 16-bit bi-directional shift register circuits configuration
- Data control with transfer clock (external) and latch
- High-speed data transfer ( $f_{max.} = 25$  MHz min. at data fetch)  
( $f_{max.} = 15$  MHz min. at cascade connection)
- High withstand output voltage (80 V, 50 mA<sub>MAX.</sub>)
- 3.3 V CMOS input interface
- High withstand voltage CMOS structure
- Capable of reversing all driver outputs by  $\overline{PC}$  pin

**ORDERING INFORMATION**

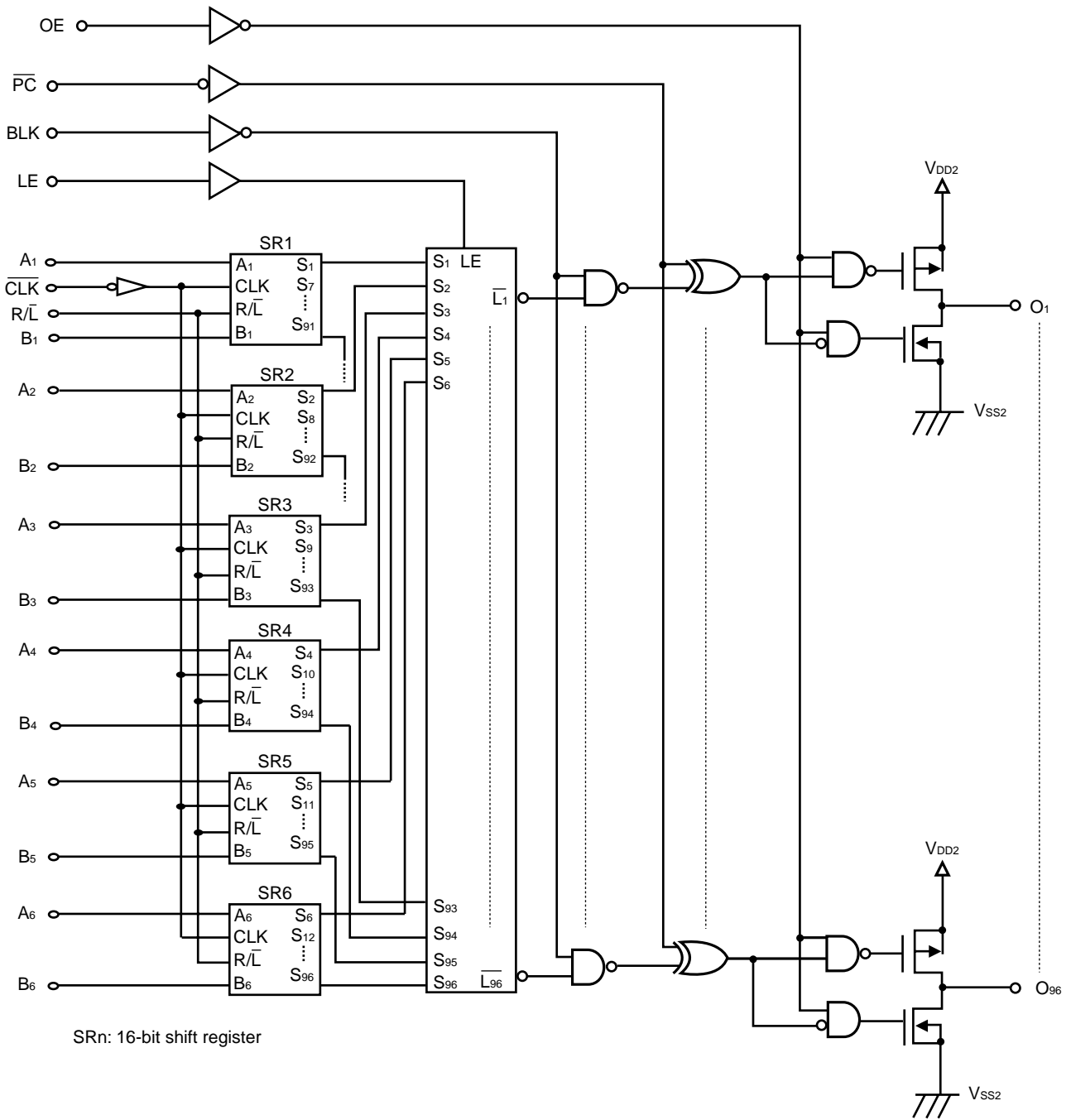
Part Number	Package
$\mu$ PD16334	COB*

\* Please consult with an NEC sales representative about COB.

BLOCK DIAGRAM (IBS = H, 3-BIT INPUT, 32-BIT LENGTH SHIFT REGISTER)



BLOCK DIAGRAM (IBS = L, 6-BIT INPUT, 16-BIT LENGTH SHIFT REGISTER)



**PIN DESCRIPTION**

Symbol	Pin Name	Description
PC	Polarity change input	PC = L: All driver output invert
BLK	Blank input	BLK = H : All output = H or L
LE	Latch enable input	Automatically executes latch by setting high at rising edge of the clock
OE	Output enable	Make output high impedance by input H
A <sub>1</sub> to A <sub>3 (6)</sub>	RIGHT data input/output <sup>(Note)</sup>	When R/L=H (values in parentheses are for 6-bit input) A <sub>1</sub> to A <sub>3 (6)</sub> : Input B <sub>1</sub> to B <sub>3 (6)</sub> : Output
B <sub>1</sub> to B <sub>3 (6)</sub>	LEFT data input/output <sup>(Note)</sup>	When R/L=L (values in parentheses are for 6-bit input) A <sub>1</sub> to A <sub>3 (6)</sub> : Output B <sub>1</sub> to B <sub>3 (6)</sub> : Input
CLK	Clock input	Shift executed on fall
R/L	Shift control input	Right shift mode when R/L= H SR <sub>1</sub> : A <sub>1</sub> → S <sub>1</sub> ...S <sub>94</sub> → B <sub>1</sub> (Same direction for SR <sub>2</sub> to SR <sub>6</sub> ) Left shift mode when R/L= L SR <sub>1</sub> : B <sub>1</sub> → S <sub>94</sub> ...S <sub>1</sub> → A <sub>1</sub> (Same direction for SR <sub>2</sub> to SR <sub>6</sub> )
IBS	Input mode switch	H: 32-bit length shift register, 3-bit input L: 16-bit length shift register, 6-bit input
O <sub>1</sub> to O <sub>96</sub>	High withstand voltage output	80 V, 50 mA <sub>MAX.</sub>
V <sub>DD1</sub>	Power supply for logic block	5 V ± 10 %
V <sub>DD2</sub>	Power supply for driver block	10 to 70 V
V <sub>SS1</sub>	Logic GND	Connect to system GND
V <sub>SS2</sub>	Driver GND	Connect to system GND

**Note** When input mode is 3-bit, set unused input and output pins “L” level.

**TRUTH TABLE 1 (Shift Register Block)**

Input		Output		Shift Register
R/L	CLK	A	B	
H	↓	Input	Output <sup>Note1</sup>	Right shift execution
H	H or L		Output	Hold
L	↓	Output <sup>Note2</sup>	Input	Left shift execution
L	H or L	Output		Hold

**Notes 1.** The data of S<sub>91</sub> to S<sub>93</sub> (S<sub>85</sub> to S<sub>90</sub>) shifts to S<sub>94</sub> to S<sub>96</sub> (S<sub>91</sub> to S<sub>96</sub>) and is output from B<sub>1</sub> to B<sub>3</sub> (B<sub>1</sub> to B<sub>6</sub>) at the falling edge of the clock, respectively. (Values in parentheses are for 6-bit input)

**2.** The data of S<sub>4</sub> to S<sub>6</sub> (S<sub>7</sub> to S<sub>12</sub>) shifts to S<sub>1</sub> to S<sub>3</sub> (S<sub>1</sub> to S<sub>6</sub>) and is output from A<sub>1</sub> to A<sub>3</sub> (A<sub>1</sub> to A<sub>6</sub>) at the falling edge of the clock, respectively (Values in parentheses are for 6-bit input)

**TRUTH TABLE 2 (Latch Block)**

LE	CLK	Output State of Latch Block (L <sub>n</sub> )
H	↑	Latch S <sub>n</sub> data and hold output data
	↓	Hold latch data
L	X	Hold latch data

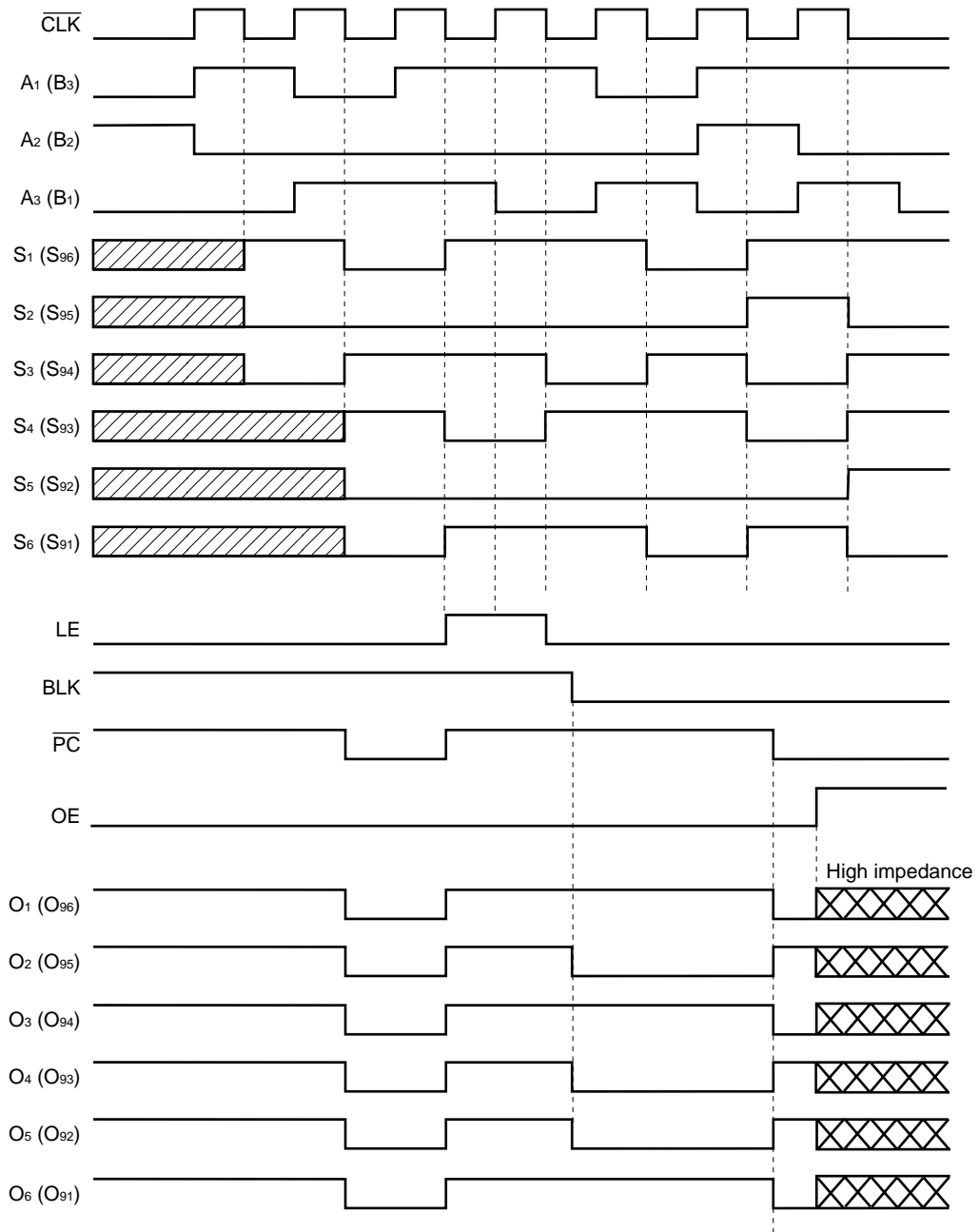
**TRUTH TABLE 3 (Driver Block)**

L <sub>n</sub>	BLK	PC	OE	Output State of Driver Block
X	H	H	L	H (All driver outputs: H)
X	H	L	L	L (All driver outputs: L)
X	L	H	L	Output latch data (L <sub>n</sub> )
X	L	L	L	Output inverted latch data (L <sub>n</sub> )
X	X	X	H	Set output impedance high

X: H or L, H: High level, L: Low level

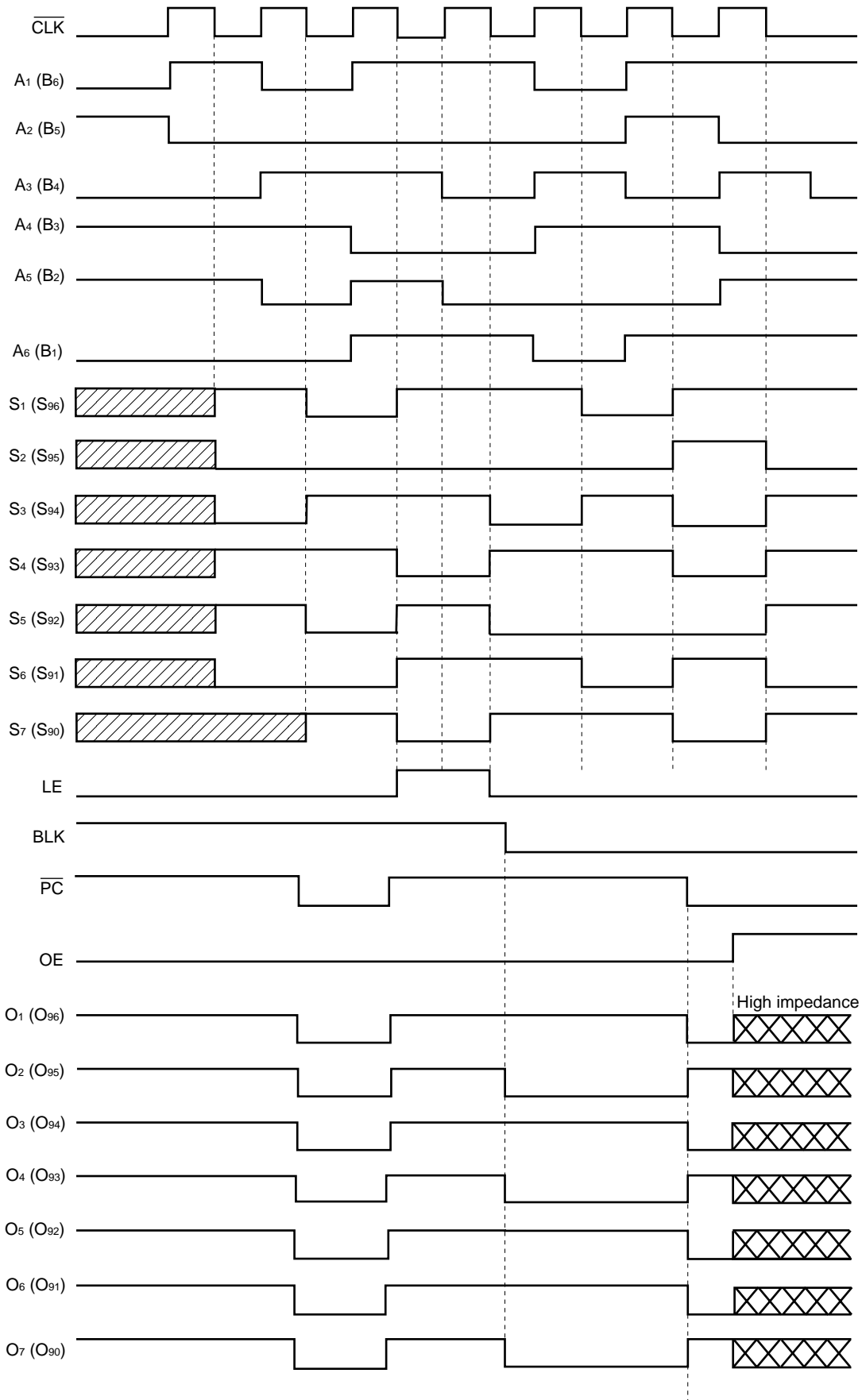
**TIMING CHART (WHEN IBS="H": 3-BIT INPUT, RIGHT SHIFT)**

Values in parentheses in the following chart are when R/L=L.



**TIMING CHART (WHEN IBS="L": 6-BIT INPUT, RIGHT SHIFT)**

Values in parentheses in the following chart are when R/L=L.



**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	Ratings	Unit
Logic Block Supply Voltage	V <sub>DD1</sub>	-0.5 to +7.0	V
Driver Block Supply Voltage	V <sub>DD2</sub>	-0.5 to +80	V
Logic Block Input Voltage	V <sub>I</sub>	-0.5 to V <sub>DD1</sub> + 0.5	V
Driver Block Output Current	I <sub>O2</sub>	50	mA
Junction Temperature	T <sub>j</sub>	+125	°C
Storage Temperature	T <sub>stg.</sub>	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = -40 to +85 °C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Block Supply Voltage	V <sub>DD1</sub>	4.75	5.0	5.25	V
Driver Block Supply Voltage	V <sub>DD2</sub>	10		70	V
High-Level Input Voltage	V <sub>IH</sub>	2.7		V <sub>DD1</sub>	V
Low-Level Input Voltage	V <sub>IL</sub>	0		0.6	V
Driver Output Current	I <sub>OH2</sub>			-40	mA
	I <sub>OL2</sub>			+40	mA

**Caution** In order to prevent latch-up breakage, be sure to enter the power to V<sub>DD1</sub>, logic signal and V<sub>DD2</sub> in that order, and turn off the power in the reverse order, keep this order also during a transition period.

**ELECTRICAL SPECIFICATIONS (T<sub>A</sub> = 25 °C, V<sub>DD1</sub> = 5.0 V, V<sub>DD2</sub> = 70 V, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-Level Output Voltage	V <sub>OH1</sub>	Logic, I <sub>OH1</sub> = -1.0 mA	0.9 • V <sub>DD1</sub>		V <sub>DD1</sub>	V
Low-Level Output Voltage	V <sub>OL1</sub>	Logic, I <sub>OL1</sub> = 1.0 mA	0		0.1 V <sub>DD1</sub>	V
High-Level Output Voltage	V <sub>OH21</sub>	O <sub>1</sub> to O <sub>96</sub> , I <sub>OH2</sub> = -1 mA	69			V
	V <sub>OH22</sub>	O <sub>1</sub> to O <sub>96</sub> , I <sub>OH2</sub> = -10 mA	65			V
Low-Level Output Voltage	V <sub>OL21</sub>	O <sub>1</sub> to O <sub>96</sub> , I <sub>OL2</sub> = 5 mA			1.0	V
	V <sub>OL22</sub>	O <sub>1</sub> to O <sub>96</sub> , I <sub>OL2</sub> = 40 mA			10	V
Input Leakage Current	I <sub>IL</sub>	V <sub>I</sub> = V <sub>DD1</sub> or V <sub>SS1</sub>			±1.0	μA
High-Level Input Voltage	V <sub>IH</sub>	V <sub>DD1</sub> = 4.75 to 5.25 V	2.7			V
Low-Level Input Voltage	V <sub>IL</sub>	V <sub>DD1</sub> = 4.75 to 5.25 V			0.6	V
Static Current Dissipation	I <sub>DD1</sub>	Logic, T <sub>A</sub> = -40 to +85 °C			10 <sup>Note</sup>	mA
	I <sub>DD1</sub>	Logic, T <sub>A</sub> = 25 °C			10 <sup>Note</sup>	mA
	I <sub>DD2</sub>	Driver, T <sub>A</sub> = -40 to +85 °C			1000	μA
	I <sub>DD2</sub>	Driver, T <sub>A</sub> = 25 °C			100	μA

**Note** When all inputs are high-level (V<sub>IH</sub> = 2.7 V to V<sub>DD1</sub>, the R/L and IBS pins are fixed to V<sub>I</sub> = V<sub>SS1</sub> or V<sub>DD1</sub>)

**SWITCHING CHARACTERISTICS (TA = 25 °C, VDD1 = 5 V, VDD2 = 70 V, VSS1 = VSS2 = 0 V, Logic CL = 15 pF, Driver CL = 50 pF, tr = tr = 6.0 ns)**

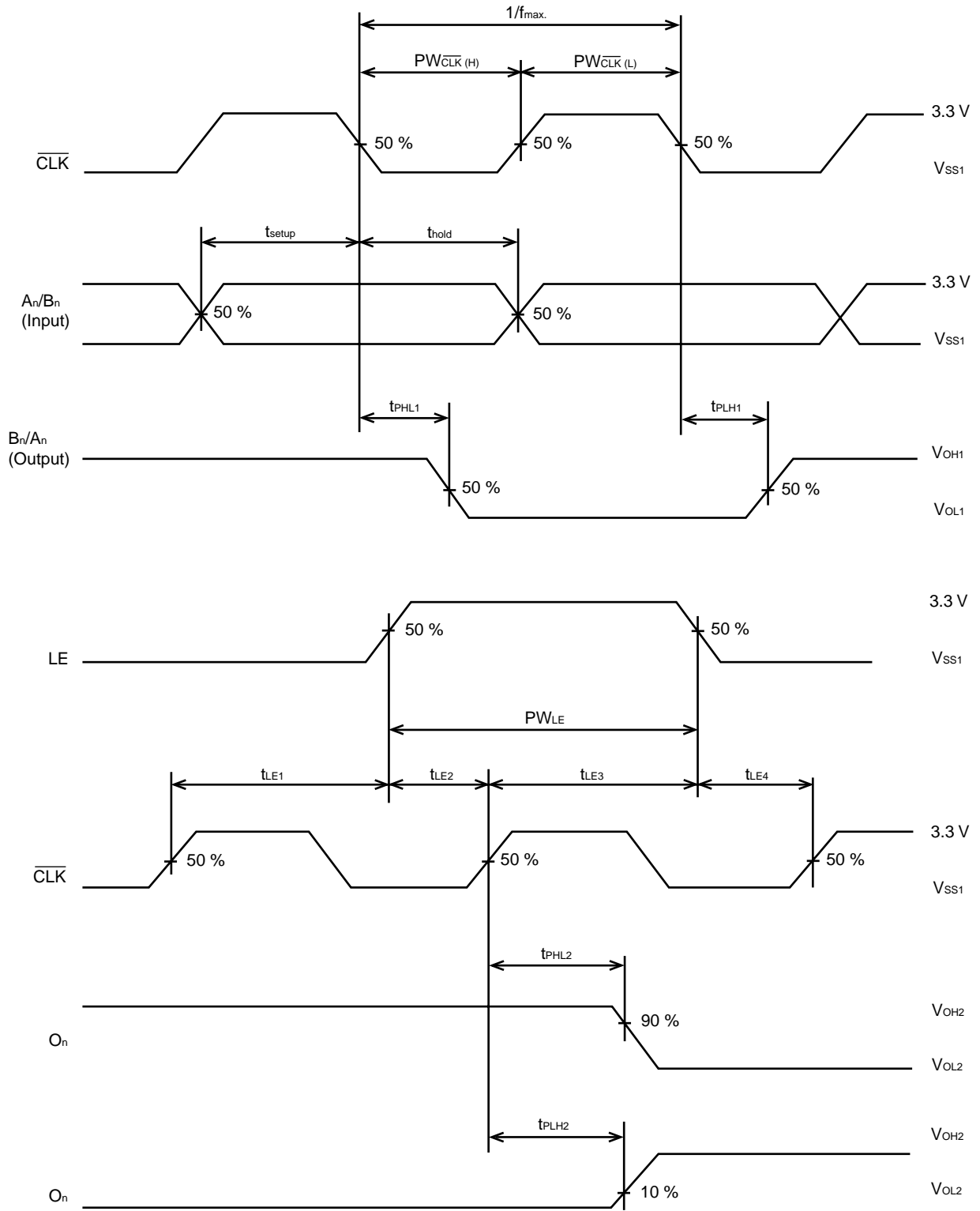
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transmission Delay time	t <sub>PHL1</sub>	$\overline{\text{CLK}} \downarrow \rightarrow \text{A/B}$			55	ns
	t <sub>PLH1</sub>				55	ns
	t <sub>PHL2</sub>	$\overline{\text{CLK}} \uparrow (\text{LE} = \text{H}) \rightarrow \text{O}_1 \text{ to } \text{O}_{96}$			180	ns
	t <sub>PLH2</sub>				180	ns
	t <sub>PHL3</sub>	$\text{BLK} \rightarrow \text{O}_1 \text{ to } \text{O}_{96}$			165	ns
	t <sub>PLH3</sub>				165	ns
	t <sub>PHL4</sub>	$\overline{\text{PC}} \rightarrow \text{O}_1 \text{ to } \text{O}_{96}$			160	ns
	t <sub>PLH4</sub>				160	ns
	t <sub>PHZ</sub>	$\text{OE} \rightarrow \text{O}_1 \text{ to } \text{O}_{96}$			300	ns
	t <sub>PZH</sub>	$\text{RL} = 10 \text{ k}\Omega$			180	ns
	t <sub>PLZ</sub>				300	ns
	t <sub>PZL</sub>				180	ns
Rise Time	t <sub>TLH</sub>	$\text{O}_1 \text{ to } \text{O}_{96}$			150	ns
	t <sub>TLZ</sub>	$\text{RL} = 10 \text{ k}\Omega$			3	μs
	t <sub>TZH</sub>	$\text{O}_1 \text{ to } \text{O}_{96}$			150	ns
Fall Time	t <sub>THL</sub>	$\text{O}_1 \text{ to } \text{O}_{96}$			150	ns
	t <sub>THZ</sub>	$\text{RL} = 10 \text{ k}\Omega$			3	μs
	t <sub>TZL</sub>	$\text{O}_1 \text{ to } \text{O}_{96}$			150	ns
Maximum Clock Frequency	f <sub>max.</sub>	When data is read, duty 50 %	25			MHz
		cascade connection, Duty 50 %	15			MHz
Input Capacitance	C <sub>i</sub>				15	pF

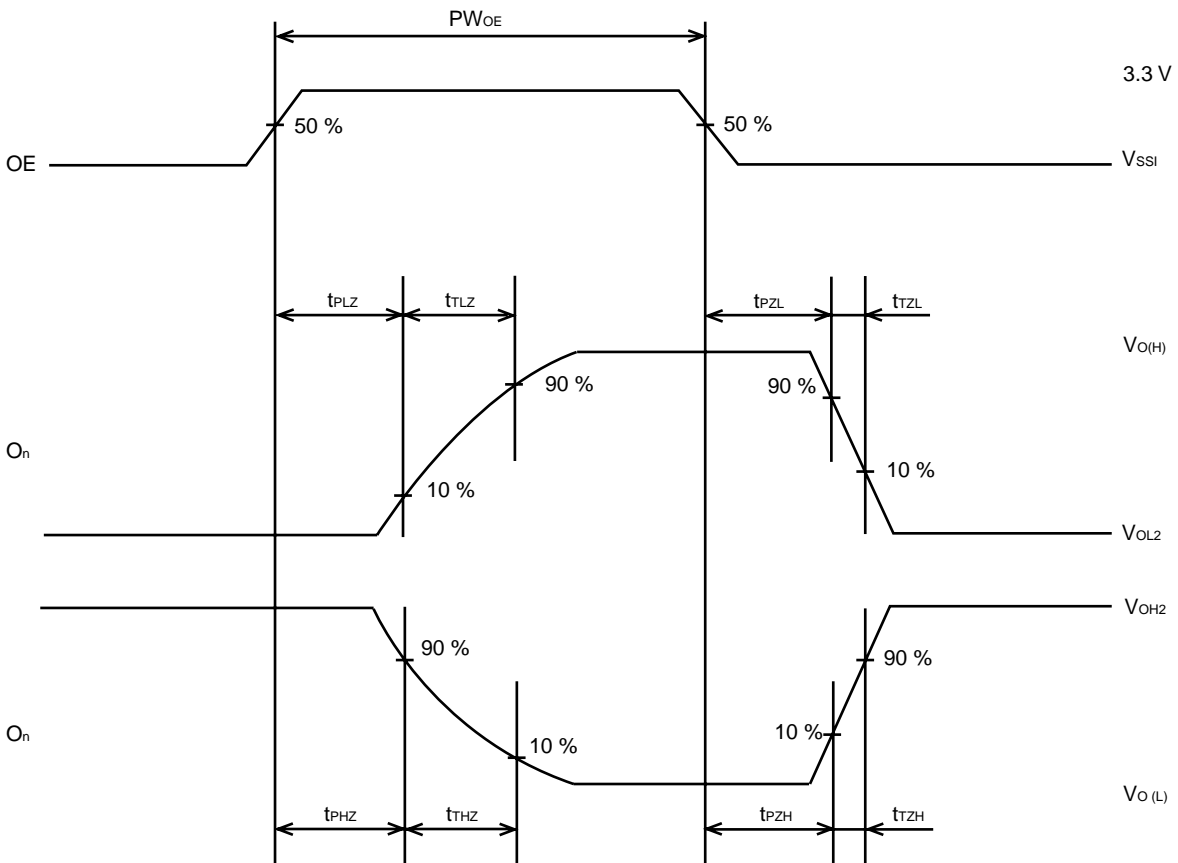
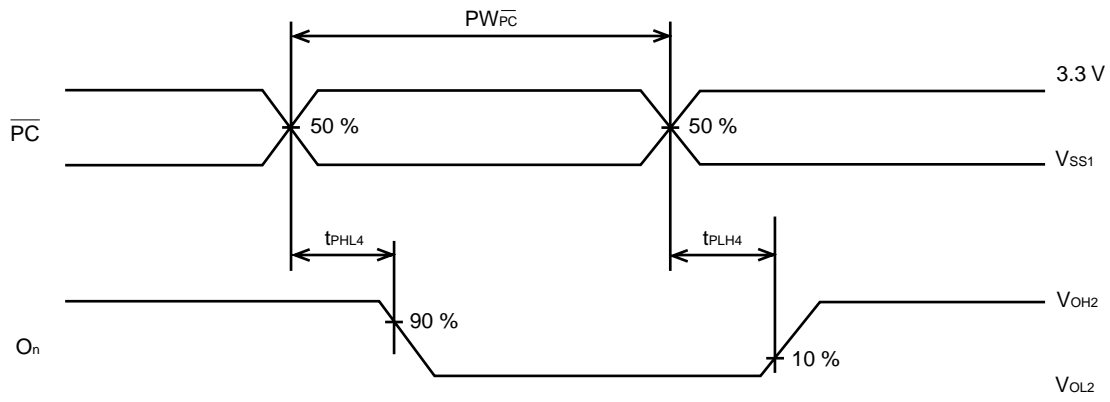
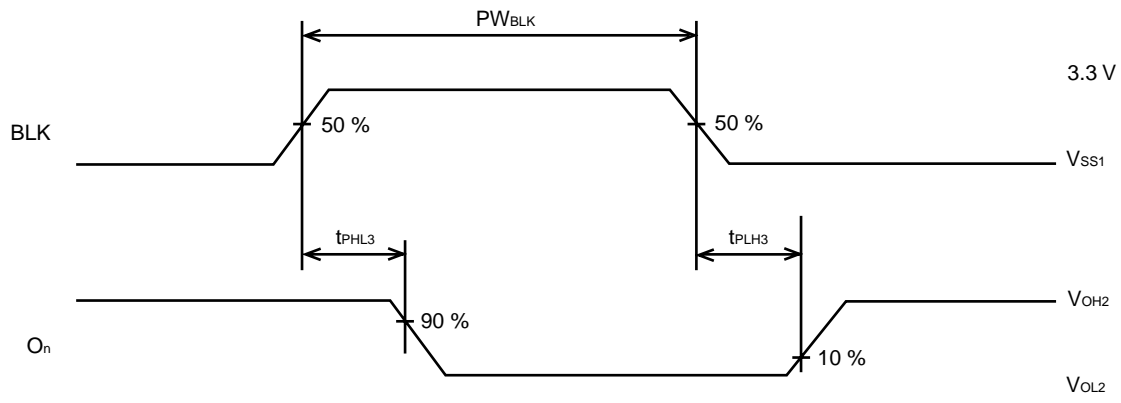
**TIMING REQUIREMENT (TA = -40 to +85 °C, VDD1 = 4.75 to 5.25 V, VSS1,2 = 0 V, tr = tr = 6.0 ns)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW <sub><math>\overline{\text{CLK}}</math></sub>		20			ns
Latch Enable Pulse Width	PW <sub>LE</sub>		30			ns
Blank Pulse Width	PW <sub>BLK</sub>		200			ns
$\overline{\text{PC}}$ Pulse Width	PW <sub><math>\overline{\text{PC}}</math></sub>		200			ns
OE Pulse Width	PW <sub>OE</sub>	$\text{RL} = 10 \text{ k}\Omega$	3.3			μs
Data Setup Time	t <sub>setup</sub>		10			ns
Data Hold Time	t <sub>hold</sub>		10			ns
Latch Enable Time 1	t <sub>LE1</sub>		25			ns
Latch Enable Time 2	t <sub>LE2</sub>		5			ns
Latch Enable Time 3	t <sub>LE3</sub>		25			ns
Latch Enable Time 4	t <sub>LE4</sub>		5			ns



SWITCHING CHARACTERISTICS WAVEFORM





[MEMO]

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